

PETITORIO

Industria y Comercio
SUPERINTENDENCIA

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Radicación: 02091936 00000000 Folios: 384
Fecha (MM/AA): 2002-10-11 15:07:13
Trámite: 011 PCT-PATENT 370 FASE NNCI 411 PRESENTAC
Dependencia: 2020 DIVISION DE NUEVAS CREACIONES

FORMULARIO UNICO DE SOLICITUD DE PATENTE
PCT
ENTRADA EN FASE NACIONAL

①

SOLICITUD DE:

☒

Patente de Invención

☐

Patente de Modelo de Utilidad

☒

Capítulo I

☒

Capítulo II

②

SOLICITANTE
(71)

Nombre: ZENITH ELECTRONICS CORPORATION

Dirección: 2000 Millbrook Drive, Lincolnshire, Illinois
60069, Estados Unidos de AméricaNacionalidad o Domicilio: Estado de Illinois, Estados
Unidos de AméricaLugar de Constitución: Estado de Illinois, Estados
Unidos de América

Teléfono: 3123800

Fax: 3122410

E-mail: general@cardenasycardenas.com

IDENTIFICACIÓN

C.C. ☐NIT ☐C.E. ☐Otro ☒

Cual _____

Número _____

③

REPRESENTANTE
O APODERADO

Nombre: DARIO CARDENAS NAVAS

Dirección: Carrera 7 No 71-52 Torre B Piso 9

Teléfono: 3123800

Fax: 3122410

E-Mail: general@cardenasycardenas.com

IDENTIFICACION

C.C. ☒NIT ☐C.E. ☐Otro ☐

Cual _____

No 17.088.829 TP 1.250

④

INVENTOR(ES)
(72)Nombre: 1. RICHARD W. CITTA
2. MARK FIMOFF
3. PAUL A. SNOPKODirección: 1. 739 Columbian, Oak Park, Illinois 60302, Estados Unidos de América
2. 1020 Concord Lane, Hoffman Estates, Illinois 60195, Estados Unidos
de América
3. 360 E. Randolph Dr. Chicago, Illinois 60601, Estados Unidos de
AméricaNacionalidad o Domicilio: 1. Illinois, Estados Unidos de América
2. Illinois, Estados Unidos de América
3. Illinois, Estados Unidos de América

⑤ PCT (88)

Solicitud Internacional No. PCT/US01/09734

Fecha Marzo 27, 2001

Publicación Internacional No. WO 01/78495 A2

Fecha Octubre 25, 2001

⑥

Título(54): RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

Clasificación Internacional (51):

H04L27/02

⑧

Prioridad

SI ☒ NO ☐

(33) País de Origen

U.S.A.

U.S.A.

U.S.A.

(32) Fecha

Abril 18, 2000

Diciembre 13, 2000

Diciembre 13, 2000

(31) N° de Solicitud

60 / 198,014

60 / 255,476

60 / 255,464

⑨

Comprobante de Pago No.:

02 - 67,397

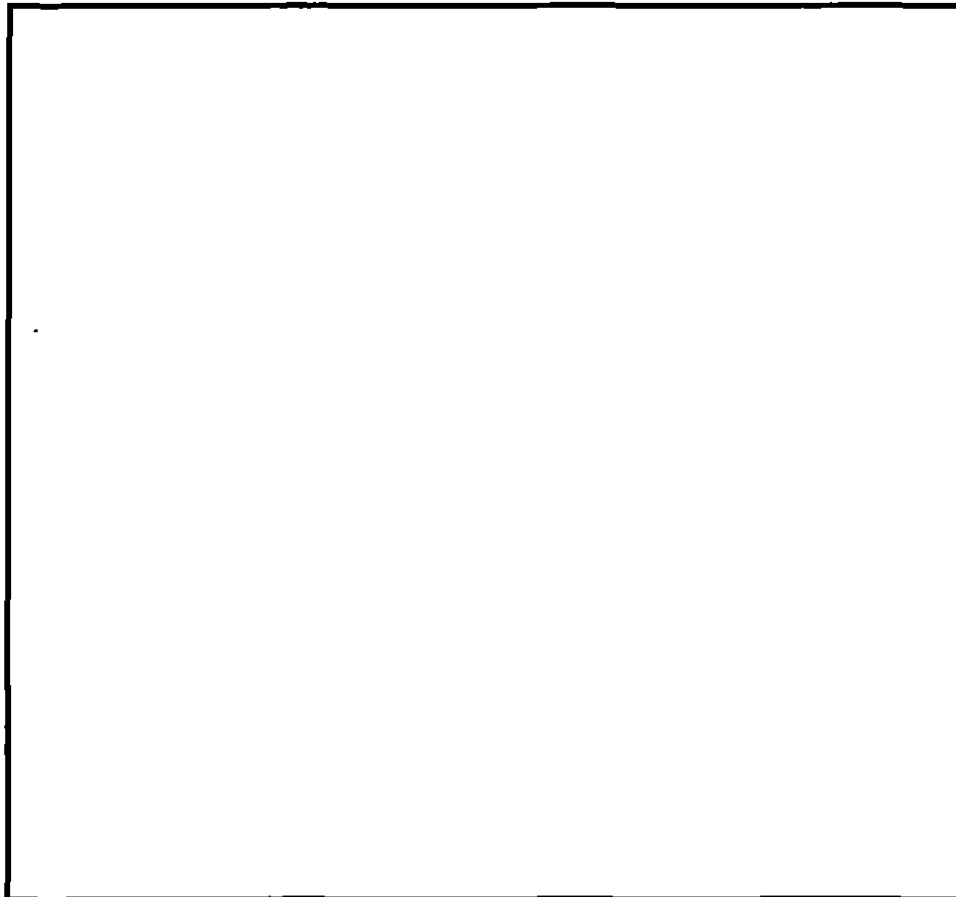
Fecha Octubre 8, 2002

10

ANEXOS

- ☒ Comprobante de pago de la tasa de presentación de la solicitud.
- ☐ Documento que acredita la existencia y representación legal cuando el solicitante sea persona jurídica.
- ☐ Poderes, si fuere el caso.
- ☐ Documento de cesión del inventor al solicitante o a su causante.
- ☒ Declaraciones
- ☒ Copia de la solicitud internacional. (Resumen, descripción, reivindicaciones, dibujos)
- ☒ Traducción de la solicitud internacional al castellano. (Resumen, descripción, reivindicaciones, dibujos)
- ☒ Copia del examen preliminar internacional efectuado por la Autoridad Internacional de Examen Preliminar (IPEA).
- ☒ Traducción del examen preliminar internacional efectuado por la IPEA.
- ☐ De ser el caso, copia del contrato de acceso.
- ☐ De ser el caso, documento que acredita la licencia o autorización de uso de conocimientos tradicionales de las comunidades indígenas.
- ☐ De ser el caso, certificado de depósito del material biológico.
- ☐ Arte final 12x12.
- ☐ De ser el caso, información sobre otras solicitudes de patente o títulos obtenidos en el extranjero por el mismo titular o su causante, relacionadas parcial o totalmente con la invención de esta solicitud.
- ☐ De ser el caso, modificaciones efectuadas a la solicitud internacional.
- ☐ Otros.

11 FIGURA CARACTERISTICA



12

Solicito la Concesión de la patente,

NOMBRE: DARIO CARDENAS NAVAS

FIRMA:

C.C. 17.066.629 TP. 1.250 LV

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference
(if desired) (12 characters maximum) 29471/37034

Box No. I TITLE OF INVENTION ENHANCED SLICE PREDICTION FEEDBACK		Retoolimentación de la Predicción Segonda de Secciones	
Box No. II APPLICANT			
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) ZENITH ELECTRONICS CORPORATION 2000 Milbrook Drive Lincolnshire, Illinois 60069 United States of America		☐ This person is also inventor. Telephone No. 847/941-8018 Facsimile No. 847/941-8003 Teleprinter No.	
State (that is, country) of nationality: US		State (that is, country) of residence: US	
This person is applicant for the purposes of:		☒ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box	
Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)			
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) CITTA, Richard W. 739 Columbian Oak Park, Illinois 60302 United States of America		This person is: ☐ applicant only ☐ applicant and inventor ☒ inventor only (If this check-box is marked, do not fill in below.)	
State (that is, country) of nationality: US		State (that is, country) of residence: US	
This person is applicant for the purposes of:		☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box	
☒ Further applicants and/or (further) inventors are indicated on a continuation sheet.			
Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE			
The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:		☒ agent ☐ common representative	
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.) JOIKE, Trevor B. MARSHALL, O'TOOLE, GERSTEIN, MURRAY & BORUN 6300 Sears Tower 233 S. Wacker Drive Chicago, Illinois 60606 United States of America		Telephone No. 312/474-6300 Facsimile No. 312/474-0448 Teleprinter No.	
☐ Address for correspondence: Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.			

Continuation of Box No. III FURTHER APPLICANTS AND/OR (FURTHER) INVENTOR(S)

If none of the following sub-boxes is used, this sheet is not to be included in the request.

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)

FIMOFF, Mark
1020 Concord Lane
Hoffman Estates, Illinois 60185
United States of America

This person is:

- ☐ applicant only
☐ applicant and inventor
☒ inventor only (If this check-box is marked, do not fill in below.)

State (that is, country) of nationality:

State (that is, country) of residence:

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)

SNOPKO, Paul A.
380 E. Randolph Dr.
Chicago, Illinois 60601
United States of America

This person is:

- ☐ applicant only
☐ applicant and inventor
☒ inventor only (If this check-box is marked, do not fill in below.)

State (that is, country) of nationality:

State (that is, country) of residence:

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)

This person is:

- ☐ applicant only
☐ applicant and inventor
☐ inventor only (If this check-box is marked, do not fill in below.)

State (that is, country) of nationality:

State (that is, country) of residence:

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)

This person is:

- ☐ applicant only
☐ applicant and inventor
☐ inventor only (If this check-box is marked, do not fill in below.)

State (that is, country) of nationality:

State (that is, country) of residence:

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on another continuation sheet.

Box No.V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) (mark the applicable check-boxes; at least one must be marked).

Regional Patent

- ☒ **AP** ARIPO Patent: GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, MZ Mozambique, SD Sudan, SL Sierra Leone, SZ Swaziland, TZ United Republic of Tanzania, UG Uganda, ZW Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☒ **EA** Eurasian Patent: AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☒ **EP** European Patent: AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, CY Cyprus, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☒ **OA** OAPI Patent: BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, GW Guinea-Bissau, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT (if other kind of protection or treatment desired, specify on dotted line)

National Patent (if other kind of protection or treatment desired, specify on dotted line):

- | | |
|---|---|
| ☒ AE United Arab Emirates | ☒ LC Saint Lucia |
| ☒ AG Antigua and Barbuda | ☒ LK Sri Lanka |
| ☒ AL Albania | ☒ LR Liberia |
| ☒ AM Armenia | ☒ LS Lesotho |
| ☒ AT Austria | ☒ LT Lithuania |
| ☒ AU Australia | ☒ LU Luxembourg |
| ☒ AZ Azerbaijan | ☒ LV Latvia |
| ☒ BA Bosnia and Herzegovina | ☒ MA Morocco |
| ☒ BB Barbados | ☒ MD Republic of Moldova |
| ☒ BG Bulgaria | ☒ MG Madagascar |
| ☒ BR Brazil | ☒ MK The former Yugoslav Republic of Macedonia |
| ☒ BY Belarus | ☒ MN Mongolia |
| ☒ BZ Belize | ☒ MW Malawi |
| ☒ CA Canada | ☒ MX Mexico |
| ☒ CH and LI Switzerland and Liechtenstein | ☒ MZ Mozambique |
| ☒ CN China | ☒ NO Norway |
| ☒ CR Costa Rica | ☒ NZ New Zealand |
| ☒ CU Cuba | ☒ PL Poland |
| ☒ CZ Czech Republic | ☒ PT Portugal |
| ☒ DE Germany | ☒ RO Romania |
| ☒ DK Denmark | ☒ RU Russian Federation |
| ☒ DM Dominica | ☒ SD Sudan |
| ☒ DZ Algeria | ☒ SE Sweden |
| ☒ EE Estonia | ☒ SG Singapore |
| ☒ ES Spain | ☒ SI Slovenia |
| ☒ FI Finland | ☒ SK Slovakia |
| ☒ GB United Kingdom | ☒ SL Sierra Leone |
| ☒ GD Grenada | ☒ TJ Tajikistan |
| ☒ GE Georgia | ☒ TM Turkmenistan |
| ☒ GH Ghana | ☒ TR Turkey |
| ☒ GM Gambia | ☒ TT Trinidad and Tobago |
| ☒ HR Croatia | ☒ TZ United Republic of Tanzania |
| ☒ HU Hungary | ☒ UA Ukraine |
| ☒ ID Indonesia | ☒ UG Uganda |
| ☒ IL Israel | ☐ US United States of America |
| ☒ IN India | ☒ UZ Uzbekistan |
| ☒ IS Iceland | ☒ VN Viet Nam |
| ☒ JP Japan | ☒ YU Yugoslavia |
| ☒ KE Kenya | ☒ ZA South Africa |
| ☒ KG Kyrgyzstan | ☒ ZW Zimbabwe |
| ☒ KP Democratic People's Republic of Korea | |
| ☒ KR Republic of Korea | |
| ☒ KZ Kazakhstan | |

Check-boxes reserved for designating States which have become party to the PCT after issuance of this sheet:

☒ **CO** Colombia

Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all other designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. (Confirmation (including fees) must reach the receiving Office within the 15-month time limit.)

Supplemental Box *If the Supplemental Box is not used, this sheet need not be included in the request.*

1. If, in any of the Boxes, the space is insufficient to furnish all the information: in such case, write "Continuation of Box No. ..." [Indicate the number of the Box] and furnish the information in the same manner as required according to the captions of the Box in which the space was insufficient, in particular:

- (i) If more than two persons are involved as applicants and/or inventors and no "continuation sheet" is available: in such case, write "Continuation of Box No. III" and indicate for each additional person the same type of information as required in Box No. III. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below;
- (ii) If, in Box No. II or in any of the sub-boxes of Box No. III, the indication "the States indicated in the Supplemental Box" is checked: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the applicant(s) involved and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is applicant;
- (iii) If, in Box No. II or in any of the sub-boxes of Box No. III, the inventor or the inventor/applicant is not inventor for the purposes of all designated States or for the purposes of the United States of America: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the inventor(s) and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is inventor;
- (iv) If, in addition to the agent(s) indicated in Box IV, there are further agents: in such case, write "Continuation of Box No. IV" and indicate for each further agent the same type of information as required in Box No. IV;
- (v) If, in Box No. V, the name of any State (or OAPI) is accompanied by the indication "patent of addition," or "certificate of addition," or if, in Box No. V, the name of the United States of America is accompanied by an indication "continuation" or "continuation-in-part": in such case, write "Continuation of Box No. V" and the name of each State involved (or OAPI), and after the name of each such State (or OAPI), the number of the parent title or parent application and the date of grant of the parent title or filing of the parent application;
- (vi) If, in Box No. VI, there are more than three earlier applications whose priority is claimed: in such case, write "Continuation of Box No. VI" and indicate for each additional earlier application the same type of information as required in Box No. VI;
- (vii) If, in Box No. VI, the earlier application is an ARIPO application: in such case, write "Continuation of Box No. VI", specify the number of the item corresponding to that earlier application and indicate at least one country party to the Paris Convention for the Protection of Industrial Property or one Member of the World Trade Organization for which that earlier application was filed.

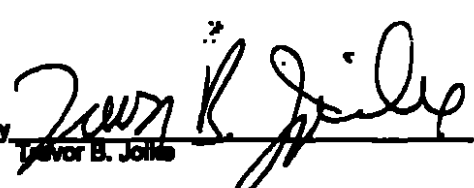
2. If, with regard to the precautionary designation statement contained in Box No. V, the applicant wishes to exclude any State(s) from the scope of that statement: in such case, write "Designation(s) excluded from precautionary designation statement" and indicate the name or two-letter code of each State so excluded.

3. If the applicant claims, in respect of any designated Office, the benefits of provisions of the national law concerning non-prejudicial disclosures or exceptions to lack of novelty: in such case, write "Statement concerning non-prejudicial disclosures or exceptions to lack of novelty" and furnish that statement below.

Continuation of Box VI

13 March 2001 Unassigned US
(13.03.01)

7

Box No. VI PRIORITY CLAIM		☐ Further priority claims are indicated in the Supplemental Box.		
Filing date of earlier application (day/month/year)	Number of earlier application	Where earlier application is:		
		national application: country	regional application: regional Office	international application: receiving Office
Item (1) 18 April 2000 (18.04.00)	60/188,014	US		
Item (2) 13 December 2000 (13.12.00)	60/255,478	US		
Item (3) 13 December 2000 (13.12.00)	60/255,484	US		
☒ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) (only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office) identified above as item(s): 1, 2, 3, and 4 . * Where the earlier application is an ARIPO application, it is mandatory to indicate in the Supplemental Box at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(a)(ii)). See Supplemental Box.				
Box No. VII INTERNATIONAL SEARCHING AUTHORITY				
Choice of International Searching Authority (ISA) (If two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used): ISA/EP		Request to use results of earlier search; reference to that search (if an earlier search has been carried out by or requested from the International Searching Authority): Date (day/month/year) Number Country (or regional Office)		
Box No. VIII CHECK LIST: LANGUAGE OF FILING				
This international application contains the following number of sheets: request : 5 description (excluding sequence listing part) : 45 claims : 6 abstract : 1 drawings : 12 sequence listing part of description : Total number of sheets : 69		This international application is accompanied by the item(s) marked below: 1. ☒ fee calculation sheet 2. ☐ separate signed power of attorney 3. ☒ copy of general power of attorney; reference number, if any: 4. ☐ statement explaining lack of signature 5. ☐ priority document(s) identified in Box No. VI as item(s): 6. ☐ translation of international application into (language): 7. ☐ separate indications concerning deposited microorganism or other biological material 8. ☐ nucleotide and/or amino acid sequence listing in computer readable form 9. ☒ other (specify): postcard		
Figure of the drawings which should accompany the abstract:		Language of filing of the international application: English		
Box No. IX SIGNATURE OF APPLICANT OR AGENT				
Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request). By  Trevor B. Jolles				

For receiving Office use only		2. Drawings: ☐ received: ☐ not received:
1. Date of actual receipt of the purported international application:		
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:		
4. Date of timely receipt of the required corrections under PCT Article 11(2):		
5. International Searching Authority (if two or more are competent): ISA/	6. ☐ Transmittal of search copy delayed until search fee is paid.	

For International Bureau use only
Date of receipt of the record copy by the International Bureau:

8
888

PCT

FEE CALCULATION SHEET

Annex to the Request

For receiving Office use only

International application No.

Applicant's or agent's
file reference

29417/37034

Date stamp of the receiving Office

Applicant
ZENITH ELECTRONICS CORPORATION

CALCULATION OF PRESCRIBED FEES

1. TRANSMITTAL FEE	240.00	T	
2. SEARCH FEE	848.00	S	
International search to be carried out by <u>EP</u>			
<i>(If two or more International Searching Authorities are competent in relation to the international application, indicate the name of the Authority which is chosen to carry out the international search.)</i>			
3. INTERNATIONAL FEE			
Basic Fee			
The international application contains <u>88</u> sheets.			
first 30 sheets	362.00	b1	
<u>30</u> x <u>\$9.00</u>	341.00	b2	
remaining sheets additional amount			
Add amounts entered at b1 and b2 and enter total at B	733.00	B	
Designation Fees			
The international application contains <u>87</u> designations.			
<u>8</u> x <u>\$2.00</u>	482.00	D	
number of designation fees payable (maximum 6)			
Add amounts entered at B and D and enter total at I	1,225.00	I	
<i>(Applicants from certain States are entitled to a reduction of 75% of the international fee. Where the applicant is (or all applicants are) so entitled, the</i>			
4. FEE FOR PRIORITY DOCUMENT (if applicable)		P	
5. TOTAL FEES PAYABLE	2,311.00		
Add amounts entered at T, S, I and P, and enter total in the TOTAL box	TOTAL		

☐ The designation fees are not paid at this time.

MODE OF PAYMENT

- | | | |
|---|---|---|
| ☐ authorization to charge
deposit account (see below) | ☐ bank draft | ☐ coupons |
| ☒ cheque | ☐ cash | ☐ other (specify): |
| ☐ postal money order | ☐ revenue stamps | |

DEPOSIT ACCOUNT AUTHORIZATION *(this mode of payment may not be available at all receiving Offices)*The RO/ US ☐ is hereby authorized to charge the total fees indicated above to my deposit account.☒ *(this check-box may be marked only if the conditions for deposit accounts of the receiving Office so permit)* i hereby authorized to charge any deficiency or credit any overpayment in the total fees indicated above to my deposit account.☒ is hereby authorized to charge the fee for preparation and transmittal of the priority document to the International Bureau of WIPO to my deposit account.

13-2858

Deposit Account No.

Date (day/month/year)

Signature

PATENT COOPERATION TREATY

[Handwritten signature] 9

General Appointment of Agent

The undersigned applicant appoints:

Trevor B. Joice
MARSHALL, O'TOOLE, GERSTEIN,
MURRAY & BORUN
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
United States of America
(312) 474-6300

as agent, to act on its behalf before the competent
International Authorities in connection with any and
all international applications filed by it and of which
it is the sole applicant.

Date: October 13, 1997

Zenith Electronics Corporation
a Delaware corporation
1000 Milwaukee Avenue
Glenview, Illinois 60025
U.S.A.

By: *[Handwritten signature]*
Name: Richard F. Vitkus
Title: Secretary

PCT**(TRATADO DE COOPERACIÓN PARA PATENTES)**

El suscrito solicita que la presente solicitud internacional
se tramite de conformidad con el
Tratado de Cooperación de Patentes.

Referencia del archivo del solicitante o del agente:

29471/37034

Casilla No. I. TÍTULO DEL INVENTO:

RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

Casilla No. II.

SOLICITANTE: **ZENITH ELECTRONICS CORPORATION**
2000 Millbrook Drive
Lincolnshire, Illinois 60069
Estados Unidos de América

TELÉFONO: **847/941-8018**

FAX: **847/941-8003**

NACIONALIDAD: **NORTEAMERICANA**

PAÍS DE RESIDENCIA: **ESTADOS UNIDOS**

Esta persona es el solicitante para los propósitos de:

☒ Todos los Estados Designados

M. P. Espinoza
M. P. Espinoza
ABOGADO
CALLE 14, NO. 1000

11
~~11~~

Casilla No. III.

SOLICITANTE(S) ADICIONAL(ES) Y/O INVENTOR(ES) (ADICIONAL(ES))

CITTA, Richard W.
739 Columbian
Oak Park, Illinois 60302
Estados Unidos de América

☒ Inventor solamente

☒ Los solicitantes y/o inventores (adicionales) se indican en una hoja de continuación.

Casilla No. IV.

AGENTE O REPRESENTANTE COMÚN; O DIRECCIÓN PARA CORRESPONDENCIA:

☒ Agente

Nombre y Dirección:

JOIKE, Trevor B.
MARSHALL, O'TOOLE, GERSTEIN, MURRAY & BORUN
6300 Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
Estados Unidos de América

TELÉFONO: 312/474-6399

FAX: 312/474-0448

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C ntinuación de la Casilla No. III

SOLICITANTE(S) ADICIONAL(ES) Y/O INVENTOR(ES) (ADICIONAL(ES))

NOMBRE Y DIRECCIÓN: FIMOFF, Mark
1020 Concord Lane
Hoffman Estates, Illinois 60195
Estados Unidos de América

☒ **Inventor solamente**

NOMBRE Y DIRECCIÓN: SNOPKO, Paul A.
360 E. Randolph Dr.
Chicago, Illinois 60601
Estados Unidos de América

☒ **Inventor solamente**

Casilla No. V. DESIGNACIÓN DE LOS ESTADOS

Se hacen las siguientes designaciones conforme a la Regla
4.9(a) (marcar las casillas aplicables)

Patente Regional

☒ **AP - Patente ARIPO:** GH Ghana, GM Gambia, KE Kenia, LS
Lesotho, MW Malawi, MZ Mozambique, SD Sudán, SL, Sierra
León, SZ Swazilandia, TZ República Unida de Tanzania, UG
Uganda, ZW Zimbabwe, y en cualquier otro estado que sea
un Estado Contratante del Protocolo de Harare y del PCT.

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☒ **EA - Patente Euroasia:** AM Armenia, AZ Azerbaiján, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD República de Moldova, RU Federación Rusa, TJ Tayikistán, TM Turkmenistán y cualquier otro estado que sea un Estado Contratante de la región de Euroasia.

☒ **EP - Patente Europea:** AT Australia, BE Bélgica, CH y LI Suiza y Liechtenstein, CY Ciprus, DE Alemania, DK Dinamarca, ES España, FI Finlandia, FR Francia, GB Reino Unido, GR Grecia, IE Irlanda, IT Italia, LU Luxemburgo, MC Mónaco, NL Holanda, PT Portugal, SE Suecia, y cualquier otro estado que sea un Estado Contratante de la Patente Europea y del PCT.

☒ **OA - Patente OAPI:** BF Burkina Faso, BJ Benin, CF República Central Africana, CG Congo, CI Côte d'Ivoire, CM Camerún, GA Gabón, GN Guinea, GW Guinea-Bissau, ML Malí, MR Mauritania, NE Nigeria, SN Senegal, TD Chad, TG Togo y cualquier otro Estado que sea un Estado miembro de la OAPI y un Estado Contratante del PCT (si se desea otro tipo de protección o tratamiento, especificar en la línea punteada).....

[Handwritten signature]

Patente Nacional (Si se desea cualquier otra clase de protección o de tratamiento, especificar en la línea punteada).....

☒ AE Emiratos Árabes Unidos	☒ LC Santa Lucía
☒ AG Antigua y Barbuda	☒ LK Sri Lanka
☒ AL Albania.....	☒ LR Liberia
☒ AM Armenia.....	☒ LS Lesotho
☒ AT Austria.....	☒ LT Lituania
☒ AU Australia.....	☒ LU Luxemburgo
☒ AZ Azerbaiján	☒ LV Latvia
☒ BA Bosnia y Herzegovina	☒ MA Marruecos.....
☒ BA Barbados	☒ MD República de Moldova.....
☒ BU Bulgaria.....	☒ MG Madagascar.....
☒ BR Brasil.....	☒ MK La Antigua República Yugoslava de Macedonia.....
☒ BY Belarus.....	☒ MN Mongolia
☒ BZ Belice	☒ MW Malawi
☒ CA Canadá	☒ MX México
☒ CH y LI Suiza y Liechtenstein	☒ MZ Mozambique
☒ CN China	☒ NO Noruega
☒ CR Costa Rica	☒ NZ Nueva Zelanda

☒ CU Cuba	☒ PL Polonia
☒ CZ República Checa.....	☒ PT Portugal
☒ DE Alemania	☒ RO Rumania
☒ DK Dinamarca	☒ RU Federación Rusa
☒ DM Dominica	☒ SD Sudan
☒ DZ Algeria	☒ SE Suecia
☒ EE Estonia	☒ SG Singapur
☒ ES España	☒ SI Eslovenia
☒ FI Finlandia	☒ SK Eslovaquia
☒ GB Reino Unido	☒ SL Sierra León
☒ GD Granada	☒ TJ Tayikistán
☒ GE Georgia	☒ TM Turkmenistán.....
☒ GH Ghana	☒ TR Turquía
☒ GM Gambia	☒ TT Trinidad y Tobago
☒ HR Croacia	☒ TZ República Unida de Tanzania
☒ HU Hungría	☒ UA Ucrania
☒ ID Indonesia	☒ UG Uganda
☒ IL Israel	☐ US Estados Unidos de América..
☒ IN India	☒ UZ Uzbekistán
☒ IS Islandia	☒ VN Vietnam

[Handwritten signature] 16

☒ JP Japón	☒ YU Yugoslavia
☒ KE Kenia	☒ ZA Sudáfrica
☒ KG Kyrgyzstan	☒ SW Zimbabwe.....
☒ KP República Popular Democrática de Corea ...	Marque las casillas reservadas para designar los Estados que han llegado a ser parte del PCT después de la emisión de esta hoja:
☒ KR República de Corea	
☒ KZ Kazakhstan	☒ CO Colombia

Declaración de Designación Precautelativa: Además de las designaciones arriba efectuadas, el solicitante también hace otras designaciones conforme a las Regla 4.9(b) que se permitirían conforme al PCT salvo por cualesquiera designaciones indicadas en la Casilla Suplementaria como excluidas del alcance de esta declaración. El solicitante declara que aquellas designaciones adicionales están sujetas a confirmación y que cualquier designación que no se confirme antes de la expiración de 15 meses contados a partir de la fecha de prioridad se ha de considerar como retirada por el solicitante a la expiración de ese límite de tiempo. *(La confirmación (incluidos los derechos) deben llegar a la Oficina receptora dentro del límite de tiempo de 15 meses).*

13 de marzo de 2001 No cedida Estados Unidos

(13-03-01)

 47

Casilla No. 6 REIVINDICACIÓN DE PRIORIDAD

Fecha de presentación de la solicitud anterior (día/mes/año)	Número de la solicitud anterior	País de la solicitud:
Item(1) 18 de abril de 2000 (18.04.00)	60/198.014	Estados Unidos
Item(2) 13 de diciembre de 2000 (13.12.00)	60/255.476	Estados Unidos
Item(e) 13 de diciembre de 2000 (13.12.00)	60/255.464	Estados Unidos

☒ La Oficina receptora debe preparar y transmitir a la Oficina Internacional una copia certificada de la(s) solicitud(es) anterior(es) arriba identificada(es) como ítem(s): 1, 2, 3 y 4

Casilla No. VII - AUTORIDAD DE BÚSQUEDA INTERNACIONAL: ISA/EP

Casilla No. VIII - LISTA DE LOS ÍTEMS QUE HACEN PARTE DE LA SOLICITUD E IDIOMA DE LA MISMA

Esta solicitud internacional contiene el siguiente número de hojas:

Solicitud: 5

Descripción (incluyendo la parte de la lista de secuencia): 45

Reivindicaciones: 6

 18

Resumen: 1

Dibujos: 12

Número total de hojas: 69

Esta solicitud internacional está acompañada de los ítems que se marcan a continuación:

1. ☒ hoja del cálculo de los derechos
3. ☒ copia del poder general;
9. ☒ otros (especificar): tarjeta postal

Idioma en que se presentó la solicitud internacional: Inglés

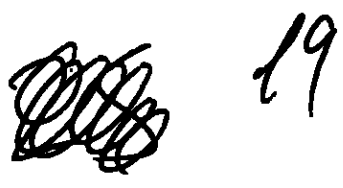
Por: (Fdo.) Trevor B. Joike

HOJA DEL CÁLCULO DE LOS DERECHOS

Referencia del Archivo del Solicitante o del Agente:

94417/37034

Solicitante: ZENITH ELECTRONICS CORPORATION



CÁLCULO DE LOS DERECHOS

1. Derecho de Traspaso..... US\$240.00 T
2. Derecho por la Búsqueda..... US\$846.00 S

La búsqueda internacional se llevará solamente por: EP

3. Derechos Internacionales

Derecho Básico

Esta solicitud internacional contiene 69 hojas.

Las primeras 30 hojas.....US4382.00 b1

39 x US\$9.00 =.....US\$351.00 b2

sume las casillas b1 y b2 y
registre el total en el B.....US\$733.00 B

Derechos de Designación

La Solicitud Internacional contiene 87 designaciones

$\frac{6}{\text{número de derechos de designación por pagar (máximo 6)}}$	x	$\frac{82.00}{\text{monto del derecho de designación}}$	= 492.00	D
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Sume los montos registrados en el B y en el D
y coloque el total en el I..... 1.225.00 I

4.
5. TOTAL DERECHOS POR PAGAR US\$2.311.00

MODALIDAD DE PAGO:

☒ Cheque

AUTORIZACIÓN PARA CONSIGNAR EN UNA CUENTA

El RO/ US

☒ (esta casilla se puede marcar solamente si las condiciones para las cuentas de depósitos de la Oficina receptora lo permiten). Por el presente autorizo cargar cualquier faltante o acreditar cualquier sobrepago del total de derechos arriba indicados a mi cuenta corriente.

☒ está autorizado a cargar a mi cuenta corriente el derecho correspondiente a la preparación y transmisión del documento de prioridad a la Oficina Internacional de la OMPI.

13-2855

27/03/01

Trevor B. Joike

Cuenta corriente No.

Fecha

Firmado

TRATADO DE COOPERACIÓN PARA PATENTES

Nombramiento General de Agente

El suscrito solicitante nombra a:

Trevor B. Joike
MARSHALL, O'TOOLE, GERSTEIN, MURRAY & BORUN
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
Estados Unidos de América
(312) 474-6300

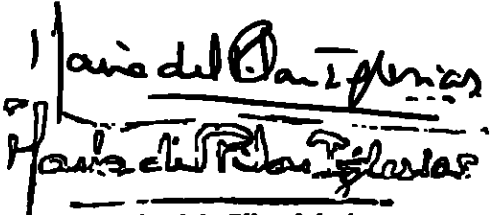
21

como agente para actuar en su nombre ante las Autoridades Internacionales competentes en relación con todas y cualesquiera solicitudes internacionales presentadas por él y de las cuales sea el único solicitante.

Fechado: 13 de octubre, 1997

Zenith Electronics Corporation
a Delaware corporation
1000 Milwaukee Avenue
Glenview, Illinois 60025
Estados Unidos de América

Por: (Fdo.) Richard F. Vitkus, Secretario.


María del Pilar Iglesias
C. C. 41.339.183 de Bogotá
intérprete Oficial según Resolución No. 815 de
15 de Abril de 1971 del Ministerio de Justicia

CLAIMS:

1. A method of providing enhanced slice prediction, the method being CHARACTERIZED by the following steps:

receiving an input containing symbols representing first data and symbols representing second data, wherein each of the symbols representing the first data correspond to a first number of data bits, wherein each of the symbols representing the second data correspond to a second number of data bits, wherein the first and second numbers of data bits are unequal, and wherein the first and second data have the same n level constellation;

decoding only the second data with a decoder; producing an output in response to the input and the decoder, wherein the output is confined to at least one but fewer than $n/2$ of the n constellation levels, and wherein $n > 2$; and,

providing the output as the enhanced slice prediction.

2. The method of claim 1 wherein the decoder is a first decoder, wherein the receiving step comprises the step of decoding the input with a second decoder to recover the first and second data, wherein the second decoder has n states; wherein the producing step comprises the step of choosing $n/4$ states out of $n/2$ states of the n states of the second decoder, and wherein

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the providing step comprises the step of providing the $n/4$ states as the enhanced slice prediction.

3. The method of claim 2 further comprising the step of delaying the choosing step based upon a processing time of the second decoder.

4. The method of claim 1 wherein the decoder is a first decoder, wherein the receiving step comprises the step of decoding the ^{extra}input with a second decoder to recover the first and second data, wherein the second decoder has n states, wherein the producing step comprises the step of choosing only one state out of $n/2$ states of the n states of the second decoder, and wherein the providing step comprises the step of providing the one state as the enhanced slice prediction.

5. The method of claim 4 further comprising the step of delaying the choosing step based upon a processing time of the second decoder.

6. The method of claims 1, 2, 3, 4, or 5 wherein n is eight.

7. The method of claim 1 wherein the producing step comprises the following steps:

decoding the input when the second data is not available so as to produce the output; and,

decoding the second data when the second data is available so as to produce the output.

8. The method of claim 7 further comprising the step of delaying the decoding of the input based at least in part upon a processing time of the decoder.

9. The method of claim 7 wherein the providing step comprises providing only one state as the enhanced slice prediction.

10. The method of claim 7 further comprising the step of selecting between decoding the input and the second data in response to a received map.

11. The method of claim 1 wherein the decoder is a first decoder, wherein the receiving step comprises the step of decoding the input with a second decoder to recover the first and second data, wherein the step of decoding only the second data comprises the step of decoding the second data with the first decoder to produce decoded second data, and wherein the producing step comprises the following steps:

producing the output by decoding the input with a third decoder when the decoded second data is not available; and,

producing the output by decoding the second decoded data with the third decoder when the decoded second data is available.

12. The method of claim 11 further comprising the step of delaying the step of decoding the input with the third decoder.

13. The method of claim 11 wherein the third decoder implements a Viterbi algorithm.

14. The method of claim 11 ^{en donde} wherein the ^{parte de} providing step ^{suministrando} comprises the step of providing only one state of the third decoder as the enhanced slice prediction.

15. The method of claim 11 further comprising the step of selecting between decoding the input and the decoded second data in response to a received map.

16. The method of claims 7 or 11 wherein the first data comprises eight level non-RVSB symbols, and wherein the second data comprises eight level RVSB symbols.

18. The method of claim 1, 7, or 11 wherein the providing step comprises the step of providing the enhanced slice prediction based upon a known ^{instrucción} training signal when a transmitted training signal is contained in a received signal.

18. The method of claim 1 further comprising the step of providing the enhanced slice prediction as feedback to an equalizer.

19. The method of claim 1 further comprising the step of providing the enhanced slice prediction as feedback to a phase tracker.

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TRADUCCIÓN OFICIAL No. 002-1013

Efectuada el día 7 de octubre del 2002, de un documento escrito en Inglés, al cual para su identificación se le estampa el sello de María del Pilar Iglesias, Traductora e Intérprete Oficial según consta en la Resolución No. 819 expedida por el Ministerio de Justicia el 15 de abril de 1971.

REIVINDICACIONES: (Predicción mejorada de secciones)

1. Un método para proporcionar predicción mejorada de secciones, el cual se CARACTERIZA por los siguientes pasos:

recibir un entrada que contiene símbolos que representan los primeros datos y símbolos que representan los segundos datos, en el cual cada uno de los símbolos que representa los primeros datos corresponden al primer número de bits de datos, en donde cada símbolo que representa los segundos datos corresponde al segundo número de bits de datos, siendo los primeros y los segundos números de bits de datos diferentes y en donde los primeros y los segundos datos tienen el mismo nivel n de constelación;

decodificar únicamente los segundos datos con otro decodificador;

M. P. Iglesias
María del Pilar Iglesias
TRADUCTORA E
INTÉRPRETE OFICIAL
Resolución No. 819 del 15 de Abril de 1971

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producir una salida en respuesta a la entrada y al decodificador, en donde la salida se confina a al menos uno pero menos de $n/2$ de los niveles de constelación n y en donde $n > 2$; y

proporcionar la salida como la predicción mejorada de secciones.

2. El método de la reivindicación 1 en donde el decodificador es un primer decodificador, y en donde el paso de recepción comprende el paso de decodificar la entrada con un segundo decodificador para recuperar los primeros y los segundos datos, en donde el segundo decodificador tiene n estados y el paso de producción comprende el paso de elegir $n/4$ estados de $n/2$ estados de los n estados del segundo decodificador y en donde el paso de suministro proporciona $n/4$ estados como una predicción mejorada de secciones.

3. El método de la reivindicación 1 que comprende además el paso de demorar el paso de elección con base en un tiempo de procesamiento del segundo decodificador.

4. El método de la reivindicación 2 en donde el decodificador es un primer decodificador y en donde el paso receptor comprende el paso de decodificar la entrada con un

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segundo decodificador para recuperar los primeros y los segundos datos y en donde el segundo decodificador tienen n estados y el paso de producción incluye el paso de elegir únicamente un estado entre $n/2$ estados de los n estados del segundo decodificador y en donde el paso de suministro comprende el paso de proporcionar un estado como una predicción mejorada de secciones.

5. El método de la reivindicación 4 que comprende además el paso de demorar el paso de elección con base en un tiempo de procesamiento del segundo decodificador.

6. El método de las reivindicaciones 1, 2, 3, 4 o 5 en donde n es ocho.

7. El método de la reivindicación 1 en el cual el paso de producción comprende los siguientes pasos:

decodificar la entrada cuando los segundos datos no están disponibles como para producir la salida; y,

decodificar los segundos datos cuando estos están disponibles como para producir la salida.

8. El método de la reivindicación 7 que comprende además el paso de demorar la decodificación de la entrada con

base al menos en parte en un tiempo de procesamiento del decodificador.

9. El método de la reivindicación 7 en donde el paso de suministro comprende el suministro de únicamente un estado, tal como la predicción mejorada de secciones.

10. El método de la reivindicación 7 que comprende además el paso de seleccionar entre decodificar la entrada y los segundos datos en respuesta a un mapa recibido.

11. El método de la reivindicación 1 en donde el decodificador es un primer decodificador, en donde el paso receptor comprende el paso de decodificar la entrada con un segundo decodificador para recuperar los primeros y los segundos datos y en donde el paso de decodificar únicamente los segundos datos incluye el paso de decodificar los segundos datos con el primer decodificador para producir segundos datos decodificados y en donde el paso de producción comprende los siguientes pasos:

producir la salida mediante la decodificación de la entrada con un tercer decodificador cuando los segundos datos decodificados no estén disponibles; y

producir la salida mediante la decodificación de los segundos datos decodificados con un tercer decodificador cuando los segundos datos decodificados están disponibles.

12. El método de la reivindicación 11 que comprende además el paso de demorar el paso de decodificar la entrada con el tercer decodificador.

13. El método de la reivindicación 11 en donde el tercer decodificador implementa un algoritmo Viterbi.

14. El método de la reivindicación 11 en donde el paso de suministro comprende el paso de suministrar únicamente un estado del tercer decodificador, tal como la predicción mejorada de secciones.

15. El método de la reivindicación 11 que comprende además el paso de seleccionar entre decodificar la entrada y los segundos datos decodificados en respuesta a un mapa recibido.

16. El método de las reivindicaciones 7 u 11 en donde los primeros datos comprenden símbolos no-RVSB de ocho niveles y en donde los segundos datos incluyen símbolos de RVSB de ocho niveles.

17. El método de las reivindicaciones 1, 7 u 11 en donde el paso de suministro incluye el paso de suministrar la predicción mejorada de secciones con base en una señal de instrucción conocida cuando una señal de instrucción transmitida está contenida en una señal recibida.

18. El método de la reivindicación 1 que comprende además el paso de suministrar la predicción mejorada de secciones como retroalimentación para un ecualizador.

19. El método de la reivindicación 1 que comprende además el paso de suministrar la predicción mejorada de secciones como retroalimentación a un rastreador de fase.

Es traducción fiel y completa efectuada por:

María del Pilar Iglesias
C.C. 41.339.183 de Bogotá

María del Pilar Iglesias
C.C. 41.339.183 de Bogotá
según Resolución No. 673 del
13 de mayo de 1971 del Ministerio de Justicia

CARDENAS & CARDENAS



ABOGADOS

PROPIEDAD INTELECTUAL LTDA.

CARRERA 7a N° 71-52 - Torre B - Piso 9
TELEFONOS (571) 312 36 00 - 312 23 69 - 312 23 79
general@cardenasycardenas.com - Fax: (571) 312 24 10 - 312 24 20
BOGOTA, D.C. - COLOMBIA

Bogotá, D.C.
Septiembre 17 de 2002

Señores
TRADUCCIONES TÉCNICAS
Atn. Sergio Andrés Rueda
L.C.

URGENTE VENCIMIENTO

Corresponsal: SCHIFF, HARDIN & WAITE
Cilente: ZENITH ELECTRONICS CORPROATION.
Marca: Patente U5011/09734 "Enhanced F P01.0519-CO"

Estimado Sergio:

De acuerdo a nuestra conversación del día de hoy acompaño los (14) documentos en referencia, para proceder con la traducción y recoger el día 7 de octubre.

Atentamente,


IVONN OSPINA

PD. Para las facturas correspondiente por favor tener en cuenta el membrete de la carta para la elaboración, si es para Cárdenas Y Cárdenas Abogados Ltda. o Cárdenas & Cárdenas Propiedad Intelectual. Incluir el número de traducción a la factura , el idioma al cual se traduce, especificar el documento que se esta traduciendo.

MIT : 800176087-2

RECIBO OFICIAL DE CAJA : 02 - 67,397
FECHA : OCTUBRE 8 DE 2002

SUPERINTENDENCIA Y COMERCIO
Radicacion : 02091936 00000000 Folios: 304
Fecha (AND): 2002-10-11 15:07:13
Tramite : 011 PCT-PATENT 378 FASE NACI 411 PRESENTAC
Dependencia: 2020 DIVISION DE NUEVAS CREACIONES

***** CONSIGNACION *****

DEPOSITANTE	TIPO PAGO	BANCO	CUENTA	No. PAGO	FECHA PAGO	Vr. PAGO
ARDEMAS Y CARDENAS P.I. CONSIGNACION		BANCO POPULAR	050-00110-6	3163918	08/10/2002	2,931,000.00

***** CONCEPTO *****

CANT. CONTABILITICO	CONCEPTO	TOTAL CONCEPTO
1 50005-01-01 SOLICITUDES	1 TRAMITES DE SOL. DE PATENTE DE IN	378,000.00
	TOTAL :	378,000.00

MON: OCHOCIENTOS SETENTA Y OCHO MIL PESOS

RESPONSABLE : _____

RECIBO DE CAJA APLICADO AL EXPEDIENTE No. _____

Carrera 13 No. 27-00 Pisos 5, 7 y 10
Conmutador 382 0840
Fax 350 5220
E-mail: info@sic.gov.co
www.sic.gov.co
Bogotá, D.C., Colombia

ENHANCED SLICE PREDICTION FEEDBACK

^{Substantives}
Related Applications

This application ^{revises} claims the benefit of U.S. Provisional Application No. 60/198,014, filed April 18, 2000, U.S. Provisional Application No. 60/255,476, filed December 13, 2000, and U.S. Provisional Application No. 60/255,464, filed December 13, 2000.

Technical Field of the Invention

The present invention relates to the transmission and/or reception of digital data.

Background of the Invention

The ^{ATSC} standard in the United States for the transmission of digital television signals is known as 8 VSB data (ATSC Digital Television Standard ^{ATSC Digital TV Standard} A/53). This 8 VSB data has a constellation consisting of eight possible symbol levels. In a VSB system, the eight possible symbol levels are all in the same phase. In a QAM system, however, the symbols are transmitted in phase ^{in quadrature} quadrature relationship.

The standard referred to above specifies the formatting and modulation of digital video and audio data. The transmitted data is in the form of symbols with each symbol representing two bits of data that are ^{can video subframes} ~~trellis~~ encoded into three bits of trellis encoded data. Each three bits of trellis encoded data are mapped into a symbol having a corresponding one of eight levels. Reed/Solomon encoding and interleaving are also provided to increase the ^{robustness} robustness of the transmitted information.

Auxiliary data (data other than digital video or audio data) are also permitted to be transmitted in a digital television channel. These data are formatted and modulated according to the standard in the same manner as video and audio data. Receivers made in accordance with the 8 VSB standard are able to read packet identifications (PIDs) which allow the receivers to differentiate between audio, video, and auxiliary data.

However, while the robustness of the transmitted digital television signals is sufficient for digital television reception, this robustness

may not be sufficient for the transmission of auxiliary data, particularly where the auxiliary data are critical. Accordingly, one of the applications of the present invention is the transmission of auxiliary data in a VSB format with outer encoding for added robustness. The auxiliary data transmitted in accordance with the application of the present invention are referred to herein as robust VSB data (RVSB).

Summary of the Invention

In one aspect of the present invention, a method for providing enhanced slice prediction comprises the following: receiving an input containing first and second data, wherein the first and second data have different bit rates and are defined by the same n level constellation; decoding only the second data with a decoder; producing an output in response to the input and the decoder, wherein the output is confined to at least one but fewer than $n/2$ of the n constellation levels, and wherein $n > 2$; and, providing the output as the enhanced slice prediction.



Attorney Docket
7174D

5 In another aspect of the present inven-
tion, an apparatus for providing enhanced slice
prediction comprises an inner decoder, an outer
decoder, and an enhanced slice predictor. The inner
decoder inner decodes a received signal to provide
an inner decoded output. The inner decoder produces
n/2 possible decoding states based upon the received
signal, and the received signal contains data having
n levels, wherein $n > 2$. The outer decoder outer
10 decodes the inner decoded output. The enhanced
slice predictor chooses at least one but fewer than
the n/2 of the n/2 possible decoding states based
upon an output of the outer decoder and provides the
chosen state or states as the enhanced slice
15 prediction.

In yet another aspect of the present
invention, an apparatus for providing enhanced slice
prediction comprises an inner decoder, an outer
decoder, and an enhanced slice predictor. The inner
20 decoder inner decodes a received signal containing
first and second data to provide inner decoded first
and second data. The outer decoder outer decodes
only the second data. The enhanced slice predictor



provides a prediction output based upon the first data when the second data is not available and based upon the outer decoded second data when the second data is available.

5 Brief Description of the Drawing

These and other features and advantages will become more apparent from a detailed consideration of the invention when taken in conjunction with the drawing in which:

10 Figure 1 shows a robust VSB transmitter for transmitting robust VSB data and ATSC data in accordance with the present invention;

15 Figure 2 shows a standard ATSC receiver for receiving the ATSC data transmitted by the robust VSB transmitter of Figure 1;

Figure 3 shows a robust VSB receiver for receiving the robust VSB data transmitted by the robust VSB transmitter of Figure 1;

20 Figure 4 shows the 2/3 rate encoder of Figure 1 in additional detail;

Figure 5 shows the mapping function performed by the mapper of Figure 4;

Figure 6 shows the operation of the 2/3 rate decoders of Figures 2 and 3;

Figure 7 shows another robust VSB transmitter for transmitting robust VSB data and ATSC data in accordance with the present invention;

Figure 8 shows a standard ATSC receiver for receiving the ATSC data transmitted by the robust VSB transmitter of Figure 7;

Figure 9 shows a robust VSB receiver for receiving the robust VSB data transmitted by the robust VSB transmitter of Figure 7;

Figure 10 shows a circuit for generating the appropriate control signal on the discard control line of Figure 9;

Figure 11 shows yet another robust VSB transmitter for transmitting robust VSB data and ATSC data in accordance with the present invention;

Figure 12 shows an example of four data segments containing 1/2 rate outer coded data that may be transmitted by a robust VSB transmitter according to the present invention;

Figure 13 shows an example of four data segments containing 1/4 rate outer coded data that

may be transmitted by a robust VSB transmitter according to the present invention;

Figure 14 shows an example of four data segments containing 3/4 rate outer coded data that may be transmitted by a robust VSB transmitter according to the present invention;

Figure 15 shows the interleavers (I_r) of Figures 1, 9, and 11 in more detail;

Figure 16 shows the deinterleavers (D_r) of Figures 3 and 9 in more detail;

Figure 17 shows a map definition structure of a first robust VSB data packet of a frame;

Figure 18 shows a portion of the frame sync segment of a frame that carries a map indicating where in the frame robust VSB data can be found;

Figure 19 illustrates an enhanced slice predictor according to one embodiment of the present invention;

Figure 20 shows the trellis for the inner decoder of Figure 19;

Figure 21 shows possible state transitions for the outer decoder of Figure 19; and,



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Figure 22 illustrates an enhanced slice predictor according to another embodiment of the present invention.

Detailed Description

5 RVSB and ATSC Data Transmission and Reception

Figure 1 shows a robust VSB transmitter 10 that transmits both ATSC data and robust VSB data in accordance with one embodiment of the present invention. Figure 2 shows a standard ATSC receiver 10
10 12 that receives the ATSC data transmitted by the robust VSB transmitter 10, and Figure 3 shows a robust VSB receiver 14 that receives the robust VSB data transmitted by the robust VSB transmitter 10.

The robust VSB transmitter 10 includes a
15 Reed/Solomon encoder 16 that encodes uncoded auxiliary data bytes by adding Reed/Solomon parity bytes to the uncoded auxiliary data bytes. The uncoded auxiliary data bytes and the Reed/Solomon parity bytes are interleaved by an interleaver 18.
20 Then, the interleaved uncoded auxiliary data bytes and the Reed/Solomon parity bytes are bitwise encoded by an outer coder 20 using either a



convolutional code or other error correcting code.

5 The outer coder 20 improves the robustness of the
uncoded auxiliary data bytes and the Reed/Solomon
parity bytes, converting them to robust data bytes
(hereinafter referred to as robust VSB data bytes)
and Reed/Solomon parity bytes.

10 The outer coder 20, for example, may be a
1/2 rate coder which produces two output bits for
every input bit, a 1/4 rate coder which produces
four output bits for every input bit, or a 3/4 rate
coder which produces four output bits for every
three input bits. Other coders could instead be
used.

15 At the output of the outer coder 20, a
three byte transport (tx) header is added to each
group of 184 coded robust VSB data and Reed/Solomon
bytes to form robust VSB data packets. A
multiplexer 24 multiplexes these robust VSB data
packets with ATSC data packets (typically, video and
20 audio) each comprising a three byte transport header
and 184 bytes of ATSC data. Either input to the
multiplexer 24 may be selected on a packet by packet
basis and each selected input is supplied to an ATSC

transmitter 26. The selection by the multiplexer 24 of which input to pass to the ATSC transmitter 26 is based on a robust VSB map to be described hereinafter.

5 The ATSC transmitter 26, as is typical, includes a Reed/Solomon encoder 28, an interleaver 30, and a 2/3 rate inner encoder 32 all operating in accordance with the ATSC standard.

10 A standard ATSC receiver, such as the standard ATSC receiver 12 shown in Figure 2, receives and processes the ATSC data and discards the robust VSB data. Accordingly, the standard ATSC receiver 12 includes a 2/3 rate inner decoder 34, a deinterleaver 36, and a Reed/Solomon decoder 38, all
15 operating in accordance with the ATSC standard. The standard ATSC receiver 12, however, is programmed to decode both the ATSC data and the robust VSB data transport headers (which include the packet identifications or PID's and which have not been
20 coded by the outer coder 20). The standard ATSC receiver 12 reads the PID's of all packets and, at 40, discards those packets having the PID's of robust VSB data. The standard ATSC receiver 12 also



includes a slice predictor 42 (such as the slice predictor disclosed in U.S. Patent No. 5,923,711) which is responsive to the inner decoded data and which provides an output back to a phase tracker and/or equalizer, as is known in the art.

The robust VSB data packets can be received, decoded, and processed by a robust VSB receiver such as the robust VSB receiver 14 shown in Figure 3. As is known, and as shown in Figure 4, the 2/3 rate inner encoder 32 of the ATSC transmitter 26 includes a precoder 44 and a four state trellis encoder 46. In combination, the precoder 44 and the four state trellis encoder 46 may be viewed as an eight state coder that produces three trellis encoded output bits (Z0 Z1 Z2) for every two input bits (X1 X2). A mapper 48 maps the three trellis encoded output bits to a symbol having one of eight levels as shown in Figure 5. As is well known from convolutional code theory, the operation of the precoder 44 and the four state trellis encoder 46 may be viewed as an eight state 4-ary trellis.



Therefore, in the robust VSB receiver 14,
a 2/3 rate inner decoder 50 may operate on an eight
state 4-ary trellis which views the precoder 44 and
the four state trellis encoder 46 of the 2/3 rate
inner encoder 32 in combination as shown in Figure 6
to produce a soft output decision (using, for
example, the SSA algorithm as described in "Optimum
Soft Output Detection for Channels with Intersymbol
Interference," Li, Vucetic, and Sato, IEEE
Transactions on Information Theory, May, 1995).

This soft decision making operation is more
complicated than the widely used Viterbi algorithm,
which produces a hard decision output, but the soft
decision making operation more fully takes advantage
of the coding gain provided by the outer coder 20.

The output of the 2/3 rate inner decoder
50 is deinterleaved by a deinterleaver 52. The
robust VSB receiver 14 reads the PID's of all
packets at the output of the deinterleaver 52.
Based upon these PID's, the robust VSB receiver 14
discards those packets at 54 which have the PID's of
ATSC data and also discards the transport headers
added following the outer coder 20 and the parity

bytes added by the Reed/Solomon encoder 28. Thus,
the robust VSB receiver 14, at 54, passes only the
robust VSB data packets containing the robust VSB
data coded by the outer coder 20. The robust VSB
5 data packets are decoded by an outer decoder 56,
deinterleaved by a deinterleaver 58 (which is the
inverse of the interleaver 18), and Reed/Solomon
decoded by a Reed/Solomon decoder 60 in order to
reconstruct the original uncoded auxiliary data
10 supplied to the Reed/Solomon encoder 16 of Figure 1.

The reliable output of the outer decoder
56 (either soft or hard output may be used) is
interleaved by an interleaver 62 (corresponding to
the interleaver 30) in a feedback path 64 in order
15 to restore the ordering of the outer decoded data to
the order of the data in the channel. This
interleaved outer decoded data can be used, for
example, by a slice predictor 66 to create reliable
feedback to a phase tracker and/or equalizer.

20 However, the overall feedback delay introduced by
the deinterleaver 52 and the interleaver 62 in the
robust VSB receiver 14 is generally too long to

provide useful feedback to the phase tracker and/or equalizer.

The arrangement shown in Figures 7, 8, and 9 avoids the feedback delay introduced by the deinterleaver 52 and the interleaver 62 of the robust VSB receiver 14. Figure 7 shows a robust VSB transmitter 80 in which uncoded auxiliary data bytes are encoded by a Reed/Solomon encoder 82 which adds Reed/Solomon parity bytes to the uncoded auxiliary data bytes. The uncoded auxiliary data bytes and the Reed/Solomon parity bytes are interleaved by an interleaver 84. Then, the interleaved uncoded auxiliary data bytes and Reed/Solomon parity bytes are bitwise encoded by an outer coder 86 using either a convolutional code or a turbo product code, as discussed above. The bitwise output of the outer coder 86 is small block interleaved by a small block interleaver 88 in order to reduce the impact of channel burst errors on the outer decoding. The data provided by the small block interleaver 88 may be referred to as Rdata(n.o.) which stands for normally ordered robust VSB data.

One input of a first multiplexer 92 receives ATSC formatted packets each comprising (i) a valid three byte transport header with a PID number for robust VSB data, (ii) 184 placeholder bytes of dummy robust VSB data, and (iii) twenty placeholder bytes for dummy ATSC Reed/Solomon parity data. The other input of the first multiplexer 92 receives ATSC formatted dummy packets each comprising 207 bytes of dummy ATSC data. These ATSC formatted dummy packets serve as placeholders for the real ATSC packets to be added downstream. The inputs of the first multiplexer 92 may be selected on a packet by packet basis, and this selection is based on the robust VSB map to be described later.

The selected output of the first multiplexer 92 is interleaved by an interleaver 94 according to the ATSC Standard for the convolutional byte interleave. A data replacer 96 receives both the output of the interleaver 94 and the output of the small block interleaver 88. The data replacer 96 replaces each dummy robust VSB data placeholder byte from the interleaver 94 with the next normally

ordered robust VSB data byte from the small block interleaver 88.

5 The output of the data replacer 96 contains normally ordered robust VSB data with interspersed transport headers, dummy ATSC Reed/Solomon parity bytes, and dummy ATSC data packet bytes. A deinterleaver 98, which operates according to the ATSC Standard for byte deinterleaving, deinterleaves the output of the data
10 replacer 96 to thus effectively "repacketize" the data as packets of transport headers, reordered robust VSB data (Rdata(r.o.)), dummy ATSC Reed/Solomon parity bytes, and dummy ATSC data. The reordering of the normally reordered robust VSB data
15 results from the deinterleaving of the deinterleaver 98 and the reordered data may be referred to as reordered robust VSB data.

20 The dummy ATSC Reed/Solomon parity bytes (20 per packet) of the robust VSB packets and the dummy ATSC data packets (207 bytes per packet) are discarded at 100. The remaining robust VSB packets, each including a transport header and reordered robust VSB data, are multiplexed by a second



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5 multiplexer 102 with real ATSC data packets each
containing 187 bytes of a transport header and ATSC
data. Either input to the second multiplexer 102
may be selected on a packet by packet basis and is
supplied to an ATSC transmitter 104. The selection
by the second multiplexer 102 of which input to pass
to the ATSC transmitter 104 is based on the robust
VSB map to be described hereinafter.

10 The ATSC transmitter 104 typically
includes a Reed/Solomon encoder 106, an interleaver
108, and a twelve way 2/3 rate inner encoder 110 all
operating in accordance with the ATSC standard. The
Reed/Solomon encoder 106 outputs packets of
transport headers, reordered robust VSB data, and
15 ATSC Reed/Solomon parity bytes multiplexed with
packets of transport headers, ATSC data, and ATSC
Reed/Solomon parity bytes. The ATSC Reed/Solomon
parity bytes for the robust VSB data are calculated
based on the reordered robust VSB data. Moreover,
20 the interleaver 108 changes the ordering of the
robust VSB data so that the robust VSB data at the
output of the interleaver 108 is again normally
ordered robust VSB data. Also, the interleaver 108

5 disperses the transport headers, the ATSC
Reed/Solomon parity bytes, and the ATSC data. This
data is 2/3 rate coded by the twelve way 2/3 rate
inner encoder 110 and is transmitted. The
transmitted robust VSB data is in normal order,
i.e., the order provided at the output of the small
block interleaver 88. This normal order permits the
robust VSB receiver to avoid the delay caused by the
deinterleaver 52 and the interleaver 62 of the
robust VSB receiver 14.

10 As shown in Figure 8, a standard ATSC
receiver 120 includes a twelve way 2/3 inner decoder
122 which decodes the transmitted data to provide an
output data stream comprising normally ordered
robust data with interspersed transport headers,
ATSC data, and ATSC Reed/Solomon parity bytes
located according to the ATSC convolutional byte
interleave provided by the interleaver 108. An ATSC
deinterleaver 124 restores the transport headers,
ATSC data, and ATSC Reed/Solomon parity bytes to
their transport "packetized" positions. Also, the
ATSC deinterleaver 124 converts the normally ordered
robust VSB data into reordered robust VSB data.



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This reordered form permits an ATSC Reed/Solomon decoder 126 of the standard ATSC receiver 120 to correctly test parity for the robust VSB data packets. The standard ATSC receiver 120 can then read the robust VSB data packet transport headers and gracefully discard the robust VSB data packets at 128 based on their PIDs.

As shown in Figure 9, a robust VSB receiver 130 includes a soft output twelve way 2/3 rate inner decoder 132. (A hard output 2/3 decoder would result in a considerable loss of coding gain). The output of the soft output twelve way 2/3 rate inner decoder 132 comprises normally ordered robust VSB data, with reordered ATSC data, transport headers, and ATSC Reed/Solomon parity symbols dispersed within the robust VSB data at locations indicated by a discard control line 134 discussed below. A discard block 136, under control of the discard control line 134, discards the reordered ATSC data, transport headers, and ATSC Reed/Solomon parity symbols.

A small block deinterleaver 138 deinterleaves the robust VSB data. The small block

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deinterleaver 138 has a relatively low delay time. This deinterleaving disperses possible burst errors in the robust VSB data at the output of the soft output twelve way 2/3 rate inner decoder 132. The normally ordered robust VSB data is bitwise decoded by an outer decoder 140 which also packs the robust VSB data into bytes. The amp information telling the outer decoder 140 what decoding rate to use on what data is provided to the outer decoder 140 at an R_{mp} Data input. Neither the deinterleaver 52 nor the interleaver 62 is needed in the robust VSB receiver 130 allowing for lower overall feedback delay to the phase tracker and/or equalizer. The outer decoded data can be used, for example, by an enhanced slice predictor 142 to generate feedback to the phase tracker and/or equalizer. If desired, the feedback may be gated, or the step size of the equalizer gradient algorithm adjusted proportionally to the reliability of the decoded data.

The robust VSB data packet payload decoded by the outer decoder 140 is deinterleaved by a deinterleaver 144 (which is the inverse of the interleaver 84) and is Reed/Solomon decoded by a



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Reed/Solomon decoder 146 (corresponding to the Reed/Solomon encoder 82) in order to reconstruct the original uncoded auxiliary data supplied to the Reed/Solomon encoder 82 of Figure 7.

5 As provided in the ATSC standard, a frame comprises a plurality of segments each containing a predetermined number of bytes. The first segment of a frame is a frame sync segment, and the remaining segments in the frame are data segments. Although
10 robust VSB data can be transmitted in segments or in partial segments, it is convenient to transmit robust VSB data in segment pairs. The robust VSB map discussed above indicates which segment pairs contain robust VSB data so that the discard block
15 136 can correctly discard the reordered ATSC data before the reordered ATSC data can get to the outer decoder 140. The transport headers and the ATSC Reed/Solomon parity data for all segments (robust VSB and ATSC) must also be discarded by the discard
20 block 136.

A conceptually simple circuit to generate the appropriate control signal on the discard control line 134 to control this discarding function



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is shown in Figure 10, together with the relevant portion of the robust VSB receiver 130. The robust VSB receiver 130 uses received map information (the method for transmission and reception of this map information is described below) to instruct a dummy segment generator 150 when to construct dummy 207 byte segments. The dummy segment generator 150 also uses the frame sync signal. For each ATSC dummy segment, the dummy segment generator 150 sets all bytes to FF. For each robust VSB data dummy segment, the dummy segment generator 150 sets the transport header and ATSC Reed/Solomon parity bytes to FF. The dummy segment generator 150 sets the rest of the bytes of each robust VSB data dummy segment to 00.

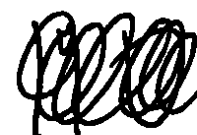
These dummy segments are fed by the dummy segment generator 150 to an ATSC convolutional byte interleaver 152 whose output is then used to control the discard block 136 which then responds to the FF and 00 codes to correctly discard the reordered ATSC data, the transport headers, and the ATSC Reed/Solomon parity data which are interleaved



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within the received data stream. The discard block 136, thus, passes only the robust VSB data.

Figure 11 shows a multiple outer code robust VSB transmitter 160. The robust VSB transmitter 160 operates similarly to the robust VSB transmitter 80 of Figure 7. The robust VSB transmitter 160 has a first Reed/Solomon encoder 162 which encodes first uncoded auxiliary data by adding Reed/Solomon parity bytes to the first uncoded auxiliary data, a second Reed/Solomon encoder 164 which encodes second uncoded auxiliary data by adding Reed/Solomon parity bytes to the second uncoded auxiliary data, and a third Reed/Solomon encoder 166 which encodes third uncoded auxiliary data bytes by adding Reed/Solomon parity bytes to the third uncoded auxiliary data. The Reed/Solomon encoded first uncoded auxiliary data are interleaved by a first interleaver 168, the Reed/Solomon encoded second uncoded auxiliary data are interleaved by a second interleaver 170, and the Reed/Solomon encoded third uncoded auxiliary data are interleaved by a third interleaver 172. Then, the interleaved Reed/Solomon encoded first uncoded auxiliary data



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are bitwise encoded by a first outer coder 174, the interleaved Reed/Solomon encoded second uncoded auxiliary data are bitwise encoded by a second outer coder 176, and the interleaved Reed/Solomon encoded third uncoded auxiliary data are bitwise encoded by a third outer coder 178. The bitwise output of the first outer coder 174 is interleaved by a first small block interleaver 180, the bitwise output of the second outer coder 176 is interleaved by a second small block interleaver 182, and the bitwise output of the third outer coder 178 is interleaved by a third small block interleaver 184.

The first outer coder 174 is a 1/4 rate coder, the second outer coder 176 is a 1/2 rate coder, and the third outer coder 178 is a 3/4 rate coder, although any other combination of these or other outer coders using different coding rates could be used. The data outputs of the first, second, and third small block interleavers 180, 182, and 184 are selected by a multiplexer 186 under control of a select input which determines the order in which the differently outer coded data are inserted into the frame to be transmitted. The data



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at the output of the multiplexer 186 may be referred to as Rdata(n.o.) which, as before, stands for normally ordered robust VSB data.

5 The top three inputs of a multiplexer 190 receive ATSC format packets each having of a valid three byte transport header with a PID number for robust VSB data, 184 placeholder bytes of dummy robust VSB data, and twenty dummy placeholder bytes for ATSC Reed/Solomon parity data. The robust VSB
10 data at the topmost input of the multiplexer 190 correspond to 1/4 rate coded data from the first outer coder 174, the robust VSB data at the next input of the multiplexer 190 correspond to 1/2 rate coded data from the second outer coder 176, and the
15 robust VSB data at the next input of the multiplexer 190 correspond to 3/4 rate coded data from the third outer coder 178. The data supplied to the bottommost input of the multiplexer 190 comprises ATSC format dummy packets each having 207 bytes of
20 dummy ATSC data. These dummy ATSC data packets serve as placeholders for the real ATSC data packets to be added downstream of the multiplexer 190. The inputs to the multiplexer 190 may be selected on a

packet by packet basis in accordance with the input on a select line. This selection is based on the robust VSB data map to be described below.

5 The output of the multiplexer 190 is interleaved by an interleaver 192 in order to achieve a correct ATSC convolutional interleave. A data replacer 194 receives both the output of the interleaver 192 and the output of the multiplexer 186. The data replacer 194 replaces each dummy
10 robust VSB data placeholder byte from the multiplexer 190 with the next corresponding normally ordered robust VSB data byte from the multiplexer 186.

15 The output of the data replacer 194 contains normally ordered robust VSB data (which is 1/4 rate coded, 1/2 rate coded, and/or 3/4 rate coded, as appropriate) with interspersed transport headers, dummy ATSC Reed/Solomon parity bytes, and dummy ATSC data packet bytes. A convolutional byte
20 deinterleaver 196 (as described in the ATSC Standard) deinterleaves the output of the data replacer 194 to thus effectively "repacketize" the data as packets of transport headers, reordered

robust VSB data (1/4, 1/2, and/or 3/4 rate coded),
dummy ATSC Reed/Solomon parity bytes, and dummy
packets of ATSC data. The reordering of the
normally ordered robust VSB data results from the
deinterleaving of the deinterleaver 196.

The dummy ATSC Reed/Solomon parity bytes
(20 per packet) and the dummy ATSC data packets (207
bytes per packet) are discarded at 198 in a manner
similar to that provided by the discard control line
134 and the discard block 136 of Figure 9. The
remaining robust VSB packets, each including a
transport header and reordered robust VSB data, are
multiplexed by a multiplexer 200 with real ATSC data
packets each containing 187 bytes of a transport
header and ATSC data. Either input to the
multiplexer 200 may be selected on a packet by
packet basis and is supplied to an ATSC transmitter
202. The selection by the multiplexer 200 of which
input to pass to the ATSC transmitter 202 is based
on the robust VSB map to be described hereinafter.

The ATSC transmitter 202 typically
includes a Reed/Solomon encoder 204, an interleaver
206, and a twelve way 2/3 rate inner encoder 208 all

operating in accordance with the ATSC standard. The Reed/Solomon encoder 204 outputs packets of transport headers, reordered robust VSB data, and ATSC Reed/Solomon parity bytes multiplexed with packets of transport headers, ATSC data, and ATSC Reed/Solomon parity bytes. The ATSC Reed/Solomon parity bytes for the robust VSB data are calculated based on the reordered robust VSB data. Moreover, the interleaver 206 changes the ordering of the robust VSB data so that the robust VSB data at the output of the interleaver 206 are again normally ordered robust VSB data. Also, the interleaver 206 disperses the transport header bytes, the ATSC Reed/Solomon parity bytes, and the ATSC data. These data are 2/3 rate coded by the twelve way 2/3 rate inner encoder 208 and are transmitted. The transmitted robust VSB data are in normal order, i.e., the order provided at the output of the multiplexer 186. This normal data order permits the robust VSB receiver to avoid the delay caused by the deinterleaver 52 and the interleaver 62.

As discussed above, an ATSC frame comprises a frame sync segment and a plurality of

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data segments and, for convenience, robust VSB data are packed into groups of four segments. More specifically, Figure 12 shows an example of four data segments that may be used in a frame to transmit robust VSB data that is 1/2 rate coded, Figure 13 shows an example of four data segments that may be used in a frame to transmit robust VSB data that is 1/4 rate coded, and Figure 14 shows an example of four data segments that may be used in a frame to transmit robust VSB data that is 3/4 rate coded. These examples represent the frame prior to the interleaver 108 and assume that each group of four robust VSB data segments contains an integral number of robust Reed/Solomon encoded blocks each of which is 184 bytes long, of which twenty bytes are parity bytes.

For the case of a 1/2 rate outer code, Figure 12 shows that the outer coder outputs two bits for each input bit. A robust VSB data packet is packed as one RVSB Reed-Solomon block to a pair of data segments (one bit per symbol) so that, for a 1/2 rate outer code, four segments contain two robust Reed/Solomon encoded blocks. As shown in

Figure 13, for the case of a 1/4 rate outer code,
the outer coder outputs four bits for each input
bit. Robust VSB data is packed as one RVSB Reed-
Solomon block for every four data segments (1/2 bit
per symbol) so that, for a 1/4 rate outer code, four
segments contain one robust Reed/Solomon encoded
block. As shown in Figure 14, for the case of a 3/4
rate outer code, the outer coder outputs four bits
for each three input bits. In this case,
transmitted symbol and byte boundaries do not always
match. However, three complete RVSB Reed-Solomon
blocks will pack exactly into four data segments
(1.5 bits per symbol) so that, for a 3/4 rate outer
code, four segments contain three robust
Reed/Solomon encoded blocks.

Accordingly, Figures 12, 13, and 14 can be
represented by the following table:

S	X	Y
1/2	1	2
1/4	1	4
3/4	3	4

where X represents the number of complete robust Reed/Solomon encoded blocks and Y represents the number of frame segments required to contain the corresponding number X of robust Reed/Solomon encoded blocks.

However, it should be understood that other coding rates can be used in conjunction with the present invention and, therefore, the above table will change depending upon the particular coding rates that are used.

The interleavers 18, 84, 168, 170, and 172 are shown in more detail in Figure 15, and the deinterleavers 58 and 144 are shown in more detail in Figure 16, assuming that a robust Reed/Solomon encoded block is chosen to be 184 bytes long. The interleavers 18, 84, 168, 170, and 172 are $B = 46$, $M = 4$, $N = 184$ convolutional interleavers that byte wise interleave the robust VSB data. This interleaving scheme is the same as the ATSC interleave scheme described in the ATSC Digital Television Standard A/53 and the Guide to the Use of the ATSC digital Television Standard A/54, except that the B parameter for the robust interleaver is

46 instead of 52 and the parameter N is 184 instead of 208. This interleaver is needed so that a robust VSB receiver can cope with long bursts of noise on the channel even though the ATSC deinterleaver (D_A) is bypassed as shown in Figure 9.

As shown in Figure 16, the deinterleavers 58 and 144 are $B = 46$, $M = 4$, $N = 184$ convolutional deinterleavers that byte wise deinterleave the robust VSB data. This deinterleaving scheme is also the same as the ATSC deinterleaver scheme described in the ATSC Digital Television Standard A/53 and the Guide to the Use of the ATSC digital Television Standard A/54, except that the B parameter for the robust deinterleaver is 46 instead of 52 and the parameter N is 184 instead of 208.

Because a robust VSB Reed/Solomon block comprises 184 bytes, and because an integral number of robust VSB Reed/Solomon blocks are in a data frame, the number of robust VSB data bytes plus robust VSB Reed/Solomon parity bytes in a data frame is always evenly divisible by 46. Therefore, the frame sync segment can be used as a synchronizer for the deinterleavers 58 and 144 (D_r) in the receiver,

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regardless of the value of G (to be described
below). At frame sync, the deinterleaver
commutators are forced to the top positions. The
deinterleavers 58 and 144 are byte wise
deinterleavers.

Data Mapping

As discussed above, each data frame may
contain a mix of robust VSB data segments and ATSC
(non-robustly coded) data segments. Moreover, the
robust VSB data may contain data coded with a mix of
coding rates. The robust VSB receiver 14 or 130
must have a robust VSB map that indicates which
segments are robust VSB coded and which outer code
is used for the robust VSB coding so that the robust
VSB receiver 14 or 130 can correctly process the
robust VSB data and discard the ATSC data. The
robust VSB transmitters 10, 80, and 160 also use the
robust VSB map to control their corresponding
multiplexing and discard functions. This robust VSB
map is transmitted by the robust VSB transmitter 10,
80, or 160 to the robust VSB receiver 14 or 130



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along with all the other data in a manner described below.

The presence, amount, and location of the robust VSB data in a data frame encoded with a particular outer code are indicated by one or more numbers S_c that appear as two level data in the frame sync segment of the data frame. As is known, the frame sync segment is the first segment in a frame. So, for the outer codes described above (1/4 rate, 1/2 rate, and 3/4 rate), the frame sync segment should preferably contain $[S_{1/4} S_{1/2} S_{3/4}]$. Each S_c (such as $S_{1/4}$ or $S_{1/2}$ or $S_{3/4}$) is encoded as eighteen symbols (bits) of two level data. For all three codes, a total of $3 \times 18 = 54$ symbols are needed as a definition of the robust VSB map. These symbols are inserted into the reserved area near the end of each frame sync segment (just before the twelve precoding bits). For each group of eighteen bits ($b_{18} \dots b_1$), the last six bits ($b_6 \dots b_1$) represent the number G of groups of eight segments (8 segments = 2, 4 or 6 robust VSB data packets depending on the outer code) mapped as robust VSB data in the current frame. The twelve preceding

5

bits are for comb filter compensation (see the Guide to the Use of the ATSC digital Television Standard A/54). Accordingly, as shown in Figure 18, bits b_6 . . . b_1 represent the number G , bits b_{18} . . . b_{13} are the complement of bits b_6 . . . b_1 , and bits b_{12} . . . b_7 can be alternating +1 and -1 (or any other pattern).

10

Let it be assumed that $S = S_{1/4} + S_{1/2} + S_{3/4}$. Because $312/8 = 39$, 0-39 groups of eight segments can be mapped as robust VSB data or 8 VSB data (ATSC data). Therefore, each S_c may have a value of 0 . . . 39, as long as their sum S is ≤ 39 .

15

The robust VSB data segments are preferably distributed as uniformly as possible over the data frame. For example, if $S = 1$, then the following eight segments are mapped as robust VSB data segments and all other segments are mapped as ATSC data segments: 1, 40, 79, 118, 157, 196, 235, and 274. If $S = 2$, then the following sixteen

20

segments are mapped as robust VSB data segments and all other segments are mapped as ATSC data segments: 1, 20, 39, 58, 77, 96, 115, 134, 153, 172, 191, 210, 229, 248, 267, and 286. These examples continue

until $S = 39$, where the whole data frame is mapped as robust VSB data segments. For some values of S , the spacing between robust VSB data segment pairs is not perfectly uniform. However, for any value of S , the spacing is fixed in advanced and, therefore, known to all receivers.

If a frame contains robust VSB data provided by three outer coders operating at $1/4$ rate, $1/2$ rate, and $3/4$ rate, then the data from these three outer coders may be divided in a frame such that, as to RVSB segments, the first $8 \times S_{1/4}$ segments contain the $1/4$ rate outer coded data, the next $8 \times S_{1/2}$ segments contain the $1/2$ rate outer coded data, and the last $8 \times S_{3/4}$ segments contain the $3/4$ rate outer coded data. However, other robust VSB data segment organizations are possible for these three outer coders or for any number of other types of outer coders.

Because this robust VSB map is contained in the frame sync segment, as discussed above, the robust VSB map does not enjoy the same level of coding gain as the robust VSB data. However, the robust VSB map may still be reliably acquired by a

robust VSB receiver by correlating the robust VSB map over some number of frames. Therefore, the robust VSB map should not change too often (for example, not more often than every ~60 frames).

5 The above mapping method allows a receiver to reliably and simply acquire the robust VSB map by correlation. Once a receiver has acquired the map, it is desirable for the receiver to instantly and reliably track changes in the map. In order to

10 instantly and reliably track changes in the map, the definition in the robust VSB map for each outer code, excluding the comb compensation bits, is duplicated in the first robust VSB Reed/Solomon encoded block of the frame. In addition, there is

15 data indicating (i) when in the future the map will change and (ii) the future new map definition. The first robust VSB data packet of a frame for an outer coder, therefore, has the structure shown in Figure 17, where the robust VSB map definition data is

20 given by the following: eight bits designating the current map (only six of these bits are used); eight bits designating the number of frames until the map changes (1-125; if 0, then no change

5 coming); and, eight bits designating the next map
(again, only six of these bits are used). The
remaining portion of the first robust VSB data
packet is data. The first RVSB segment in a frame
for a respective outer coder has the arrangement
shown Figure 17.

10 In this way, a receiver can track map
changes using reliable robust VSB data. Even if a
burst error destroys a number of the frames, the
receiver can keep its own frame countdown using the
number of frames read from a previously received
frame.' If the receiver finds at any time that the
definition for an outer code previously acquired by
the frame sync correlation does not match the
15 definition for that outer code in the first robust
VSB data segment, the receiver should restart its
map acquisition process.

RVSB Enhanced Slice Prediction and Equalizer
Feedback

20 ATSC 8 VSB receivers make important use of
adaptive equalization and phase tracking as
explained in the ATSC Digital Television Standard



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A/53 published by the Advanced Television Systems Committee, in the Guide to the Use of the ATSC Digital Television Standard A/54, also published by the Advanced Television Systems Committee. RVSB as
5 described above has features that allow for improvements in adaptive equalization and phase tracking.

One such improvement results from feeding back delayed reliable estimates of the input symbol
10 level to the adaptive equalizer and/or phase tracker based on a sequence estimation from an enhanced Viterbi Algorithm. (See "The Viterbi Algorithm," G. D. Forney, Jr., Proc. IEEE, vol 61, pp. 268-278, March, 1973). This type of feedback avoids the need
15 for "re-encoding," which has a state initialization problem.

U.S. Patent No. 5,923,711, entitled "Slice Predictor for a Signal Receiver," discloses an ATSC
8 VSB receiver which utilizes a slice predictor in
20 order to provide more reliable feedback to the phase tracker or adaptive equalizer. This feedback can be made even more reliable by a enhanced slice predictor system 300 shown in Figure 19. The

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enhanced slice predictor system 300 has an inner decoder 302 and an outer decoder 304 which operate similarly to the inner decoders and outer decoders described above.

5 The slice prediction output from the inner decoder 302 works in a manner similar to that described in the aforementioned U.S. Patent No. 5,923,711. As explained above, the inner decoder 302 is based on an 8 state 4-ary trellis that includes a precoder. Based on the best path metric at the current time t , the slice predictor of the inner decoder 302 decides a most likely state at time t . Then, based on the next possible pair of states, four possible predicted input levels (out of eight) for the next symbol at time $t + 1$ are selected. For example, as shown by the inner decoder trellis in Figure 20, if the most likely state at time t is state one, the next state is $\epsilon\{1$
10 5 2 6}. Therefore, the next input level at time $t + 1$ may be -7, +1, -3, or +5. These next input levels correspond to decoded bit pairs 00, 10, 01, and 11, respectively.

15

20

Similarly, the outer decoder 304 also finds the best path metric for the current time t for the respective trellis. A portion of this trellis is shown in Figure 21 for an exemplary outer decoder and may be applied generally to all three outer codes. As shown in Figure 21, two possible outer decoder input bit pairs are selected for the time $t + 1$ based on the next possible pair of states. By way of example, the two possible outer decoder input bit pairs may be 11 or 01. The bit pair chosen by the outer decoder 304 is sent to a prediction enhancer 306 which selects amplitude levels +5 or -3 from the set of four levels previously selected by the slice predictor of the inner decoder 302 as the enhanced slice prediction for time $t + 1$. Because the slice prediction of the inner decoder 302 is near zero delay, but because the outer decoder 304 cannot operate on the same symbol until after the inner decoder 302 has provided a decoded soft output, a delay module 308 provides a delay time slightly greater than the traceback delay time of the inner decoder 302. The slice prediction provided by the prediction enhancer

306 may be supplied as feedback to an equalizer of phase tracker 310.

5 With some additional delay time, the outer decoder 304 can make a final hard decision and select a single most likely input bit pair for time $t + 1$. For example, if 11 is found to be the most likely input bit pair to the outer decoder 304 as determined by its Viterbi Algorithm, this information is sent by the outer decoder 304 to the prediction enhancer 306 which then chooses +5 from the set of four levels and corresponding bit pairs already selected by the slice predictor of the inner decoder 302. The outer code can be a convolutional code or other type of error correction code. The predictor enhancer 306 is disabled during the periods of time when ATSC data is being received.

15 A feedback enhanced maximum likelihood sequence estimator (MLSE) slice predictor system 320 uses the Viterbi Algorithm and is shown in Figure 22 along with other relevant parts of an RVSB receiver. The feedback enhanced MLSE slice predictor system 320 has an inner decoder 322 and an outer decoder 324 which operate similarly to the inner decoder 302



5

and the outer decoder 304 described above. However, instead of using the slice prediction output of the inner decoder 302, an enhanced MLSE module 326 is configured to execute the usual Viterbi Algorithm on the received signal by operating the eight state 2/3 rate code trellis (the same trellis used by the inner decoder 322, including the precoder).

10

The enhanced MLSE module 326 selects as its next input either (i) the noisy eight level received signal as delayed by a delay module 328 if the next input is a non-RVSB symbol or (ii) the bit pair decision output of the outer decoder 324 (hard or soft) if the next input is a RVSB symbol. The enhanced MLSE module 326 makes this selection according to the symbol by symbol information in the RVSB map.

15

20

The enhanced MLSE module 326 outputs one of eight possible symbols as its slice prediction, and this slice prediction (symbol decision) is provided by the enhanced MLSE module 326 as feedback to an equalizer or phase tracker 330.

The enhanced MLSE module 326 should follow a more correct path through the eight state trellis



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than does the inner decoder 322 because the enhanced MLSE module 326 gets more reliable input from the outer decoder 324 when an RVSB symbol is available.

5 The output of the enhanced MLSE module 326 may be a hard slice decision or a soft level. Also, any symbol reliability indication from the inner decoder 322 or the outer decoder 324 may be used to change the step size of the equalizer LMS algorithm. (See the Guide to the Use of the ATSC Digital
10 Television Standard A/54.)

An optional predetermined coded training sequence may be included in a specified portion of the first RVSB segment of a data field. This sequence is known in advance by both the transmitter and receiver. During the time the decoded training
15 sequence is output from the outer decoder 324, the input to the enhanced MLSE module 326 is switched to a stored version of the decoded training sequence.

Certain modifications of the present
20 invention have been discussed above. Other modifications will occur to those practicing in the art of the present invention. For example, although the standard ATSC receiver 12 and the robust VSB

receiver 14 are shown above as separate receivers,
the functions of the standard ATSC receiver 12 and
the robust VSB receiver 14 can be combined in two
data paths of a single receiver capable of decoding
both types of data (ATSC data and robust VSB data).

Accordingly, the description of the
present invention is to be construed as illustrative
only and is for the purpose of teaching those
skilled in the art the best mode of carrying out the
invention. The details may be varied substantially
without departing from the spirit of the invention,
and the exclusive use of all modifications which are
within the scope of the appended claims is reserved.

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CLAIMS:

2 1. A method of providing enhanced slice
3 prediction, the method being CHARACTERIZED by the
4 following steps:
5 receiving an input containing first and
6 second data, wherein the first and second data have
7 the same n level constellation and different bit
8 rates;
9 decoding only the second data with a
10 decoder;
11 producing an output in response to the
12 input and the decoder, wherein the output is
13 confined to at least one but fewer than $n/2$ of the n
14 constellation levels, and wherein $n > 2$; and,
15 providing the output as the enhanced slice
16 prediction.

1 2. The method of claim 1 wherein the
2 decoder is a first decoder, wherein the receiving
3 step comprises the step of decoding the input with a
4 second decoder to recover the first and second data,
5 wherein the second decoder has n states, wherein the

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6 producing step comprises the step of choosing $n/4$
7 states out of $n/2$ states of the n states of the
8 second decoder, and wherein the providing step
9 comprises the step of providing the $n/4$ states as
10 the enhanced slice prediction.

1 3. The method of claim 2 further
2 comprising the step of delaying the choosing step
3 based upon a processing time of the second decoder.

1 4. The method of claim 1 wherein the
2 decoder is a first decoder, wherein the receiving
3 step comprises the step of decoding the input with a
4 second decoder to recover the first and second data,
5 wherein the second decoder has n states, wherein the
6 producing step comprises the step of choosing only
7 one state out of $n/2$ states of the n states of the
8 second decoder, and wherein the providing step
9 comprises the step of providing the one state as the
10 enhanced slice prediction.

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1 5. The method of claim 4 further
2 comprising the step of delaying the choosing step
3 based upon a processing time of the second decoder.

1 6. The method of claims 1, 2, 3, 4, or 5
2 wherein n is eight.

1 7. The method of claim 1 wherein the
2 producing step comprises the following steps:
3 decoding the input when the second data is
4 not available so as to produce the output; and,
5 decoding the second data when the second
6 data is available so as to produce the output.

1 8. The method of claim 7 further
2 comprising the step of delaying the decoding of the
3 input based at least in part upon a processing time
4 of the decoder.

1 9. The method of claim 7 wherein the
2 providing step comprises providing only one state as
3 the enhanced slice prediction.

1 10. The method of claim 7 further
2 comprising the step of selecting between decoding
3 the input and the second data in response to a
4 received map.

1 11. The method of claim 1 wherein the
2 decoder is a first decoder, wherein the receiving
3 step comprises the step of decoding the input with a
4 second decoder to recover the first and second data,
5 wherein the step of decoding only the second data
6 comprises the step of decoding the second data with
7 the first decoder to produce decoded second data,
8 and wherein the producing step comprises the
9 following steps:
10 producing the output by decoding the input
11 with a third decoder when the decoded second data is
12 not available; and,
13 producing the output by decoding the
14 second decoded data with the third decoder when the
15 decoded second data is available.

1 12. The method of claim 11 further
2 comprising the step of delaying the step of decoding
3 the input with the third decoder.

1 13. The method of claim 11 wherein the
2 third decoder implements a Viterbi algorithm.

1 14. The method of claim 11 wherein the
2 providing step comprises the step of providing only
3 one state of the third decoder as the enhanced slice
4 prediction.

1 15. The method of claim 11 further
2 comprising the step of selecting between decoding
3 the input and the decoded second data in response to
4 a received map.

1 16. The method of claims 7 or 11 wherein
2 the first data comprises eight level non-RVSB
3 symbols, and wherein the second data comprises eight
4 level RVSB symbols.

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1 18. The method of claim 1, 7, or 11
2 wherein the providing step comprises the step of
3 providing the enhanced slice prediction based upon a
4 known training signal when a transmitted training
5 signal is contained in a received signal.

1 18. The method of claim 1 further
2 comprising the step of providing the enhanced slice
3 prediction as feedback to an equalizer.

1 19. The method of claim 1 further
2 comprising the step of providing the enhanced slice
3 prediction as feedback to a phase tracker.

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4 Abstract of the Disclosure

5 Enhanced slice prediction is based upon
6 ATSC 8 VSB data when robust 8 VSB data are not
7 available and is based upon robust 8 VSB data when
8 robust 8 VSB data are available.

RVSB Transmitter (initial concept)

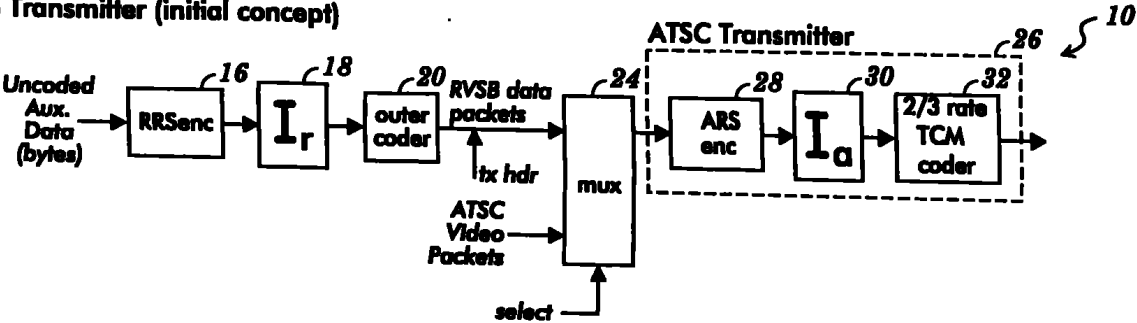


Figure 1

ATSC Receiver

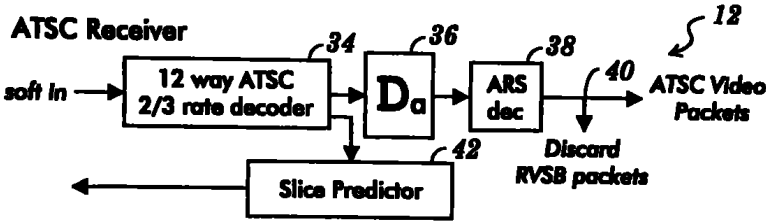


Figure 2

mapper function			
Z2	Z1	Z0	level
0	0	0	-7
0	0	1	-5
0	1	0	-3
0	1	1	-1
1	0	0	+1
1	0	1	+3
1	1	0	+5
1	1	1	+7

Figure 5

RVSB Receiver

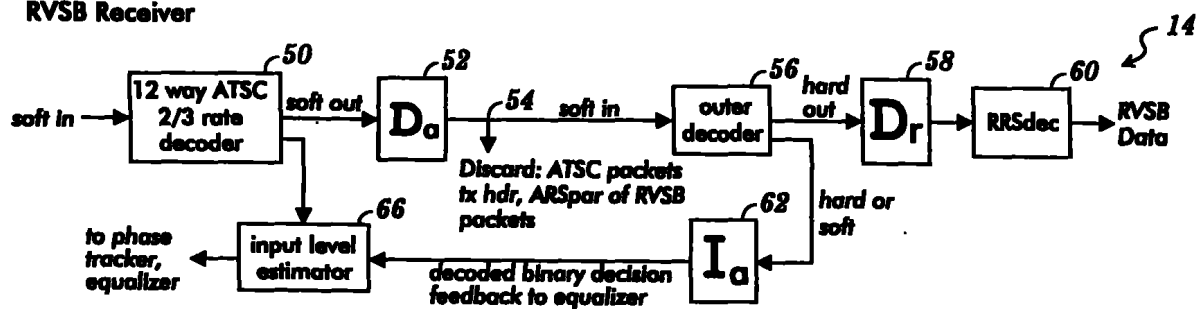


Figure 3

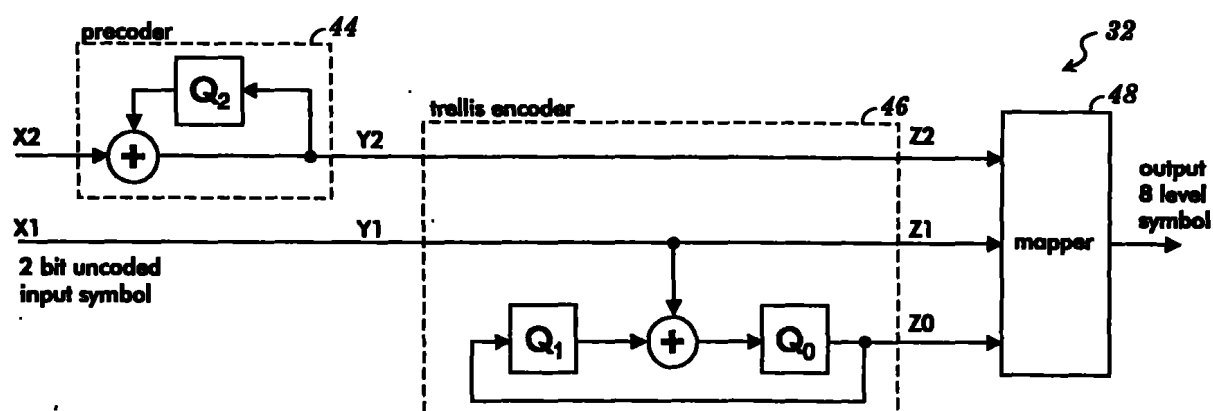


Figure 4

branch label :
 $X_2 X_1$ / mapped output level

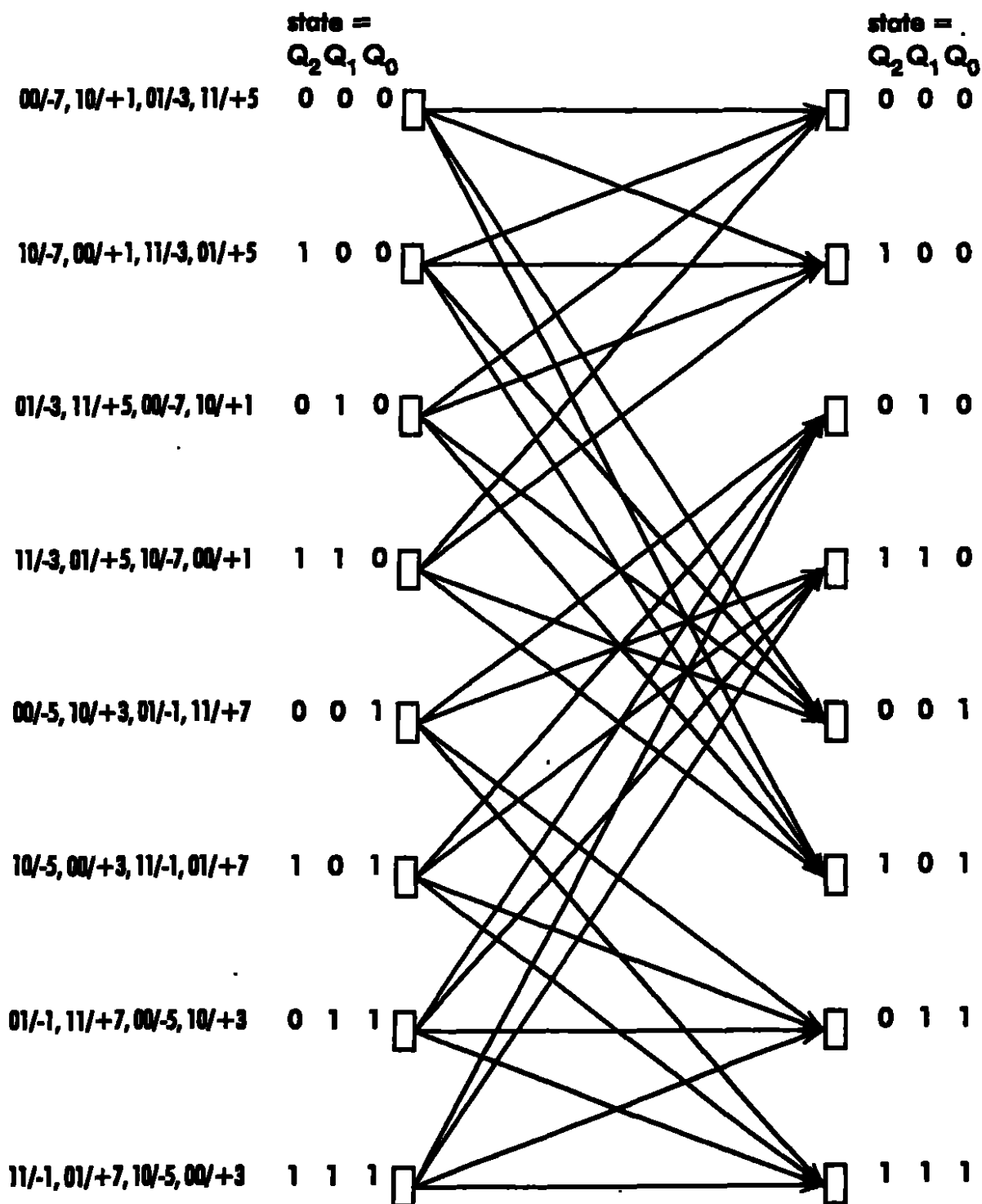


Figure 6

RVSb Transmitter

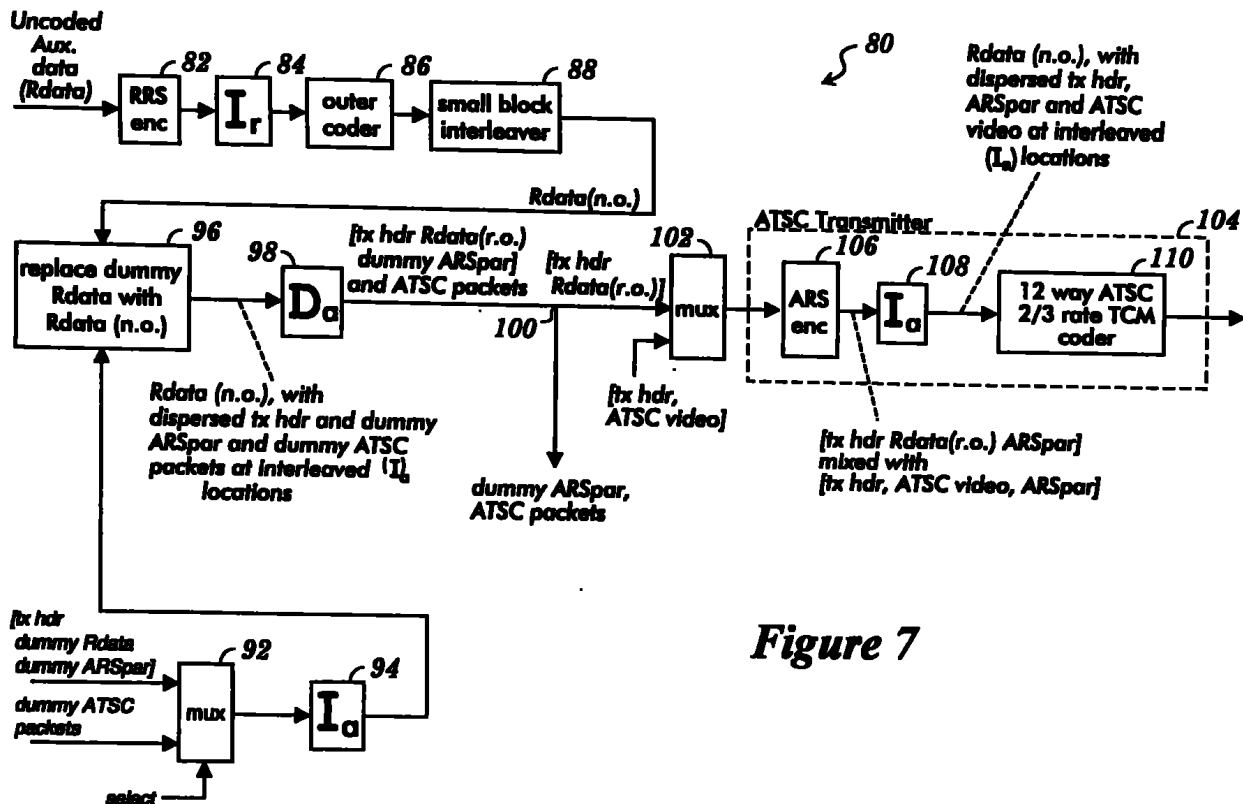
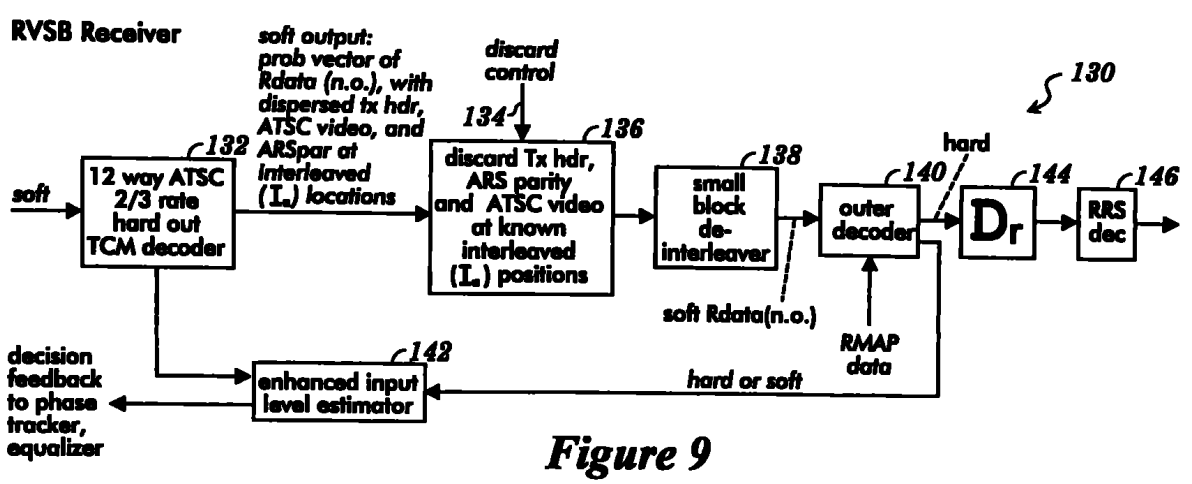
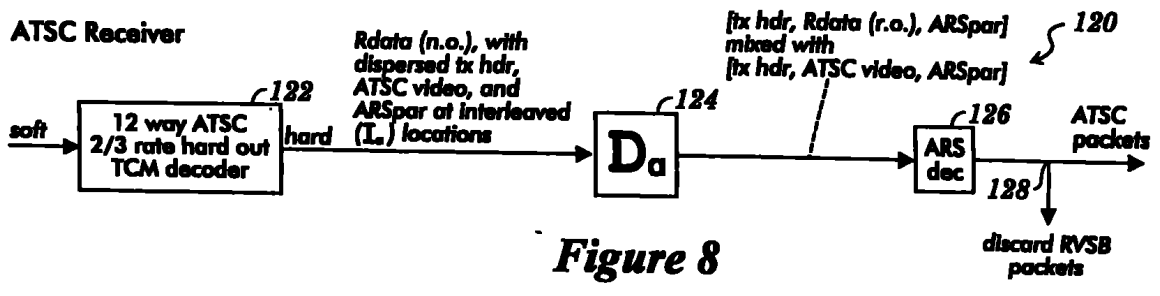


Figure 7

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RVSB Receiver

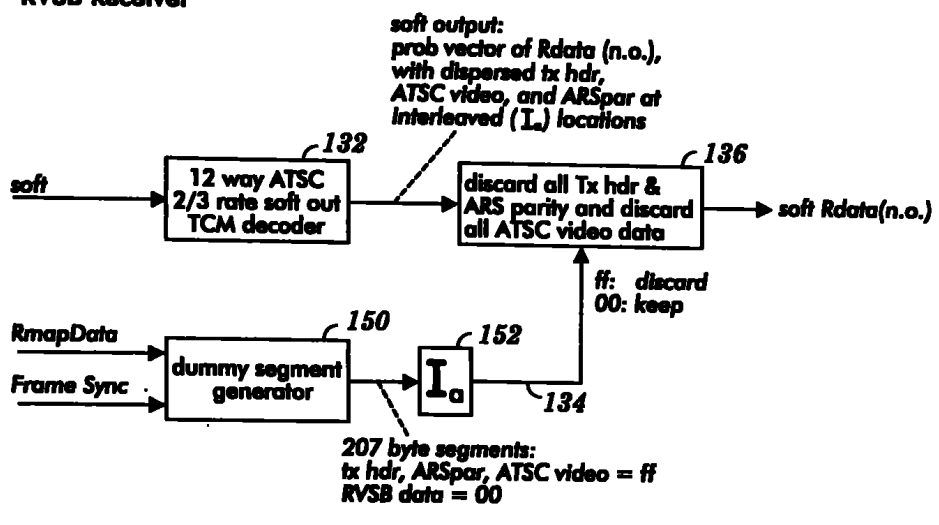


Figure 10

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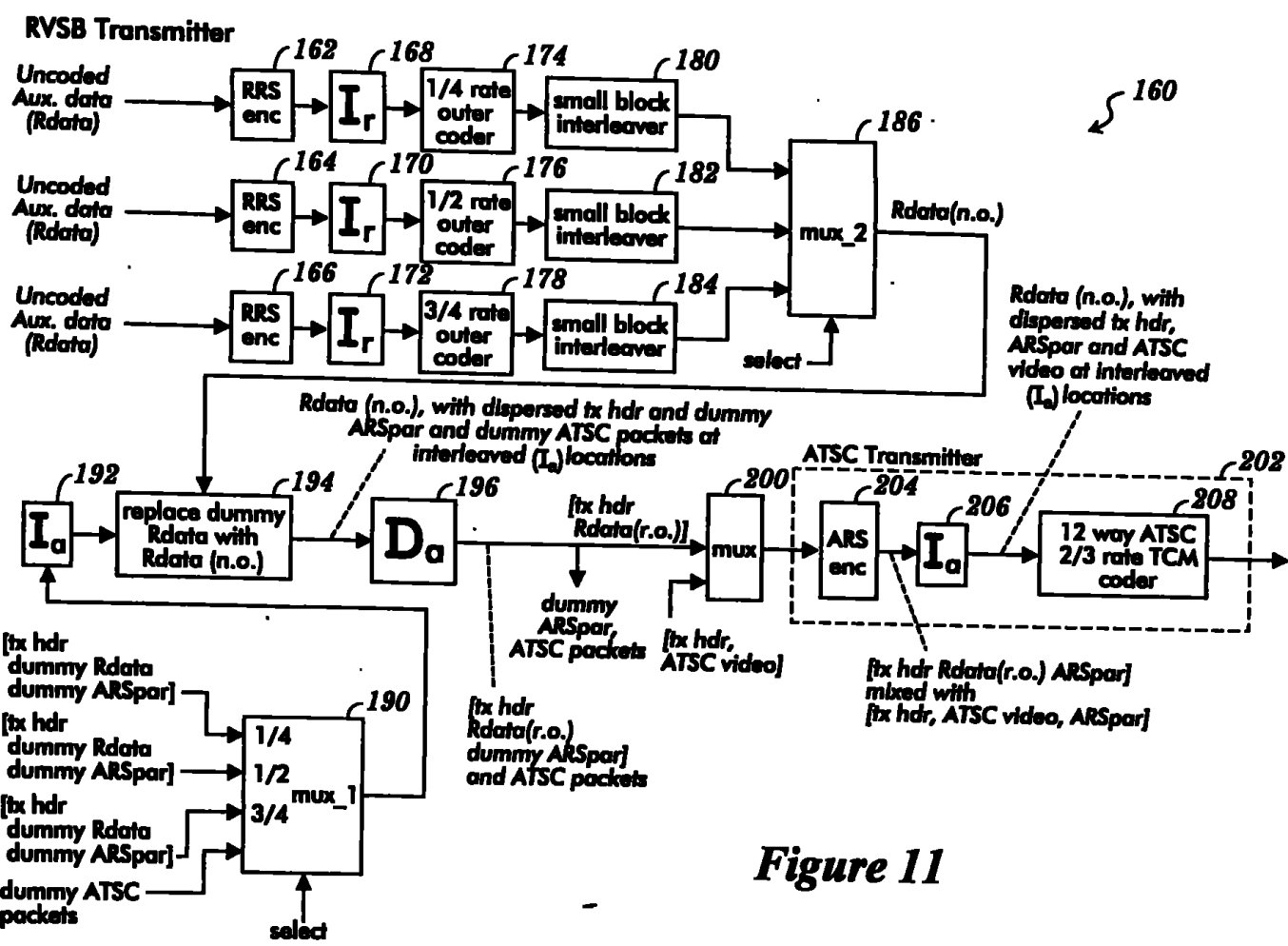


Figure 11

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for 1/2 rate outer code

ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 92 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (576 symbols) 72 bytes payload	RRS parity (160 symbols) 20 bytes	ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 92 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (576 symbols) 72 bytes payload	RRS parity (160 symbols) 20 bytes	ARS parity (80 symbols)
2 bits/symbol		1 bit/symbol	2 bits/symbol

Figure 12

for 1/4 rate outer code

ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 46 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 46 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 46 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (416 symbols) 26 bytes payload	RRS parity (320 symbols) 20 bytes	ARS parity (80 symbols)
2 bits/symbol		0.5 bit/symbol	2 bits/symbol

Figure 13

for 3/4 rate outer code

ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 138 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 26 bytes payload	20 bytes RRS parity 92 bytes payload	ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 72 bytes payload	20 bytes RRS parity 46 bytes payload	ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 118 bytes payload	20 bytes RRS parity	ARS parity (80 symbols)
2 bits/symbol		1.5 bit/symbol	2 bits/symbol

Figure 14

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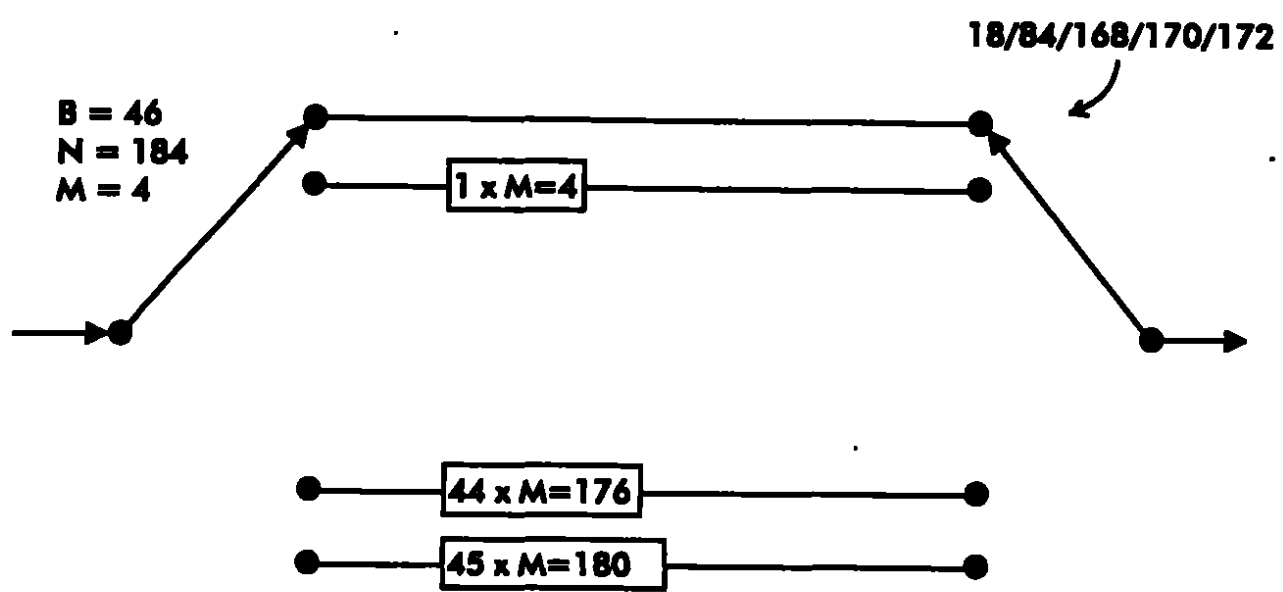


Figure 15

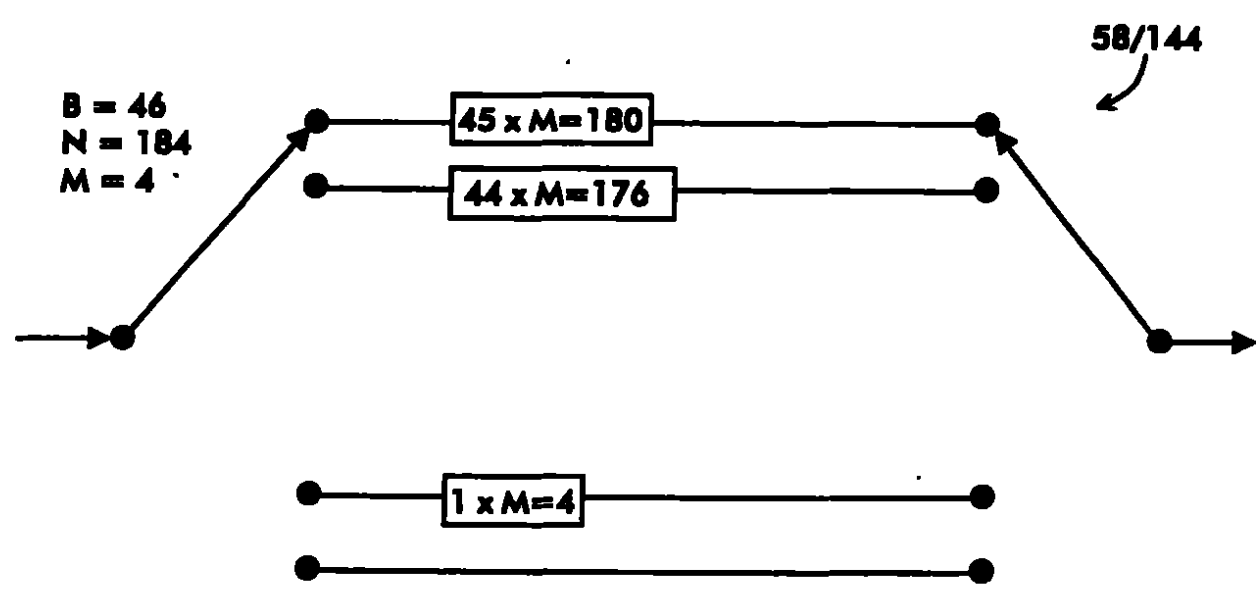


Figure 16

First RVSB RS block of field

RVSB map data (24 bits)	1288 bits
-------------------------	-----------

Figure 17

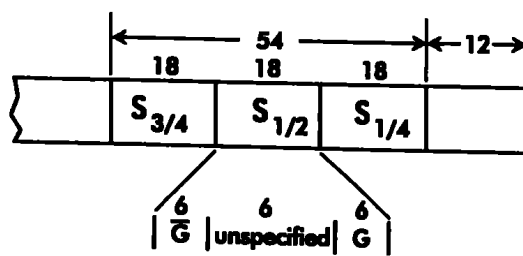


Figure 18

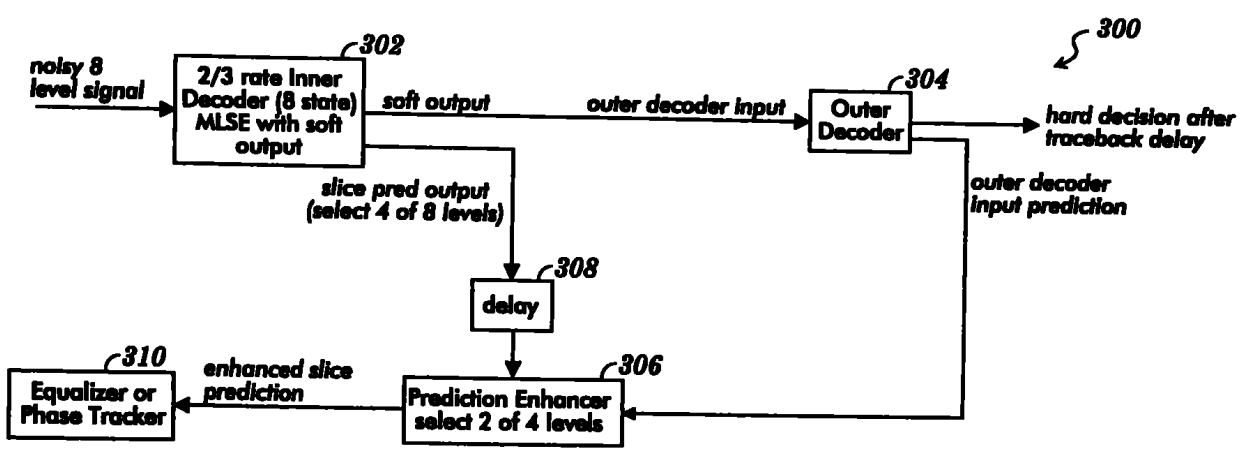


Figure 19

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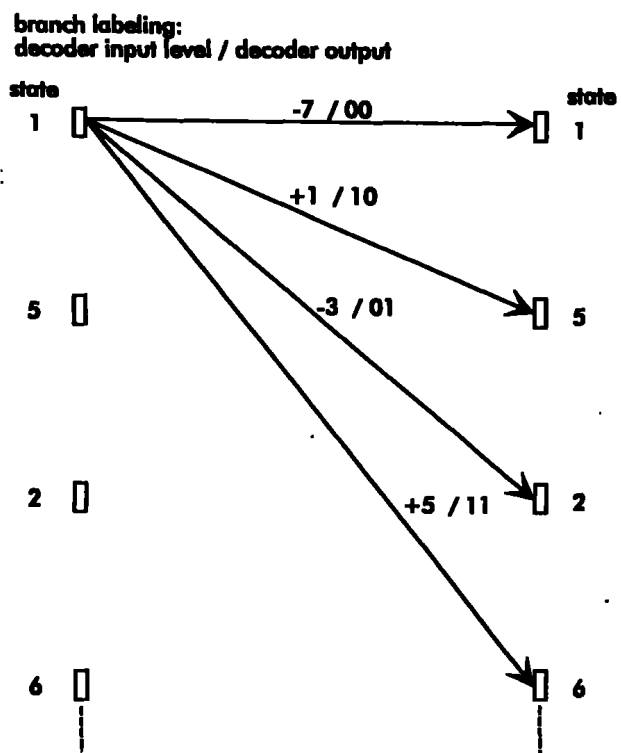


Figure 20

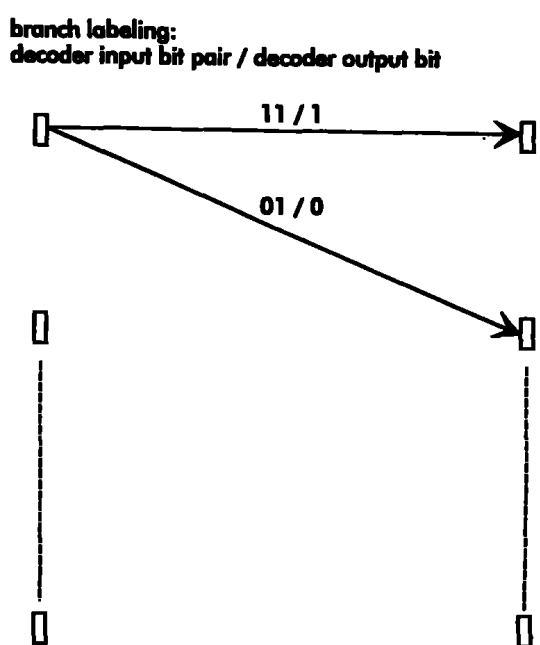


Figure 21

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tbl

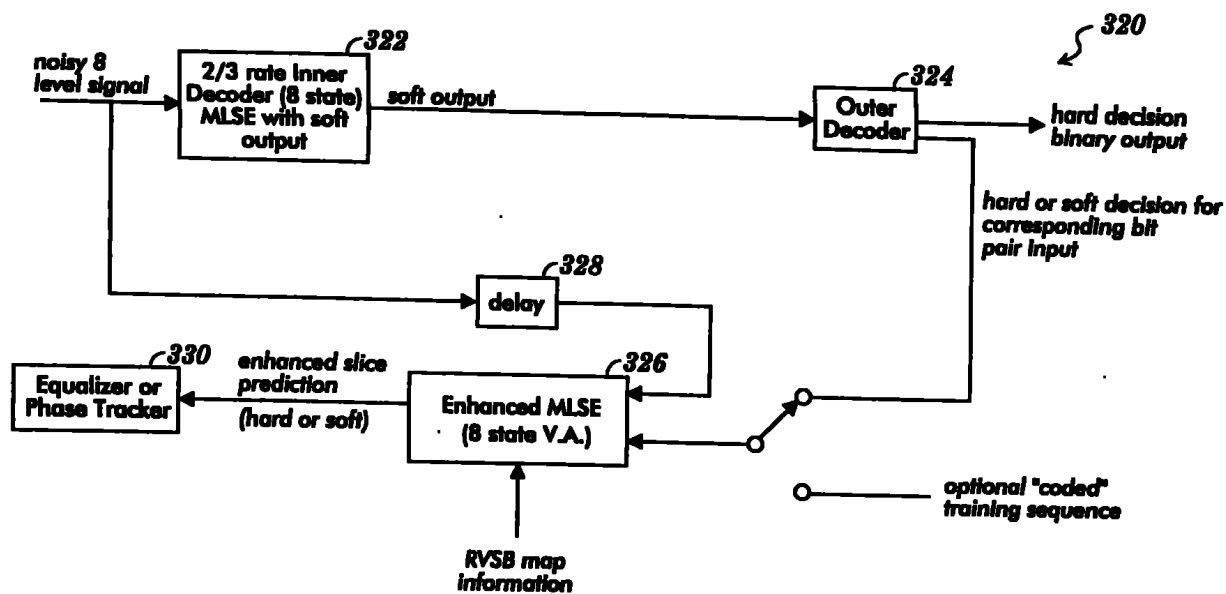


Figure 22

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RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

Solicitudes Relacionadas

Esta solicitud reivindica el beneficio la Solicitud Provisional Norteamericana No. 60/198.014, presentada el 18 de abril de 2000, la Solicitud Provisional Norteamericana No. 60/255.476 presentada el 13 de diciembre de 2000 y la Solicitud Provisional Norteamericana No. 60/255.464 presentada el 13 de diciembre de 2000.

Campo Técnico del Invento

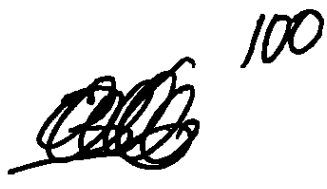
Este invento está relacionado con la transmisión y/o recepción de datos digitales.

Antecedentes del Invento

La norma para transmisión de señales digitales de televisión en los Estados Unidos se conoce como datos 8 VSB (Norma A/53 para Televisión Digital ATSC). Estos datos 8 VSB tienen una constelación que consiste de ocho niveles de símbolos posibles. En un sistema VSB los ocho millones de símbolos posibles se encuentran todos en la misma fase. Sin embargo, en un sistema QAM, los símbolos se transmiten en una relación de fase de cuadratura.

La norma arriba indicada especifica el formateo y modulación de datos digitales de video y audio. Los datos se

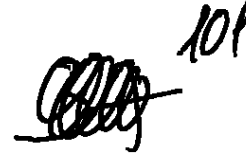
M. P. Tolson
Marta del Pilar Tolson
MANCINI I
SECRETARÍA GENERAL
Presidencia de la Corte Suprema

100


transmiten en la forma de símbolos con cada símbolo representando dos bits de datos que son cuadrículas codificadas en tres bits de datos codificados en cuadrícula. Cada tres bits de datos codificados en cuadrícula se mapean en un símbolo que tiene un nivel correspondiente entre los ocho niveles. La codificación e intercalación Reed/Solomon también se proveen para incrementar la robustez de la información transmitida.

Los datos auxiliares (diferentes de video digital o datos de audio) también pueden transmitirse en un canal de televisión digital. Estos datos se formatean y modulan de conformidad con la norma en la misma forma que los datos de video y audio. Los receptores fabricados de conformidad con la norma 8 VSB pueden leer identificaciones de paquetes (PIDs) que les permiten diferenciar entre datos de audio, video y datos auxiliares.

Sin embargo, mientras que la robustez de las señales de televisión digital transmitidas es suficiente para la recepción de televisión digital, esta robustez puede no ser suficiente para la transmisión de datos auxiliares, particularmente cuando dichos datos sean críticos. De acuerdo con lo anterior, una de las aplicaciones del presente invento

10P


es la transmisión de datos auxiliares en un formato VSB con codificación exterior para mayor robustez. Los datos auxiliares transmitidos de acuerdo con la aplicación del presente invento se referirán en este documento como los datos VSB robustos (RVSB).

Resumen del Invento

En un aspecto del presente invento, un método para proporcionar predicción mejorada de secciones comprende lo siguiente: recibir una entrada que contiene los primeros y los segundos datos, en donde los primeros y los segundos datos tienen diferentes tasas de bits y están definidos por la misma contestación de nivel n ; decodificar únicamente los segundos datos con un decodificador; producir una salida en respuesta a la entrada y al decodificador en donde la salida está confinada a al menos uno pero menos de $n/2$ de los niveles de constelación n y en donde $n > 2$; y proporcionar la salida como la predicción mejorada de secciones.

Handwritten notes: "donde?" with an arrow pointing to "y están definidos" and "donde" with an arrow pointing to "en donde".

En otro aspecto del presente invento un aparato para proporcionar la predicción mejorada de secciones comprende un decodificador interno, un decodificador externo y un predictor mejorado de secciones. El decodificador interno codifica una señal recibida para proporcionar una salida

interna decodificada. El decodificador interno produce $n/2$ estados de decodificación posibles con base en la señal recibida y la señal recibida contiene datos con n niveles en donde $n > 2$. El decodificador externo decodifica externamente la salida decodificada interna. El predictor mejorado de secciones elige al menos uno pero menos de $n/2$ de los $n/2$ estados de decodificación posibles con base en una salida del decodificador externo y proporciona el estado o estados elegidos como la predicción mejorada de secciones.

En otro aspecto del presente invento, un aparato que suministra la predicción mejorada de secciones incluye un decodificador interno, un decodificador externo y un predictor mejorado de secciones. El decodificador interno decodifica una señal recibida que contiene los primeros y los segundos datos para proporcionar dichos datos decodificados internamente. El decodificador externo decodifica externamente únicamente los segundos datos. El predictor mejorado de secciones proporciona una salida de predicción con base en los primeros datos cuando los segundos datos no están disponibles y con base en los segundos datos decodificados externamente cuando los segundos datos están disponibles.

Breve Descripción del Plano

Estas y otras características y ventajas serán más visibles desde una consideración detallada del invento cuando sean tomadas en su conjunto con el plano en el cual:

La Figura 1 muestra un transmisor VSB robusto para transmisión de datos VSB robustos y datos ATSC de conformidad con el presente invento;

La Figura 2 muestra un receptor estándar ATSC para recibir los datos ATSC transmitidos por el transmisor VSB robusto de la Figura 1;

La Figura 3 muestra un receptor VSB robusto para el recibo de datos VSB robustos transmitidos por el transmisor VSB robusto de la Figura 1;

La Figura 4 muestra el codificador con tasa de 2/3 de tasa de la Figura 1 con detalles adicionales;

La Figura 5 muestra la función de mapeo desempañada por el mapeador de la Figura 4;

La Figura 6 muestra la operación de los decodificadores de tasa 2/3 de las Figuras 2 y 3;

La Figura 7 muestra otro transmisor VSB robusto para transmitir datos VSB robustos y datos ATSC de acuerdo con el presente invento.

La Figura 8 muestra un receptor ATSC estándar para recibir los datos ATSC transmitidos por el transmisor VSB robusto de la Figura 7;

La Figura 9 muestra un receptor VSB robusto para recibir los datos VSB robustos transmitidos por el transmisor VSB robusto de la Figura 7;

La Figura 10 muestra un circuito para la generación de la señal de control adecuada en la línea de control de descarte de la Figura 9;

La Figura 11 muestra otro transmisor VSB robusto para la transmisión de datos VSB robustos y de datos ATSC de acuerdo con el presente invento;

La Figura 12 muestra un ejemplo de cuatro segmentos de datos que contienen datos codificados externos de tasa 1/2 que pueden transmitirse por un transmisor VSB robusto de acuerdo con el presente invento;

La Figura 13 muestra un ejemplo de cuatro segmentos de datos que contienen datos codificados externos de tasa 1/4

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que pueden transmitirse mediante un transmisor VSB robusto de acuerdo con el presente invento;

La Figura 14 muestra un ejemplo de cuatro segmentos de datos que contienen datos codificados externos de tasa 3/4 que pueden transmitirse mediante un transmisor VSB robusto de conformidad con el presente invento;

La Figura 15 muestra los intercaladores (I_r) de las Figuras 1, 9 y 11 con mayor detalle;

La Figura 16 muestra los desintercaladores (D_r) de las Figuras 3 y 9 con más detalle;

La Figura 17 muestra una estructura de definición de mapa de un primer paquete de datos VSB robustos de una trama;

La Figura 18 muestra una parte del segmento sincronizado de una trama que porta un mapa que indica en qué parte de la trama pueden encontrarse los datos VSB robustos;

La Figura 19 ilustra un predictor mejorado de secciones de acuerdo con una incorporación del presente invento;

La Figura 20 muestra las cuadrículas del decodificador interno de la Figura 19;

La Figura 21 muestra transiciones de estado posibles para el decodificador externo de la Figura 19; y

La Figura 22 ilustra un predictor mejorado de secciones de acuerdo con otra incorporación del presente invento.

Descripción Detallada

Transmisión y Recepción de Datos RVSB y ATSC

La Figura 1 muestra un transmisor VSB (10) que transmite tanto datos ATSC como datos VSB robustos (de acuerdo con) una incorporación del presente invento. La Figura 2 muestra un receptor ATSC estándar (12) que recibe los datos ATSC transmitidos por el transmisor VSB robusto (10), y la Figura 3 muestra un receptor VSB robusto (14) que recibe los datos VSB robustos transmitidos por el transmisor VSB robusto (10).

El transmisor VSB robusto (10) incluye un codificador Reed/Solomon (16) que codifica los bytes de datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a los bytes de datos auxiliares no codificados. Los bytes de datos auxiliares no codificados y los bytes de paridad Reed/Solomon son intercalados por un intercalador (18). Entonces los bytes de datos auxiliares sin codificar intercalados y los bytes de paridad Reed/Solomon se codifican con bits por un codificador externo (20) utilizando ya sea un

código convolucional u otro código de corrección de errores.

El codificador externo (20) mejora la robustez de los bytes de datos auxiliares no codificados y de los bytes de paridad Reed/Solomon, convirtiéndolos en bytes de datos robustos (en adelante denominados bytes de datos VSB robustos) y en bytes de paridad Reed/Solomon.

El codificador externo (20) puede por ejemplo, ser un codificador con una tasa de $1/2$ que produzca dos bits de salida por cada bit de entrada, o un codificador, con una tasa de $1/4$ que produzca cuatro bits de salida por cada bit de entrada, o un codificador con tasa de $3/4$ de tasa que produzca 4 bits de salida por cada tres bits de entrada. Otros codificadores podrán utilizarse en lugar de estos.

En la salida del codificador externo (20), se adiciona una cabecera de transporte (tx) de tres bytes a cada grupo de 184 datos VSB robustos codificados y bytes Reed/Solomon para formar paquetes de datos VSB robustos. Un multiplexor (24) multiplexa estos paquetes de datos VSB robustos con paquetes de datos ATSC (típicamente video y audio) cada uno de los cuales comprende una cabecera de transporte de tres bytes y 184 bytes de datos ATSC. Cualquiera de estas entradas al multiplexor (24) puede seleccionarse sobre la base de paquete

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por paquete y cada entrada seleccionada se suministra a un transmisor ATSC (26). La selección por parte del multiplexor (24) por cuya entrada pasa hacia el transmisor ATSC (26) está basada en un mapa VSB robusto que se describirá más adelante.

El transmisor ATSC (26), típicamente incluye un codificador (28) Reed/Solomon, un intercalador (30) y un codificador interno (32) de tasa 2/3, todo lo cual opera de conformidad con la norma ATSC.

Un receptor de la norma ATSC, tal como el receptor (12) de la norma ATSC que aparece en la Figura 2, recibe y procesa los datos ATSC y descarta los datos VSB robustos. De acuerdo con lo anterior, el receptor de la norma ATSC (12) incluye un decodificador interno de tasa 2/3 (34), un desintercalador (36) y un decodificador Reed/Solomon (38) todos los cuales operan de conformidad con la norma ATSC. Sin embargo, el receptor de la norma ATSC (12) está programado para decodificar las cabeceras de transporte de datos VSB robustos y de datos ATSC (lo cual incluye el paquete de identificaciones o PIDs que no han sido codificados por el codificador externo (20)). El receptor de la norma ATSC (12) lee los PIDs de todos los paquetes y en el (40), descarta aquellos paquetes que tengan los PIDs de datos VSB robustos.

El receptor de la norma ATSC (12) incluye también un predictor de secciones (42) (tal como el predictor de secciones de la Patente Norteamericana No. 5.923.711) que responde a los datos decodificados internos y que proporciona una salida de vuelta al rastreador de fase y/o ecualizador, tal como se conoce en la técnica.

Los paquetes de datos VSB robustos pueden recibirse, decodificarse y procesarse por un receptor VSB robusto tal como el receptor VSB robusto (14) que se muestra en la Figura 3. Como se conoce y como se muestra en la Figura 4, el codificador interno de tasa 2/3 (32) del transmisor ATSC (26) incluye un precodificador (44) y un codificador de cuadrículas de cuatro estados (46). En combinación, el precodificador (44) y el codificador de cuadrícula de cuatro estados (46) puede considerarse como un codificador de ocho estados que produce tres bits de salida codificados con cuadrícula (Z0 Z1 Z2) para cada dos bits de entrada (X1 X2). Un mapeador (48) mapea los tres bits de salida codificados con cuadrícula con un símbolo que tiene uno de ocho niveles en la forma en que se indica en la Figura 5. Tal como se conoce bien a partir de la teoría de ¹ código convolucional, la operación del precodificador (44) y del codificador de

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cuadrículas de cuatro estados (46) puede observarse como una cuadrícula cuaternaria de ocho estados.

Por consiguiente, en el receptor VSB robusto (14), un decodificador interno con tasa de $2/3$ (50) puede operar en cualquier cuadrícula cuaternaria (4-ary) de ocho estados que vea al precodificador (44) y al codificador de cuadrícula de cuatro estados (46) del codificador interno con tasa de $2/3$ en combinación, tal como se muestra en la Figura 6 para producir una decisión de salida blanda utilizando por ejemplo, el algoritmo SSA en la forma descrita en la publicación "Detección de Salida Blanda Optima para Canales con Interferencia de Intersímbolo", Li, Vucetic, y Sato, IEEE Transacciones sobre la Teoría de la Información, Mayo de 1995). Esta operación de toma de decisiones blandas es más complicada que el algoritmo Viterbi ampliamente utilizado, que produce una salida de decisión dura, pero la operación de toma de decisión blanda aprovecha más ampliamente de ganancia de la codificación provista por el codificador externo (20).

La salida del decodificador interno con tasa de $2/3$ (50) se desintercala por un desintercalador (52). El receptor VSB robusto (14) lee los PIDs de todos los paquetes a la salida del desintercalador (52). Con base en estos PIDs el receptor

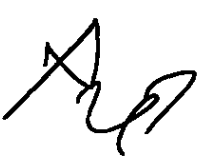
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VSB robusto (14) descarta estos paquetes en el (54) que tiene los PIDs de los datos ATSC y también descarta las cabeceras de transporte adicionales posteriormente al codificador externo (20) y los bytes de paridad adicionados por el codificador Reed/Solomon (28). Así, el receptor VSB robusto (14), en el (54), pasa únicamente los paquetes de datos VSB robustos que contienen los datos VSB robustos codificados por el codificador externo (20). Los paquetes de datos VSB robustos se decodifican por un decodificador externo (56), se desintercalan por un desintercalador (58) que es el inverso del intercalador (18) y Reed/Solomon se decodifica por un decodificador Reed/Solomon (60) para reconstruir los datos auxiliares no codificados originales provistos al codificador Reed/Solomon (16) de la Figura 1.

La salida confiable del decodificador externo (56) (que se puede utilizar en salida blanda o dura) es intercalada por un intercalador (62) (que corresponde al intercalador (30) en un trayecto de retroalimentación (64) con el fin restaurar el ordenamiento de los datos decodificados externos al orden de los datos en el canal. Estos datos decodificados externos intercalados pueden por ejemplo utilizarse por un predictor de secciones (66) para crear retroalimentación confiable a un rastreador de fase y/o ecualizador. Sin embargo, la demora de

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la retroalimentación general introducida por el desintercalador (52) y el intercalador (62) en el receptor VSB robusto (14) es generalmente muy larga para proporcionar retroalimentación útil al rastreador de fase y/o al ecualizador.

El arreglo que se muestra en las Figuras 7, 8 y 9 evita la demora en la retroalimentación introducida por el desintercalador (52) y el intercalador (62) del receptor VSB robusto (14). La Figura 7 muestra un transmisor VSB robusto (80) en el cual los bytes de datos auxiliares no codificados se codifican por un codificador Reed/Solomon (82) que adiciona bytes de paridad Reed/Solomon a los bytes de datos auxiliares no codificados. Los bytes de datos auxiliares no codificados y los bytes de paridad Reed/Solomon son intercalados por un intercalador (84). Entonces, los bytes de datos auxiliares no codificados intercalados y los bytes de paridad Reed/Solomon se codifican en término de bits por un codificador externo (86), utilizando ya sea un código convolucional o un código de producto turbo, en la forma arriba indicada. La salida en términos de bits del codificador externo (86) es un pequeño bloque intercalado por un intercalador de bloques pequeño (88) con el fin de reducir el impacto de los errores de las ráfagas del canal en el



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decodificación externo. A los datos provistos por el
intercalador de bloques pequeño (88) puede hacerse referencia
como Rdatos (n.o.) que corresponde a los datos VSB robustos
ordenados normalmente.

Una entrada del primer multiplexor (92) recibe
paquetes formateados ATSC cada uno de los cuales comprende
(i) una cabecera válida de transporte de tres bytes con un
número PID para datos VSB robustos, (ii) 184 bytes que
sostienen lugares de datos VSB robustos simulados, y (iii)
veinte bytes que sostienen lugares para datos de paridad
Reed/Solomon ATSC simulados. La otra entrada del primer
multiplexor (92) recibe paquetes simulados formateados ATSC,
cada uno de los cuales tiene 207 bytes de datos ATSC
simulados. Estos paquetes simulados formateados ATSC sirven
como tenedores de lugares ("placeholders") para los paquetes
ATSC reales que se añaden corriente abajo. Las entradas del
primer multiplexor (92) pueden seleccionarse sobre la base de
paquete por paquete y esta selección esta basada en el mapa
VSB robusto que se describirá más adelante.

Las salida seleccionada del primer multiplexor (92) es
intercalada por un intercalador (94) de acuerdo con la Norma
ATSC para intercalación convolucional de bytes. Un

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reemplazador de datos (96) recibe tanto la salida del intercalador (94) como la salida del intercalador de bloques pequeños (88). El reemplazador de datos (96) reemplaza cada byte con lugar para tener datos VSB robustos simulados desde el intercalador (94) con los siguientes bytes de datos VSB robustos normalmente ordenados desde el intercalador de bloques pequeños (88).

La salida del reemplazador de datos (96) contiene datos VSB robustos normalmente ordenados con cabeceras de transporte entremezcladas, bytes de paridad Reed/Solomon ATSC simulados y bytes de paquetes de datos ATSC simulados. Un desintercalador (98), que opera de acuerdo con la Norma ATSC para la desintercalación de bytes, desintercala la salida del reemplazador de datos (96) para así "repaquetizar" de forma efectiva los datos como paquetes de cabeceras de transporte, o datos VSB robustos reordenados (Rdata(r.o.)), o bytes de paridad Reed/Solomon ATSC simulados y datos ATSC simulados. El reordenamiento de los datos VSB robustos reordenados normalmente resulta de la desintercalación del desintercalador (98) y a los datos reordenados puede hacerse referencia como datos VSB robustos reordenados.

Los bytes de paridad Reed/Solomon ATSC simulados (20 por paquete) de los paquetes VSB robustos y de los paquetes de datos ATSC simulados (207 bytes por paquete) se descargan en (100). Los paquetes VSB robustos restantes, cada uno de los cuales incluye una cabecera de transporte y datos VSB robustos reordenados, son multiplexados por un segundo multiplexor (102) con paquetes de datos ATSC reales cada uno de los cuales contiene 187 bytes de una cabecera de transporte y datos ATSC. Cualquiera de las entradas al segundo multiplexor (102) puede seleccionarse sobre la base de paquete por paquete y se provee a un transmisor ATSC (104). La selección del segundo multiplexor (102) cuya entrada pasa al transmisor ATSC (104) está basada en un mapa VSB robusto que se describirá más adelante.

El transmisor ATSC (104) típicamente incluye un codificador Reed/Solomon (106), un intercalador (108) y un codificador interno de tasa 2/3 de doce vías (110) todo lo cual opera de conformidad con la norma ATSC. Del codificador Reed/Solomon (106) salen paquetes de cabeceras de transporte, datos VSB robustos reordenados y bytes de paridad Reed/Solomon ATSC multiplexados con paquetes de cabeceras de transporte, datos ATSC y bytes de paridad Reed/Solomon ATSC. Los bytes de paridad Reed/Solomon ATSC para los datos VSB

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robustos se calculan con base en los datos VSB robustos reordenados. Además, el intercalador (108) cambia el ordenamiento de los datos VSB robustos de manera que dichos datos en la salida del intercalador (108) vuelvan a ser datos VSB robustos normalmente ordenados. También el intercalador (108) dispersa las cabeceras de transporte, los bytes de paridad Reed/Solomon ATSC y los datos ATSC. Estos datos son codificados a una tasa de 2/3 por el codificador interno de tasa 2/3 de doce vías (110) y se transmiten. Los datos VSB robustos transmitidos están en el orden normal, v.g., el orden provisto a la salida del intercalador de bloques pequeños (88). Este orden normal permite que el receptor VSB robusto evite la demora causada por el desintercalador (52) y por el intercalador (62) del receptor VSB robusto (14).

Tal como se indica en la Figura 8, un receptor de la norma ATSC (120) incluye un decodificador interno 2/3 de doce vías que decodifica los datos transmitidos para proporcionar un flujo de datos de salida que comprenda datos robustos normalmente ordenados con cabeceras intercaladas de transporte, datos ATSC, y bytes de paridad Reed/Solomon ATSC ubicados de acuerdo con la intercalación convolucional de bytes ATSC provista por el intercalador (108). Un desintercalador ATSC (124) ~~restituye~~ las cabeceras de

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transporte, los datos ATSC y los bytes de paridad Reed/Solomon ATSC hacia sus posiciones "paquetizadas" de transporte. También el desintercalador ATSC (124) convierte los datos VSB robustos ordenados normalmente en datos VSB robustos reordenados. Esta forma reordenada permite que un decodificador Reed/Solomon ATSC (126) del receptor ATSC estándar (120) lleve a cabo pruebas correctas de la paridad de los paquetes de datos VSB robustos. El receptor ATSC estándar (120) puede entonces leer las cabeceras de transporte de los paquetes de datos VSB robustos y fácilmente descartar los paquetes de datos VSB robustos en (128) con base en sus PIDs.

Tal como se indica en la Figura 9, un receptor VSB robusto (130) incluye un decodificador interno de tasa 2/3 de doce vías de salida blanda (132). (Un decodificador de 2/3 de salida dura originaría una pérdida considerable de la ganancia de codificación). La salida del decodificador interno de tasa 2/3 de doce vías de salida blanda (132) incluye datos VSB robustos ordenados de forma normal con datos ATSC reordenados, cabeceras de transporte y símbolos de paridad Reed/Solomon ATSC dispersados dentro de los datos VSB robustos en las ubicaciones indicadas por una línea de control de descarte (134) de la que se hablará más adelante.

1 de 2 errada

Un bloque de descarte (136), bajo el control de la línea de control de descarte (134), descarta los datos ATSC reordenados, las cabeceras de transporte y los símbolos de paridad Reed/Solomon ATSC.

Un desintercalador de bloques pequeños (138) desintercala los datos VSB robustos. El desintercalador de bloques pequeños (138) tiene un tiempo de demora relativamente bajo. El desintercalador dispersa errores posibles de ráfaga en los datos VSB robustos a la salida del decodificador interno de tasa 2/3 con doce vías de salida blanda (132). Los datos VSB robustos ordenados de forma normal se decodifican en términos de bits por un decodificador externo (140) que también agrupa los datos VSB robustos en bytes. La información amplificada le indica al decodificador externo (140) qué tasa de codificación utilizar en los datos provistos al decodificador externo (140) en una entrada de Datos R_{MAP} . No se necesita ni el desintercalador (52) ni el intercalador (62) en el receptor VSB robusto (130) permitiendo menos demora en la retroalimentación general hacia el rastreador de fase y/o el ecualizador. Los datos decodificados externos pueden ser utilizados, por ejemplo, por un predictor mejorado de secciones (142) para generar retroalimentación al rastreador de fase y/o al ecualizador.

~~scribble~~

Si se desea, la retroalimentación puede atravesar por una compuerta o se puede ajustar el algoritmo del gradiente del ecualizador del tamaño del paso proporcionalmente a la confiabilidad de los datos decodificados.

La carga útil del paquete de datos VSB robusto decodificada por el decodificador externo (140) es desintercalada por un desintercalador (144) (que corresponde al inverso del intercalador (84)) y recibe una decodificación Reed/Solomon por un decodificador Reed/Solomon (146) (que corresponde al codificador Reed/Solomon (82)) para reconstruir los datos auxiliares no codificados originales proporcionados al codificador Reed/Solomon (82) de la Figura 7.

proceda

Tal como se indica en la norma ATSC, un marco comprende una diversidad de segmentos cada uno de los cuales contiene un número predeterminados de bytes. El primer segmento de una trama es un segmento sincronizado de la trama y los segmentos restantes en la trama son segmentos de datos. Aunque los datos VSB robustos pueden transmitirse en segmentos o en segmentos parciales, es conveniente transmitir dichos datos en pares de segmentos. El mapa VSB robusto discutido arriba indica cuáles pares de segmentos contienen datos VSB robustos

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para que el bloque de descarte (136) pueda descartar correctamente los datos ATSC reordenados antes de que éstos puedan llegar al decodificador externo (140). Las cabeceras de transporte y los datos de paridad Reed/Solomon ATSC para todos los segmentos (VSB robustos y ATSC) también pueden descartarse por el bloque de descarte (136).

En la Figura 10 aparece un circuito conceptualmente simple para generar la señal de control adecuada en la línea de control de descarte (134) para controlar esta función de descarte, junto con la porción relevante del receptor VSB robusto (130). El receptor VSB robusto (130) utiliza la información del mapa recibida (el método para transmisión y recepción de esta información de mapa está descrito a continuación) para dar una orden a un generador de segmento simulado (150) de cuándo construir los segmentos de bytes simulados (207). El generador de segmentos simulados (150) también utiliza la señal sincronizada de la trama. Para cada segmento simulado ATSC, el generador de segmentos simulados (150) fija todos los bytes en FF. Para cada uno de los segmentos simulados de los datos VSB robustos, el generador de segmentos simulados (150) fija la cabecera de transporte y los bytes de paridad Reed/Solomon en FF. El generador de

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~~FIGURA 11~~

segmentos simulados (150) fija el resto de los bytes de cada segmento simulado de datos VSB robustos en 00.

Estos segmentos simulados son alimentados por el generador de segmentos simulados (150) a un intercalador de bytes convolucional (152) cuya salida es posteriormente utilizada para controlar el bloque de descarte (136) que posteriormente responde a los códigos FF y 00 para descartar correctamente los datos ATSC reordenados, las cabeceras de transporte y los datos de paridad Reed/Solomon ATSC que están intercalados dentro del flujo de datos recibidos. El bloque de descarte (136) entonces, pasa únicamente por los datos VSB robustos.

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La Figura 11 muestra un transmisor VSB robusto con código de salida múltiple (160). El transmisor VSB robusto (160) opera de forma similar al transmisor VSB robusto (80) de la Figura 7. El transmisor VSB robusto (160) tiene el primer codificador Reed/Solomon (162) que codifica los primeros datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a los primeros datos auxiliares no codificados, un segundo codificador Reed/Solomon (164) que codifica los segundos datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a los segundos datos

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auxiliares no codificados, y un tercer codificador Reed/Solomon (166) que codifica los terceros bytes de datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a dichos terceros datos auxiliares no codificados. Los datos auxiliares no codificados, codificados de primeros como Reed/Solomon, son intercalados por un primer intercalador (168); los segundos datos auxiliares no codificados, codificados como Reed/Solomon, son intercalados por un segundo intercalador (170) y, los terceros datos auxiliares no codificados, codificados como Reed/Solomon, son intercalados por un tercer intercalador (172). Entonces, los primeros datos auxiliares no codificados, codificados como Reed/Solomon intercalados, se codifican en términos de bits por un primer codificador externo (174); los segundos datos auxiliares no codificados, codificados como Reed/Solomon intercalados, se codifican en términos de bits por un segundo codificador externo (176), y los terceros datos auxiliares no codificados, codificados como Reed/Solomon intercalados, se codifican en términos de bits por un tercer decodificador externo (178). La salida en términos de bits del primer codificador externo (174) es intercalada por un primer intercalador de bloques pequeños (180); la salida en términos de bits del segundo codificador externo (176) es intercalada

por un segundo intercalador de bloques pequeños (182) y la salida en términos de bits del tercer decodificador externo (178) es intercalada por un tercer intercalador de bloques pequeños (184).

El primer codificador externo (174) es un codificador con tasa de 1/4, el segundo codificador externo (176) es un codificador con tasa de 1/2 y el tercer decodificador externo (178) es un decodificador con tasa de 3/4, aún cuando se puede utilizar cualquier otra combinación de estos u otros codificadores externos que utilicen diferentes tasas de códigos. Las salidas de datos del primero, segundo y tercer intercaladores de bloques pequeños (180, 182 y 184) es seleccionada por un multiplexor (186) bajo control de una entrada selecta que determina el orden en que los diferentes datos codificados externos se insertan a la trama para ser transmitidos. Los datos a la salida de multiplexor (186) pueden mencionarse como Rdata(n.o.), los cuales tal como ya se dijo, corresponden a datos VSB robustos normalmente ordenados.

Las tres entradas superiores de un multiplexor (190) reciben paquetes de formato ATSC, cada uno de los cuales tiene una cabecera de transporte de tres bytes con un número



de PID para datos VSB robustos (184), bytes con sitio para sostener datos VSB robustos simulados y veinte bytes simulados con sitio para sostener datos de paridad Reed/Solomon ATSC. Los datos VSB robustos en la entrada de más arriba del multiplexor (190) corresponden a datos codificados con tasa de $1/4$ del primer codificador externo (174); los datos VSB robustos en la siguiente entrada del multiplexor (190) corresponden a datos codificados con tasa de $1/2$ del segundo codificador externo (176) y los datos VSB robustos en la siguiente entrada del multiplexor (190) corresponden a datos codificados a una tasa de $1/3$ del tercer codificador externo (178). Los datos suministrados por la entrada más baja del multiplexor (190) comprenden paquetes simulados del formato ATSC, cada uno de los cuales tiene 207 bytes de datos ATSC simulados. Estos paquetes de datos ATSC simulados sirven como sostenedores para los paquetes de datos ATSC reales que deben adicionarse corriente abajo del multiplexor (190). Las entradas al multiplexor (190) se pueden seleccionar sobre una base de paquete por paquete de acuerdo con la entrada sobre la línea de selección. Esta selección está basada en el mapa de datos VSB robusto que se describe más adelante.

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La salida del multiplexor (190) es intercalada por un intercalador (192) para lograr una intercalación convolucional ATSC correcta. Un reemplazador de datos (194) recibe tanto la salida del intercalador (192) como la salida del multiplexor (186). El reemplazador de datos (194) reemplaza cada byte con lugar para tener datos VSB robustos simulados desde el multiplexor (190) con los siguientes bytes de datos VSB robustos correspondientes ordenados normalmente que provienen del multiplexor (186).

La salida del reemplazador de datos (194) contiene datos VSB robustos normalmente ordenados (codificados a tasas de 1/4, 1/2 y/o 3/4 según sea apropiado) con cabeceras de transporte intercaladas, bytes de paridad Reed/Solomon ATSC simulados, y bytes de paquetes de datos ATSC simulados. Un desintercalador de bytes convolucional (196) (en la forma descrita en la Norma ATSC) desintercala la salida del reemplazador de datos (194) para así "repaquetizar" eficazmente los datos como paquetes de cabeceras de transporte, datos VSB robustos reordenados (codificados a tasas de 1/4, 1/2 o 3/4), bytes de paridad Reed/Solomon ATSC simulados y paquetes simulados de datos ATSC. El reordenamiento de los datos VSB robustos ordenados

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normalmente resulta de la desintercalación del desintercalador (196).

Los bytes de paridad Reed/Solomon ATSC simulados (20 por paquete) y los paquetes de datos ATSC simulados (207 bytes por paquete) se descartan en el (198) en una forma similar a aquella provista por la línea de control de descarte (134) y el bloque de descarte (136) de la Figura 9. Los paquetes VSB robustos restantes, cada uno de los cuales incluye una cabecera de transporte y datos VSB robustos reordenados, son multiplexados por un multiplexor (200) con paquetes de datos ATSC reales, cada uno de los cuales contiene 187 bytes de cabecera de transporte y datos ATSC. Cualquier entrada al multiplexor (200) puede seleccionarse sobre una base de paquete por paquete y se suministra a un transmisor ATSC (202). La selección del multiplexor (200) cuya entrada pasará al transmisor ATSC (202) está basada en el mapa VSB robusto que se describirá más adelante.

Pila
orden

El transmisor ATSC (202) típicamente incluye un codificador Reed/Solomon (204), un intercalador (206) y un codificador interno con tasa de 2/3 de doce vías (208) todo lo cual opera de conformidad con la norma ATSC. El codificador Reed/Solomon (204) saca los paquetes de cabeceras

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de transporte, los datos VSB robustos reordenados y los bytes de paridad Reed/Solomon ATSC multiflexados con paquetes de cabeceras de transporte, datos ATSC, y bytes de paridad Reed/Solomon ATSC. Los bytes de paridad Reed/Solomon ATSC para los datos VSB robustos se calculan con base en los datos VSB robustos reordenados. Además, el intercalador (206) cambia el ordenamiento de los datos VSB robustos de manera que dichos datos a la salida del intercalador (206) nuevamente sean datos VSB robustos ordenados de forma normal. También el intercalador (206) dispersa los bytes de la cabecera de transporte, los bytes de paridad Reed/Solomon ATSC y los datos ATSC. Estos datos son codificados a 2/3 a una tasa de 2/3 por un codificador interno de tasa de 2/3 con doce vías (208) y son transmitidos. Los datos VSB robustos transmitidos se encuentran en orden normal, v.g., el orden provisto a la salida del multiplexor (186). Este orden normal de datos permite al receptor VSB robusto evadir la demora causada por el desintercalador (52) y por el intercalador (62).

Tal como se discutió arriba, una trama ATSC comprende un segmento sincronizado de trama y una diversidad de segmentos y para conveniencia, los datos VSB robustos se empaquetan en grupos de cuatro segmentos. Más específicamente, la Figura 12

muestra un ejemplo de cuatro segmentos de datos que se puede utilizar en una trama para transmitir datos VSB robustos que están codificados a una tasa de $1/2$, la Figura 13 muestra un ejemplo de cuatro segmentos de datos que pueden utilizarse en una trama para transmitir datos VSB robustos que están codificados a una tasa de $1/4$ y la Figura 14 muestra un ejemplo de cuatro segmentos de datos que pueden utilizarse en una trama para transmitir datos VSB robustos que están codificados a una tasa de $3/4$. Estos ejemplos representan la trama antes del intercalador (108) y asumen que cada grupo de cuatro segmentos de datos VSB robustos contiene un número integral de bloques codificados Reed/Solomon robustos cada uno de los cuales tiene 184 bytes de largo, de los cuales veinte bytes son bytes de paridad.

Para el caso de un código externo con tasa de $1/2$, la Figura 12 muestra que el codificador externo saca dos bits por cada bit de entrada. Un paquete de datos VSB robusto se empaca como un bloque Reed/Solomon RVSB (hacia un par de segmentos de datos) (un bit por símbolo) de manera que, para un código de salida con tasa de $1/2$, cuatro segmentos contengan dos bloques codificados Reed/Solomon robustos. Como se indica en la Figura 13, para el caso de códigos externos con tasa de $1/4$, el codificador externo saca cuatro bits por

cada bit de entrada. Los datos VSB robustos se empacan como un bloque Reed/Solomon RVSB por cada cuatro segmentos de datos ($1/2$ bit por símbolo) de manera que, para un código externo con tasa de $1/4$, cuatro segmentos contengan un bloque codificado Reed/Solomon robusto. Tal como se indica en la Figura 14, para el caso del código externo de tasa de $3/4$ el codificador externo saca cuatro bits por cada tres bits de entrada. En este caso, las fronteras de los bytes y símbolos transmitidos no siempre concuerdan. Sin embargo, tres bloques completos Reed/Solomon RVSB conformarán un paquete exacto de cuatro segmentos de datos (1.5 bits por símbolo) de manera que, para un código externo con tasa de $3/4$, cuatro segmentos contengan tres bloques codificados Reed/Solomon robustos.

De acuerdo con lo anterior, las Figuras 12, 13 y 14 pueden representarse por la siguiente tabla:

S	X	Y
$1/2$	1	2
$1/4$	1	4
$3/4$	3	4

donde X representa el número de bloques codificados Reed/Solomon robustos completos y Y representa el número de segmentos de trama requeridos para contener el número X correspondiente de bloques codificados Reed/Solomon robustos.

2 Sin embargo, debe entenderse que pueden utilizarse otras tasas de codificación en relación con el presente invento y, por consiguiente, la tabla anterior variará dependiendo de las tasas particulares de codificación que se utilicen.

Los intercaladores (18), (84), (168), (170) y (172) se indican con más detalle en la Figura 15 y los desintercaladores (58) y (144) también se muestran con más detalle en la Figura 16, asumiendo que el bloque codificado Reed/Solomon robusto se elige para que tenga 184 bytes de largo. Los intercaladores (18), (84), (168), (170) y (172) son intercaladores convolucionales $B = 46$, $M = 4$, $N = 184$ que intercalan los datos VSB robustos en términos de bytes. Este esquema de intercalación es el mismo esquema de intercalación ATSC descrito en la Norma A/53 de Televisión Digital ATSC y en la Guía para Utilizar la Norma A/54 de Televisión Digital ATSC, salvo que el parámetro B para el intercalador robusto es (46) en lugar de (52) y el parámetro N es (184) en lugar de (208). Este intercalador se requiere para que el receptor VSB robusto pueda manejar las largas ráfagas de ruido en el canal aún cuando no se pase por el desintercalador (D_a) ATSC, como se indica en la Figura 9.

Tal como se ilustra en la Figura 16, los desintercaladores (58) y (144) son desintercaladores convolucionales $B = 46$, $M = 4$, $N = 184$ que desintercalan los datos VSB robustos en términos de bytes. Este esquema de desintercalación también es igual al esquema de desintercalación ATSC descrito en la Norma A/53 de Televisión Digital ATSC y en la Guía para la Utilización de la Norma A/54 de Televisión Digital ATSC, salvo que el parámetro B para el desintercalador robusto es (46) en lugar (52) y el parámetro N es (184) en lugar de (208).

Teniendo en cuenta que el bloque Reed/Solomon VSB robusto comprende 184 bytes y que un número integral de bloques Reed/Solomon VSB robustos se encuentra en una trama de datos, el número de bytes de datos VSB robustos más el número de bytes de paridad Reed/Solomon VSB robustos en una trama de datos es siempre divisible por 46. Entonces, el segmento sincronizado de trama puede utilizarse como un sincronizador para los desintercaladores (58) y (144) (D_r) en el receptor, independientemente del valor de G (que se describe más adelante). En la sincronización de la trama los conmutadores del desintercalador están forzados a las posiciones más altas. Los desintercaladores (58) y (144) son desintercaladores en términos de bytes.

Mapeo de Datos

Tal como se indicó arriba, cada trama de datos puede contener una mezcla de segmentos de datos VSB robustos y de segmentos de datos ATSC (no codificados robustamente).

Además, los datos VSB robustos pueden contener datos codificados con una mezcla de tasas de codificación. El receptor VSB robusto (14) o (130) debe tener un mapa VSB robusto que indica cuáles segmentos son codificados VSB robustos y cuáles códigos externos se utilizan para la codificación VSB robusta de manera que el receptor VSB robusto (14) o (130) puedan correctamente procesar los datos VSB robustos y descartar los datos ATSC. Los transmisores VSB robustos (10), (80) y (160) también utilizan el mapa VSB robusto para controlar su correspondiente multiplexión y descartar funciones. Este mapa VSB robusto se transmite por un transmisor VSB robusto (10), (80) o (160) al receptor VSB robusto (14) o (130) junto con todos los demás datos en la forma descrita a continuación.

La presencia, número y ubicación de los datos VSB robustos en una trama de datos codificada con un código externo particular se indica por uno o más números Sc que aparecen como datos de dos niveles en el segmento

sincronizado de trama de la trama de datos. Como ya se sabe, el segmento sincronizado de trama es el primer segmento en una trama. Entonces, para los códigos externos descritos arriba (con tasas de $1/4$, $1/2$ y $3/4$), el segmento sincronizado de trama preferiblemente debe contener $[S_{1/4}, S_{1/2}, \text{ y } S_{3/4}]$. Cada S_c (tal como $S_{1/4}$, $S_{1/2}$, y $S_{3/4}$) se codifica como diez y ocho símbolos (bits) de dos niveles de datos. Para todos los tres códigos, un total de $3 \times 18 = 54$ símbolos se requieren como una definición del mapa VSB robusto. Estos símbolos se insertan al área reservada cerca de la terminación de cada segmento sincronizado de trama (justo antes de los doce bits de precodificación). Para cada grupo de diez y ocho bits ($b_{18} \dots b_1$), los últimos seis bits ($b_6 \dots b_1$) representan el número G de grupos de ocho segmentos (8 segmentos = 2, 4 o 6 paquetes de datos VSB robustos dependiendo del código de salida) mapeados como datos VSB robustos en la trama actual. Los doce bits precedentes son para compensación de filtros combinada (ver la Guía para la Utilización de la Norma A/54 de Televisión Digital ATSC). De acuerdo con lo anterior, tal como se indica en la Figura 18, los bits $b_6 \dots b_1$, representan el número G, los bits $b_{18} \dots b_{13}$ son el complemento de los bits $b_6 \dots b_1$ y los bits $b_{12} \dots b_7$ pueden alternarse +1 y -1 (o en cualquier otro patrón).

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Asumamos que $S = S_{1/4} + S_{1/2} + S_{3/4}$. Como $312/8 = 39$, 0-39 se pueden mapear grupos de ocho segmentos como datos VSB robustos o como 8 datos VSB (datos ATSC). Por consiguiente, cada S_c puede tener un valor de 0...39, siempre que la suma S de los mismos sea ≤ 39 .

Los segmentos de datos VSB robustos preferiblemente se distribuyen en la forma más uniforme posible a lo largo de la trama de datos. Por ejemplo, si $S = 1$, entonces los siguientes ocho segmentos se mapean como segmentos de datos VSB robustos y todos los otros segmentos se mapean como segmentos de datos ATSC: (1), (40), (79), (118), (157), (196), (235) y (274). Si $S = 2$, entonces los siguientes diez y seis segmentos se mapean como segmentos de datos VSB robustos y todos los demás segmentos se mapean como segmentos de datos ATSC: (1), (20), (39), (58), (77), (96), (115), (134), (153), (172), (191), (210), (229), (248), (267) y (286). Estos ejemplos continúan hasta cuando $S = 39$, en donde toda la trama de datos se mapea como segmentos de datos VSB robustos. Para algunos valores de S , el espacio entre pares de segmentos de datos VSB robustos no es perfectamente uniforme. Sin embargo, para cualquier valor de S , el espacio

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se determina de forma anticipada y por consiguiente, es conocido para todos los receptores.

Si una trama contiene datos VSB robustos proporcionados por tres codificadores externos que operan a tasas de $1/4$, $1/2$ y $3/4$, entonces los datos de estos tres codificadores externos se pueden dividir en una trama de manera que en cuanto se refiere a los segmentos RVBS, los primeros segmentos $8 \times S_{1/4}$ contengan los datos codificados externos con tasa de $1/4$, los siguientes segmentos $8 \times S_{1/2}$ contengan datos codificados externos con tasa de $1/2$ y los últimos segmentos $8 \times S_{3/4}$ contengan datos codificados externos con tasa de $3/4$. Sin embargo, son posibles otras organizaciones de segmentos de datos VSB robustos para estos tres codificadores externos o para cualquier número de otro tipo de codificadores externos.

Considerando que este mapa VSB robusto está contenido en el segmento sincronizado de trama, tal como se discutió arriba, el mapa VSB robusto no disfruta del mismo nivel de ganancia de codificación que los datos VSB robustos. No obstante, el mapa VSB robusto puede todavía adquirirse en forma confiable por un receptor VSB robusto mediante la correlación del mapa VSB robusto sobre algún número de

tramas. Por consiguiente, el mapa VSB robusto no debe cambiar muy a menudo (por ejemplo, no más a menudo de cada ~60 tramas).

El método de mapeo arriba indicado le permite a un receptor adquirir confiable y simplemente el mapa VSB robusto por correlación. Una vez que un receptor ha adquirido el mapa, es deseable que instantáneamente rastree los cambios en el mismo de forma confiable. Para rastrear dichos cambios en el mapa de forma instantánea y confiable, la definición del mapa VSB robusto para cada código externo, excluyendo los bits combinados de compensación, se duplica en el primer bloque codificado Reed/Solomon VSB robusto de la trama. Además, existen datos que indican (i) cuándo en el futuro el mapa cambiará y (ii) la definición futura del nuevo mapa. El primer paquete de datos VSB robustos de una trama para un codificador externo, por consiguiente, tiene la estructura indicada en la Figura 17, en donde la definición de datos del mapa VSB robusto está dada por lo siguiente: ocho bits que designan en mapa actual (únicamente seis de estos bits se utilizan); ocho bits que designan el número de tramas hasta que cambia el mapa (1-125; si es 0, entonces no se esperan cambios); y, ocho bits que designan el siguiente mapa (nuevamente, solo seis de estos bits se utilizan). La porción

restante del primer paquete de datos VSB robustos corresponde a datos. El primer segmento RVSB en una trama para un codificador externo respectivo tiene el arreglo que se ilustra en la Figura 17.

De esta forma, un receptor puede rastrear cambios en el mapa utilizando datos VSB robustos confiables. Aún cuando un error de ráfaga destruya un número de tramas, el receptor puede mantener su propio conteo descendiente de las tramas utilizando el número de tramas que se hayan leído a partir de una trama recibida previamente. Si el receptor en cualquier momento encuentra que una definición para un código externo previamente adquirido por la correlación sincronizada de la trama no concuerda con la definición para dicho código externo en el primer segmento de datos VSB robustos, el receptor debe reiniciar su proceso de adquisición del mapa. X

Predicción Mejorada de Secciones RVSB y Retroalimentación del Ecualizador

Los receptores VSB ATSC 8 hacen uso importante de la ecualización adaptativa y del rastreo de fase en la forma explicada en la Norma A/53 de Televisión Digital ATSC publicada por el Comité de Sistemas Avanzados de Televisión, en la Guía para la Utilización de la Norma A/54 de Televisión

Digital ATSC, también publicada por el Comité de Sistemas de Televisión Avanzada. El RVSB tal como se describió arriba tiene características que permiten mejoras en la ecualización adaptiva y en el rastreo de la fase.

El mejoramiento resulta de la retroalimentación de estimados confiables demorados del nivel de simbolos de entrada al ecualizador adaptivo y/o rastreador de fase con base en una estimación de secuencias a partir de un Algoritmo Viterbi mejorado. (Ver "El Algoritmo Viterbi", G. D. Forney, Jr., Proc. IEEE, vol 61, pp. 268-278, marzo de 1973). Este tipo de retroalimentación evita la necesidad de "recodificación", que tiene un problema de inicialización de estado.

La Patente Norteamericana No. 5.923.711 titulada "Predictor de Secciones para un Receptor de Señal" revela un receptor VSB 8 ATSC que utiliza un predictor de secciones con el fin de proporcionar retroalimentación más confiable al rastreador de fase o al ecualizador adaptivo. Esta retroalimentación puede ser aún más confiable con el sistema de predicción de secciones mejorado (300) que se muestra en la Figura 19. El sistema de predicción de secciones mejorado (300) tiene un decodificador interno (302) y un decodificador

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externo (304) que operan de forma similar a los decodificadores internos y a los decodificadores externos arriba descritos.

La salida de predicción de secciones del decodificador interno (302) trabaja en una forma similar a aquella descrita en la Patente Norteamericana 5.923.711 arriba mencionada. Tal como se explicó anteriormente, el decodificador interno (302) se basa en cuadrículas cuaternarias (4-ary) de 8 estados que incluyen un precodificador. Con base en la mejor métrica de trayectoria al tiempo actual t , el predictor de secciones del decodificador interno (302) decide el estado más probable en el tiempo t . Entonces, con base en el siguiente par posible de estados, se seleccionan cuatro niveles de entrada predicha posible (entre ocho) para el siguiente símbolo en el tiempo $t + 1$. Por ejemplo, como se indica en las cuadrículas del decodificador interno en la Figura 20, si el estado más probable en el tiempo t es el estado uno, el siguiente estado será $\epsilon[1 \ 5 \ 2 \ 6]$. Por consiguiente, el siguiente nivel de entrada en el tiempo $t + 1$ puede ser -7 , $+1$, -3 o $+5$. Estos niveles de entrada siguientes corresponden a pares de bits decodificados (00), (10), (01) y (11), respectivamente.

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De forma similar, el decodificador externo (304) también encuentra la mejor métrica de trayectoria para el tiempo actual t para las respectivas cuadrículas. Una porción de esta cuadrícula se muestra en la Figura 21 para un decodificador externo ejemplar y se puede aplicar generalmente a todos los tres códigos de salida. Tal como se indica en la Figura 21, se seleccionan dos posibles pares de bits de entrada del decodificador externo para el tiempo $t + 1$ con base en el siguiente par posible de estados. A manera de ejemplo, los dos posibles pares de bits de entrada al decodificador externo pueden ser (10) o (01). El par de bits escogido por el decodificador externo (304) se envía a un mejorador de predicción (306) que selecciona niveles de amplitud +5 o -3 del el grupo de cuatro niveles previamente seleccionado por el predictor de secciones del decodificador interno (302) como la predicción de secciones mejorada para el tiempo $t + 1$. Considerando que la predicción de secciones del decodificador interno (302) tiene una demora cercana a cero, pero como el decodificador externo (304) solo puede operar sobre el mismo símbolo hasta después de que el decodificador interno (302) haya provisto una salida blanda decodificada, un módulo de demora (308) proporciona un tiempo de mora levemente mayor que el tiempo de demora del rastreo

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del decodificador interno (302). La predicción de secciones proporcionada por el mejorador de predicción (306) se puede proporcionar como retroalimentación a un ecualizador de rastreo de fase (310).

Con algún tiempo de demora adicional, el decodificador externo (304) puede tomar una decisión dura final y seleccionar un único par de bits de entrada más posible para el tiempo $t + 1$. Por ejemplo, si se encuentra que 11 es el par de bits de entrada más probable para el decodificador externo (304) según lo determinado por su Algoritmo Viterbi, esta información es enviada por el decodificador externo (304) al mejorador de predicción (306) que entonces elige +5 de un conjunto de cuatro niveles y pares de bits correspondientes ya seleccionados por el predictor de secciones del decodificador interno (302). El código externo puede ser un código convolucional u otro tipo de código de corrección de error. El mejorador de predicción (306) es inhabilitado durante los períodos de tiempo cuando los datos ATSC están siendo recibidos.

 Una retroalimentación del sistema mejorado de predicción de secciones (320) del estimador de secuencias posibles máximas (MLSE) utiliza un algoritmo Viterbi tal como se

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muestra en la Figura 22 junto con otras partes relevantes de un receptor RVSB. La retroalimentación del sistema mejorado de predicción de secciones MLSE (320) tiene un decodificador interno (322) y un decodificador externo (324) que opera de forma similar al decodificador interno (302) y al decodificador externo (304) arriba descritos. Sin embargo, en lugar de utilizar la salida de predicción de secciones del decodificador interno (302), se configura un módulo MLSE mejorado (326) para ejecutar el Algoritmo Viterbi usual sobre la señal recibida mediante la operación de cuadrículas de código con tasa de 2/3 de ocho estados (las mismas cuadrículas utilizadas por el decodificador interno (322), incluyendo el precodificador).

El módulo MLSE mejorado (326) selecciona su siguiente entrada, bien sea (i) la señal recibida de nivel ocho ruidoso demorada por un módulo de demora (328) si la siguiente entrada es un símbolo no RVSB, o (ii) la salida de decisión de pares de bits del decodificador externo (324) (duro y blando) si la siguiente entrada es un símbolo RVSB. El módulo MLSE mejorado (326) realiza esta selección de acuerdo con la información de símbolo por símbolo en el mapa RVSB.

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El módulo MLSE mejorado (326) saca uno de ocho símbolos posibles como su predicción de secciones, y esta predicción de secciones (decisión de símbolo) es provista por el módulo MLSE mejorado (326) como retroalimentación a un ecualizador o a un rastreador de fase (330).

El módulo MLSE mejorado (326) debería seguir una trayectoria más correcta a través de la cuadrícula de ocho estados que la que sigue el codificador interno (322) porque el módulo MLSE mejorado (326) obtiene entradas más confiables del decodificador externo (324) cuando un símbolo RVSB está disponible.

La salida del módulo MLSE mejorado (326) puede ser una decisión de sección dura o de nivel blando. También, cualquier indicación de confiabilidad del símbolo del decodificador interno (322) o del decodificador externo (324) se puede utilizar para cambiar el tamaño del paso del algoritmo LMS del ecualizador. (Ver la Guía para la Utilización de la Norma A/54 para Televisión Digital ATSC).

Una secuencia opcional de instrucción codificado predeterminado puede incluirse en una porción especificada del primer segmento RVSB de un campo de datos. Esta secuencia es conocida por adelantado tanto por el transmisor como por

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el receptor. Durante el tiempo en que la secuencia de instrucción decodificada sale del decodificador externo (324), la entrada al módulo MLSE mejorado (326) se conmuta a una versión almacenado de la secuencia de instrucción decodificada.

Algunas modificaciones del presente invento han sido discutidas arriba. Otras modificaciones se les ocurrirán a aquellos que practiquen la técnica del presente invento. Por ejemplo, aunque el receptor estándar ATSC (12) y el receptor VSB robusto (14) se muestra arriba como receptores separados, las funciones del receptor estándar ATSC (12) y del receptor VSB robusto (14) pueden combinarse en dos trayectorias de datos de un mismo receptor capaz de decodificar ambos tipos de datos (datos ATSC y datos VSB robustos).

De conformidad con lo anterior, la descripción del presente invento debe interpretarse únicamente de forma ilustrativa solamente y con el propósito de enseñar a aquellos que conocen la técnica la mejor manera de implementar el invento. Los detalles pueden variar sustancialmente sin apartarse del espíritu del invento y se reserva el uso exclusivo de todas las modificaciones que estén dentro del alcance de las reivindicaciones anexas.

REIVINDICACIONES

1. Un método para proporcionar predicción mejorada de secciones, el cual se CARACTERIZA por los siguientes pasos:

recibir una entrada que contiene los primeros y los segundos datos, en donde los primeros y los segundos datos tienen la misma constelación de nivel n y diferentes tasas de bits;

decodificar únicamente los segundos datos con un decodificador;

producir una salida en respuesta a la entrada y al decodificador, en donde la salida se confina a por lo menos uno pero menos de $n/2$ de los niveles de constelación n , y en donde $n > 2$; y

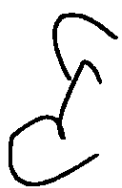
proporcionar la salida como la predicción mejorada de secciones.

2. El método de la reivindicación 1 en donde el decodificador es un primer decodificador, y en donde el paso de recepción incluye el paso de decodificar la entrada con un

segundo decodificador para recuperar los primeros y los segundos datos, en donde el segundo decodificador tiene n estados, y el paso de producción incluye el paso de elegir $n/4$ estados de $n/2$ estados de los n estados del segundo decodificador y en donde el paso de suministro comprende el paso de proporcionar los estados $n/4$ como la predicción mejorada de secciones.

3. El método de la reivindicación 2 que comprende además el paso de demorar el paso de elección con base en un tiempo de procesamiento del segundo decodificador.

4. El método de la reivindicación 1 en donde el decodificador es un primer decodificador y en donde el paso receptor comprende el paso de decodificar la entrada con segundo decodificador para recuperar los primeros y los segundos datos y en donde el segundo decodificador tiene estados n y el paso de producción incluye el paso de elegir únicamente un estado entre los estados $n/2$ de los estados n del segundo decodificador y en donde el paso de suministro comprende el paso de proporcionar un estado como una predicción mejorada de secciones.



~~147~~ 147

5. El método de la reivindicación 4 que comprende además el paso de demorar el paso de elección con base en un tiempo de procesamiento del segundo decodificador.



6. El método de las reivindicaciones 1, 2, 3, 4 o 5 en el que n es ocho.

7. El método de la reivindicación 1 en donde el paso de producción comprende los siguientes pasos:

decodificar la entrada cuando los segundos datos no están disponibles para así producir la salida; y,

decodificar los segundos datos cuando estos están disponibles para producir la salida.

8. El método de la reivindicación 7 que comprende además el paso de demorar la decodificación de la entrada con base al menos en parte en un tiempo de procesamiento del decodificador.

9. El método de la reivindicación 7 en donde el paso de suministro comprende el suministrar únicamente un estado como la predicción mejorada de secciones.

10. El método de la reivindicación 7 que comprende además el paso de seleccionar entre decodificar la entrada y los segundos datos en respuesta a un mapa recibido.

11. El método de la reivindicación 1 en donde el decodificador es un primer decodificador, en el que el paso de recepción comprende el paso de decodificar la entrada con un segundo decodificador para recuperar los primeros y los segundos datos y en donde el paso de decodificar únicamente los segundos datos incluye el paso de decodificar los segundos datos con el primer decodificador para producir dichos segundos datos decodificados y en donde el paso de producción comprende los siguientes pasos:

producir la salida mediante la decodificación de la entrada con un tercer decodificador cuando los segundos datos decodificados no estén disponibles; y

producir la salida mediante la decodificación de los segundos datos decodificados con un tercer decodificador cuando los segundos datos decodificados están disponibles.

12. El método de la reivindicación 11 que comprende además el paso de demorar el paso de decodificar la entrada con el tercer decodificador.

13. El método de la reivindicación 11 en donde el tercer decodificador implementa un algoritmo Viterbi.

14. El método de la reivindicación 11 en donde el paso de suministro comprende el paso de proporcionar únicamente un estado del tercer decodificador como la predicción mejorada de secciones.

15. El método de la reivindicación 11 que comprende además el paso de seleccionar entre decodificar la entrada y los segundos datos decodificados en respuesta a un mapa recibido.

16. El método de las reivindicaciones 7 u 11 en donde los primeros datos comprenden símbolos no-RVSB de ocho niveles y en donde los segundos datos incluyen símbolos de RVSB de ocho niveles.

17. El método de las reivindicaciones 1, 7 u 11 en donde el paso de suministro incluye el paso de suministrar la predicción mejorada de secciones con base en una señal de instrucción conocida cuando una señal de instrucción transmitida está contenida en una señal recibida.

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19. El método de la reivindicación 1 que comprende además el paso de suministrar la predicción mejorada de secciones como retroalimentación a un rastreador de fase.

La predicción mejorada de secciones está basada en datos VSB 8 ATSC cuando los datos VSB 8 robustos no están disponibles y está basada en datos VSB 8 cuando los datos VSB 8 robustos están disponibles.

María del Pilar Iglesias
C. C. 41.339.183 de Bogotá
Intérprete Oficial según Resolución No. 819 del
15 de Abril de 1971 del Ministerio de Justicia

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PATENT COOPERATION TREATY

From the RECEIVING OFFICE

PCT

NOTIFICATION OF THE INTERNATIONAL
APPLICATION NUMBER AND OF THE
INTERNATIONAL FILING DATE

(PCT Rule 20.5(c))

To:

TREVOR B. JOIKE
MARSHALL, O'TOOLE, GERSTEIN,
MURRAY & BORUN
6300 SEARS TOWER; 233 S. WACKER DRIVE
CHICAGO IL 60606Date of mailing
(day/month/year)

24 APR 2001

Applicant's or agent's file reference
29471/37034

IMPORTANT NOTIFICATION

International application No.

PCT/US01/09734

International filing date (day/month/year)

27 MAR 01

Priority date (day/month/year)

18 APR 00

Applicant ZENITH ELECTRONICS CORPORATION

Title of the Invention ENHANCED SLICE PREDICTION FEEDBACK

1. The applicant is hereby notified that the international application has been accorded the international application number and the international filing date indicated above.

2. The applicant is further notified that the record copy of the international application:



was transmitted to the International Bureau on

24 APR 2001



has not yet been transmitted to the International Bureau for the reason indicated below and a copy of this notification has been sent to the International Bureau*:



because the necessary national security clearance has not yet been obtained.



because (reason to be specified):

* The International Bureau monitors the transmittal of the record copy by the receiving Office and will notify the applicant (with Form PCT/IB/301) of its receipt. Should the record copy not have been received by the expiration of 14 months from the priority date, the International Bureau will notify the applicant (Rule 22.1(c)).

3. FOREIGN TRANSMITTAL LICENSE INFORMATION

Completed by: P. J. Jones

Additional license for foreign transmittal not required. This subject matter is covered by a license already granted on the equivalent U.S. national application. Refer to that license for information concerning its scope.



License for foreign transmittal not required. 37 CFR 5.11(e)(1) or 37 CFR 5.11(e)(2). However, a license may be required for additional subject matter. See 37 CFR 5.15(b).



Foreign transmittal license granted. 35 U.S.C. 184; 37 CFR 5.11 on

April 10, 01
(date)

37 CFR 5.15(a)



37 CFR 5.15(b)

Name and mailing address of the receiving Office

Assistant Commissioner for Patents
Box PCT
Washington, D.C. 20231

Attn: RO/US

Facsimile No.

Authorized Signature

PCT Section - IAPD Team 1

Tel: 202-305-5230 (FAX)

Telephone No.

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

152
152

To:

TREVOR B. JOIKE
MARSHALL. O'TOOLE. GERSTEIN.
MURRAY & BORUN
6300 SEARS TOWER: 233 S. WACKER DRIVE
CHICAGO IL 60606

PCT

INVITATION TO CORRECT DEFECTS IN THE INTERNATIONAL APPLICATION

(PCT Articles 3(4)(i) and 14(1) and Rule 26)

Applicant's or agent's file reference 29471/37034	Date of mailing (day/month/year) 24 APR 2001
International application No. PCT/US01/09734	REPLY DUE within ONE MONTH from the above date of mailing International filing date (day/month/year) 27 MAR 01
Applicant ZENITH ELECTRONICS CORPORATION	
Docketed: <u>15/2401</u>	

1. ☒ The applicant is hereby invited, within the time limit indicated above, to correct, in the international application as filed, the defects specified on the attached
- ☒ Annex A
 - ☐ Annex B1 (text matter of the international application as filed)
 - ☐ Annex C1 (drawings of the international application as filed)
2. ☐ The applicant is hereby invited, within the time limit indicated above, to correct, in the translation of the international application furnished under Rule 12.3, the defects specified on the attached
- ☐ Annex A
 - ☐ Annex B2 (text matter of the translation of the international application)
 - ☐ Annex C2 (drawings of the translation of the international application)

Additional observations (if necessary):

HOW TO CORRECT THE DEFECTS?

Correction must be submitted by filing a replacement sheet embodying the correction and a letter accompanying the replacement sheet, which shall draw attention to the difference between the replaced sheet and the replacement sheet. A correction may be stated in a letter only if it is of such a nature that it can be transferred from the letter to the record copy without adversely affecting the clarity and direct reproducibility of the sheet onto which the correction is to be transferred (Rule 26.4).

ATTENTION

Failure to correct the defects will result in the international application being considered withdrawn by this receiving Office (see Rule 26.5 for further details).

A copy of this invitation and any attachments has been sent to the International Bureau
☒ and the International Searching Authority.

Name and mailing address of the receiving Office Assistant Commissioner for Patents Box PCT Washington, D.C. 20231 Facsimile No.	Authorized officer Barbara Fiddle PCT Operations - IAPD Team 1 (703) 305-6747 (703) 305-6230 (FAX) Telephone No.
--	--

ANNEX A TO FORM PCT/RO/106

International application No.
PCT/US01/09734

The receiving Office has found the following defects in the international application as filed:

1. As to signature* of the international application (Rules 4.13 and 90.4), the request:

- a. ☐ is not signed.
- b. ☐ is not signed by all applicants.
- c. ☐ is not accompanied by the statement referred to in the check list in Box No. VIII of the request explaining the lack of the signature of an applicant for the designation of the United States of America.
- d. ☒ is signed by what appears to be an agent/common representative but
 - ☐ the international application is not accompanied by a power of attorney appointing him.
 - ☐ the power of attorney accompanying the international application was not signed by all the applicants.

☒ other (specify):

THE ADDRESS RECORDED ON THE POWER OF ATTORNEY SUBMITTED WITH THIS INTERNATIONAL APPLICATION FOR ZENTH ELECTRONICS CORPORATION IS NOT THE SAME AS THE ADDRESS RECORDED ON THE REQUEST. PLEASE CLARIFY.

* All applicants must sign, including inventors if they are also applicants (e.g. where the United States of America is designated).

2. As to indications concerning the applicant, the request (Rules 4.4 and 4.5):

- a. ☐ does not properly indicate the applicant's name (specify):
- b. ☐ does not indicate the applicant's address.
- c. ☐ does not properly indicate the applicant's address (specify):
- d. ☐ does not indicate the applicant's nationality.
- e. ☐ does not indicate the applicant's residence.
- f. ☐ other (specify):

3. As to the language of certain elements of the international application, other than the description and claims (Rules 12.1(c) and 26.3(a) and (c)):

- a. ☐ the request is not in a language which is both a language accepted by this receiving Office and a language of publication, which is (are):
- b. ☐ the text matter of the drawings is not in the language in which the international application is to be published, which is:
- c. ☐ the abstract is not in the language in which the international application is to be published, which is:

4. The title of the invention:

- a. ☐ is not indicated in Box No. I of the request (Rule 4.1(a)).
- b. ☐ is not indicated at the top of the first sheet of the description (Rule 5.1(a)).
- c. ☐ as appearing in Box No. I of the request is not identical with the title heading the description (Rule 5.1(a)).

5. As to the abstract (Rule 8):

- ☐ the international application does not contain an abstract.

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

PCT

NOTIFICATION REGARDING CERTAIN
CORRECTIONS MADE *EX OFFICIO*

(PCT Administrative Instructions, Section 327)

To:

TREVOR B. JOIKE
MARSHALL, O'TOOLE, GERSTEIN,
MURRAY & BORUN
6300 SEARS TOWER: 233 S. WACKER DRIVE
CHICAGO IL 60606Date of mailing
(day/month/year) 24 APR 2001Applicant's or agent's file reference
29471/37034REPLY DUE
NONE
However, see paragraph 3 belowInternational application No.
PCT/US01/09734International filing date
(day/month/year) 27 MAR 01Applicant
ZENITH ELECTRONICS CORPORATION

1. The applicant is hereby notified that this receiving Office has corrected formal defects in the international application *ex officio*, as shown on the attached copy of:

- ☒ the request, sheet No.: 4
☐ the description, sheet No.:
☐ the claims, sheet No.:
☐ the drawings, sheet No.:
☐ other (specify):

2. If the applicant agrees with these corrections, no further action is required in this regard.

3. In case of disagreement with these corrections, the applicant should promptly inform this receiving Office accordingly.

Name and mailing address of the receiving Office
Assistant Commissioner for Patents
Box PCT
Washington, D.C. 20231

Attn: RO/US

Facsimile No.

Authorized Signature

ST Operations - IAPD Team 1
303-2230 (FAX)

Telephone No.

15

PCT/US 01/09734

Sheet No. 4....

Supplemental Box If the Supplemental Box is not used, this sheet need not be included in the request.

1. If, in any of the Boxes, the space is insufficient to furnish all the information: in such case, write "Continuation of Box No. ..." [Indicate the number of the Box] and furnish the information in the same manner as required according to the captions of the Box in which the space was insufficient, in particular:
- (i) If more than two persons are involved as applicants and/or inventors and no "continuation sheet" is available: in such case, write "Continuation of Box No. III" and indicate for each additional person the same type of information as required in Box No. III. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below;
 - (ii) If, in Box No. II or in any of the sub-boxes of Box No. III, the indication "the States indicated in the Supplemental Box" is checked: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the applicant(s) involved and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is applicant;
 - (iii) If, in Box No. II or in any of the sub-boxes of Box No. III, the inventor or the inventor/applicant is not inventor for the purposes of all designated States or for the purposes of the United States of America: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the inventor(s) and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is inventor;
 - (iv) If, in addition to the agent(s) indicated in Box IV, there are further agents: in such case, write "Continuation of Box No. IV" and indicate for each further agent the same type of information as required in Box No. IV;
 - (v) If, in Box No. V, the name of any State (or OAPI) is accompanied by the indication "parent of addition," or "certificate of addition," or if, in Box No. V, the name of the United States of America is accompanied by an indication "continuation" or "continuation-in-part": in such case, write "Continuation of Box No. V" and the name of each State involved (or OAPI), and after the name of each such State (or OAPI), the number of the parent title or parent application and the date of grant of the parent title or filing of the parent application;
 - (vi) If, in Box No. VI, there are more than three earlier applications whose priority is claimed: in such case, write "Continuation of Box No. VI" and indicate for each additional earlier application the same type of information as required in Box No. VI;
 - (vii) If, in Box No. VI, the earlier application is an ARIPO application: in such case, write "Continuation of Box No. VI", specify the number of the item corresponding to that earlier application and indicate at least one country party to the Paris Convention for the Protection of Industrial Property or one Member of the World Trade Organization for which that earlier application was filed.
2. If, with regard to the precautionary designation statement contained in Box No. V, the applicant wishes to exclude any State(s) from the scope of that statement: in such case, write "Designation(s) excluded from precautionary designation statement" and indicate the name or two-letter code of each State so excluded.
3. If the applicant claims, in respect of any designated Office, the benefits of provisions of the national law concerning non-prejudicial disclosures or exceptions to lack of novelty: in such case, write "Statement concerning non-prejudicial disclosures or exceptions to lack of novelty" and furnish that statement below.

Continuation of Box VI ▲
13 March 2001 09/804237 US
(13.03.01) Unassigned

▲ PCT/US

TRANSMITTAL LETTER TO THE UNITED STATES RECEIVING OFFICE

Date	May 17, 2001
International Application No.	PCT/US01/08734
Attorney Docket No.	29471/37034

I. Certification under 37 CFR 1.10 (if applicable)

EK857823337US
Express Mail mailing number

May 17, 2001
Date of Deposit

I hereby certify that the application/correspondence attached hereto is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature of person mailing correspondence

Richard Zimmermann
Typed or printed name of person mailing correspondence

II. ☐ New International Application

TITLE	
-------	--

Earliest priority date (Day/Month/Year)

SCREENING DISCLOSURE INFORMATION: In order to assist in screening the accompanying international application for purposes of determining whether a license for foreign transmittal should and could be granted and for other purposes, the following information is supplied. (Note: check as many boxes as apply):

- A. ☐ The invention disclosed was not made in the United States.
- B. ☐ There is no prior U.S. application relating to this invention.
- C. ☐ The following prior U.S. application(s) contain subject matter which is related to the invention disclosed in the attached international application. (NOTE: priority to these applications may or may not be claimed on form PCT/RO/101 (Request) and this listing does not constitute a claim for priority).

application no.		filed on	
application no.		filed on	

- D. ☐ The present international application ☐ is identical ☐ contains less subject matter than that found in the prior U.S. application(s) identified in paragraph C.
- E. ☐ The present international application ☐ contains additional subject matter not found in the prior U.S. application(s) identified in paragraph C. above. The additional subject matter is found on pages and ☐ DOES NOT ALTER ☐ MIGHT BE CONSIDERED TO ALTER the general nature of the invention in a manner which would require the U.S. application to have been made available for inspection by the appropriate defense agencies under 35 U.S.C. 181 and 37 CFR 5.1. See 37 CFR 5.15

III. ☒ A Response to an Invitation from the RO/US. The following document(s) is (are) enclosed:

- A. ☐ A Request for An Extension of Time to File a Response
- B. ☐ A Power of Attorney (General or Regular)
- C. ☐ Replacement pages:

pages		of the request (PCT/RO/101)	pages		of the figures
pages		of the description	pages		of the abstract
pages		of the claims			

- D. ☐ Submission of Priority Documents

Priority document		Priority document	
-------------------	--	-------------------	--

- E. ☐ Fees as specified on attached Fee Calculation sheet form PCT/RO/101 annex

IV. ☐ A Request for Rectification under PCT 91 ☐ A Petition ☐ A Sequence Listing Diskette

V. ☐ Other (please specify):

The person signing this form is the:	☐ Applicant	Traver B. Jolke
	☒ Attorney/Agent (Reg. No.) 25,542	Typed name of signer
	☐ Common Representative	Signature

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (RO/US)

In the matter of:)
)
International Pat. Appl. No.: PCT/US01/09734)
)
International Filing)
Date: 27 March 2001)
)
Title: Enhanced Slice Prediction Feedback)
)
Applicant:)
Zenith Electronics Corporation)
)
Attorney Docket No.:)
29471/37034)
)

Response to Invitation to Correct Defects

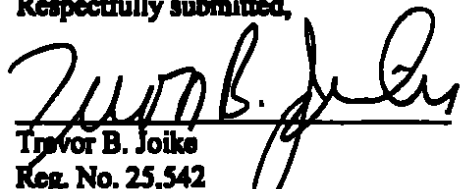
Commissioner of Patents
Box PCT
Washington, D.C. 20231

This paper is in response to the Invitation to Correct Defects dated April 24, 2001.

Officer Fridie has identified a discrepancy in Applicant's address identified in the general power of attorney and Applicant's address identified in the Request. Zenith Electronics Corporation recently moved to 2000 Millbrook Drive, Lincolnshire, Illinois 60069. The address identified in the Request is Applicant's current address.

Should the Examining Attorney have any additional questions, she is urged to contact the undersigned at the indicated number.

Respectfully submitted,


Trevor B. Joike
Reg. No. 25,542
MARSHALL, OTOOLE, GERSTEIN
MURRAY & BORUN
Attorney for Applicant
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
(312) 474-6300

Dated: May 17, 2001

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

To:
TREVOR B. JOIKE
MARSHALL, OTOOLE, GERSTEIN,
MURRAY & BORUN
6300 SEARS TOWER; 233 S. WACKER DRIVE
CHICAGO, IL 60606

PCT

RECEIVED
JUN 27 2001
MARSHALL, OTOOLE, GERSTEIN, MURRAY & BORUN

COMMUNICATION IN CASES FOR WHICH
NO OTHER FORM IS APPLICABLE

Date of mailing
(day/month/year) **20 JUN 2001**

Applicant's or agent's file reference
29471/37034

REPLY DUE
See paragraph 1 below

International application No.
PCT/US01/09734

International filing date
(day/month/year) **27 MAR 01**

Applicant
ZENITH ELECTRONICS CORPORATION

1. ☐ REPLY DUE within _____ months/days from the above date of mailing
- ☐ NO REPLY DUE, however, see below _____
- ☒ IMPORTANT COMMUNICATION
- ☐ INFORMATION ONLY

2. COMMUNICATION:
THE RECEIVING OFFICE ACKNOWLEDGE THE RECEIPT OF A RESPONSE TO INVITATION TO CORRECT DEFECTS DATED 17 MAY 2001, HOWEVER THE ADDRESS RECORDED ON THE REQUEST FOR ZENITH ELECTRONICS CORPORATION MUST BE THE SAME AS THE ADDRESS RECORDED ON THE POWER OF ATTORNEY. THE PCT/RO/108 REMAIN OUTSTANDING.

Name and mailing address of the receiving Office
Assistant Commissioner for Patents
Box PCT
Washington, D.C. 20231 Am:RO/US
Facsimile No. 703-305-3230

Authorized officer
Barbara Fridie *BF*
Telephone No. 703-305-3747

[Handwritten scribble]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (RO/US)

In the matter of:)
)
International Pat. Appl. No.: PCT/US01/09734)
)
International Filing)
Date: 27 March 2001)
)
Title: Enhanced Slice Prediction Feedback)
)
Applicant:)
Zenith Electronics Corporation)
)
Attorney Docket No.:)
29471/37034)
)

Response to Invitation to Correct Defects

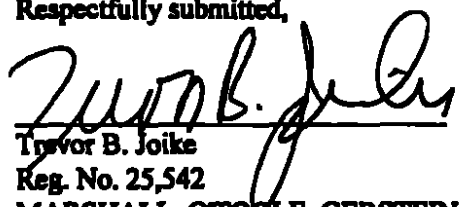
Commissioner of Patents
Box PCT
Washington, D.C. 20231

This paper is in response to the Invitation to Correct Defects dated April 24, 2001.

Officer Fridie has identified a discrepancy in Applicant's address identified in the general power of attorney and Applicant's address identified in the Request. Zenith Electronics Corporation recently moved to 2000 Millbrook Drive, Lincolnshire, Illinois 60069. The address identified in the Request is Applicant's current address.

Should the Examining Attorney have any additional questions, she is urged to contact the undersigned at the indicated number.

Respectfully submitted,

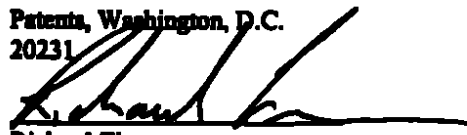


Trevor B. Joike
Reg. No. 25,542
MARSHALL, OTOOLE, GERSTEIN
MURRAY & BORUN
Attorney for Applicant
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
(312) 474-6300

Dated: May 17, 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (RO/US)

In the matter of:	)	CERTIFICATE OF MAILING
	)	BY EXPRESS MAIL
International Pat. Appl. No.: PCT/US01/09734	)	"EXPRESS MAIL" mailing
	)	label
International Filing	)	No. EK657823558US
Date: 27 March 2001	)	Date of Deposit: July 19, 2001
	)	
Title: ENHANCED SLICE PREDICTION	)	I hereby certify that this paper
FEEDBACK	)	and the documents referred to
	)	herein as enclosed herewith are
	)	being deposited with the United
Applicant:	)	States Postal Service
Zenith Electronics Corporation	)	"EXPRESS MAIL POST
	)	OFFICE TO ADDRESSEE"
	)	service under 37 C.F.R. §1.10
Attorney Docket No.:	)	on the date indicated above and
29471/37034	)	are addressed to Box PCT,
	)	Assistant Commissioner for
	)	Patents, Washington, D.C.
	)	20231
	)	
	)	Richard Zimmermann

Response to Communication

Commissioner of Patents
Box PCT
Washington, D.C. 20231
ATTN: Barbara Fridie

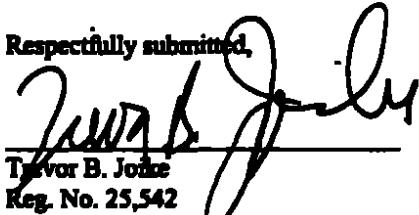
Fax: 703/305-3230

This paper is in response to the Communication dated 20 June 2001.

Enclosed is a general appointment of agent from Zenith Electronics Corporation in the undersigned's favor. The applicant's address identified in the power of attorney corresponds with the address identified in the Request.

Should the Examining Attorney have any additional questions, she is urged to contact the undersigned at the indicated number.

Respectfully submitted,


Trevor B. Joice
Reg. No. 25,542
MARSHALL, O'TOOLE, GERSTEIN
MURRAY & BORUN
Attorney for Applicant
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
(312) 474-6300

Dated: July 19, 2001

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PCT

GENERAL POWER OF ATTORNEY

(for several international applications filed under the Patent Cooperation Treaty)

(PCT Rule 90.5)

The undersigned person(s):

(Family name followed by given name; for a full legal entity, full official designation. The address must include postal code and name of country.)

ZENITH ELECTRONICS CORPORATION
2000 Millbrook Drive
Lincolnshire, Illinois 60069
United States of America

hereby appoint(s) the following person as:

☒ agent

☐ common representative

Name and address

(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)

JOIKE, Trevor B. and HEPPERMAN, Roger A.
MARSHALL, OTOOLE, GERSTEIN, MURRAY & BORUN
6300 Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
United States of America

to represent the undersigned before

☒ all the competent International Authorities

☐ the International Searching Authority only

☐ the International Preliminary Examining Authority only

in connection with any and all international applications filed by the undersigned with the following Office

United States Patent and Trademark Office

as receiving Office

and to make or receive payments on behalf of the undersigned.

Signature(s) (where there are several persons, each of them must sign; next to each signature, indicate the name of the person signing and the capacity in which the person signs, if such capacity is not obvious from reading this power):

By:

Name:

Title:

Jack Kall

Assistant Secretary

Date:

June 15, 2001

TRATADO DE COOPERACIÓN PARA PATENTES

162

De la OFICINA RECEPTORA

Para: TREVOR B. JOIKE
MARSHALL O'TOOLE, GERSTEIN, MURRAY & BORUN
6300 SEARS TOWER: 233 S. WACKER DRIVE
CHICAGO, IL 60606

PCT

NOTIFICACIÓN DEL NÚMERO DE SOLICITUD INTERNACIONAL Y DE LA
FECHA DE PRESENTACIÓN INTERNACIONAL

(Regla 20.5(c) del PCT)

Fecha de porte al correo: 24 de abril de 2001

Referencia del archivo del solicitante o del agente:

29471/37034

Solicitud Internacional: PCT/US01/09734
Fecha de presentación internacional: 27 de marzo de 2001
Fecha de prioridad: 18 de abril de 2000
Solicitante: ZENITH ELECTRONICS CORPORATION

Título del invento:

RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

1. Se notifica al solicitante que a la solicitud internacional se le asignó un número y una fecha de presentación internacional según lo arriba indicado.

M. P. Iphigene
Jefe del Párrafo Iphigene
SECCIÓN I
SECCIÓN OFICIAL
Washington D.C. 20540

150

Nombre y dirección de la Oficina receptora:

Comisario Asistente de Patentes
Box PCT
Washington D.C. 20231

Atención RO/US

(Fdo.) Ilegible

La página que sigue trae los mismos datos y además dice:

☒ Al solicitante se le invita dentro del límite arriba indicado a corregir en la solicitud internacional tal como se presentó, los defectos indicados en:

☒ El Anexo A

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TRATADO DE COOPERACIÓN PARA PATENTES

De la OFICINA RECEPTORA

Para: TREVOR B. JOIKE
MARSHALL O'TOOLE, GERSTEIN, MURRAY & BORUN
6300 SEARS TOWER: 233 S. WACKER DRIVE
CHICAGO, IL 60606

PCT

**NOTIFICACIÓN DEL NÚMERO DE SOLICITUD INTERNACIONAL Y DE LA
FECHA DE PRESENTACIÓN INTERNACIONAL**

(Regla 20.5(c) del PCT)

Fecha de porte al correo: 24 de abril de 2001

Referencia del archivo del solicitante o del agente:

29471/37034

Solicitud Internacional: PCT/US01/09734
Fecha de presentación internacional: 27 de marzo de 2001
Fecha de prioridad: 18 de abril de 2000
Solicitante: ZENITH ELECTRONICS CORPORATION

Título del invento:

RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

1. Se notifica al solicitante que a la solicitud internacional se le asignó un número y una fecha de presentación internacional según lo arriba indicado.

M.P. Iphigene
Marta del Pilar Iphigene
ENCUENCA I
SECRETARÍA
Boulevard No. 579, Guatemala

750



2. Al solicitante se le notifica además que la copia del registro de la solicitud internacional:

☒ Se transmitió a la Oficina internacional el 24 de abril de 2001

3. INFORMACIÓN SOBRE LA TRANSFERENCIA EXTRANJERA DE LA LICENCIA

☒ Se otorgó licencia para transferencia extranjera.
35 U.S.C. 184; 37 CFR 5.11 el 10 de abril de 2001

☒ 37 CFR 5.15(a)

Nombre y dirección de la Oficina receptora:

Comisario Asistente de Patentes

Box PCT

Washington D.C. 20231

Atención RO/US

(Fdo.) Ilegible

La página que sigue trae los mismos datos y además dice:

☒ Al solicitante se le invita dentro del límite arriba indicado a corregir en la solicitud internacional tal como se presentó, los defectos indicados en:

☒ El Anexo A

Se envió una copia de esta invitación a la Oficina Internacional y a la Autoridad de Búsqueda Internacional.

(Fdo.) Ilegible

La Oficina receptora ha encontrado los siguientes defectos en la solicitud internacional que se presentó:

D. ☒ Está firmada por lo que parece ser un agente/representante común pero

LA DIRECCIÓN REGISTRADA EN EL PODER PRESENTADO CON ESTA SOLICITUD INTERNACIONAL PARA ZENITH ELECTRONICS CORPORATION NO ES LA MISMA DIRECCIÓN REGISTRADA EN LA SOLICITUD. FAVOR ACLARAR.

La página que sigue trae la misma información y además dice:

Al solicitante se le notifica que esta Oficina receptora corrigió los defectos formales en la solicitud internacional exoficio que aparecen en la copia adjunta de la solicitud, página No. 4.

En caso de no estar de acuerdo con estas correcciones, el solicitante debe informar prontamente a esta Oficina receptora.

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En seguida viene la hoja No. 4 donde la corrección aparece así:

Continuación de la Casilla VI

13 de marzo de 2001 09/804.237 Estados Unidos
(13.03.0)

CARTA DE TRANSMISIÓN A LA OFICINA RECEPTORA DE
LOS ESTADOS UNIDOS

Fecha: 17 de mayo de 2001

Solicitud Internacional No.: PCT/US01/09734

Expediente de Abogado No.: 29471/37034

I. Certificación conforme al 37 CFR 1.10 (si aplica)

<u>EK657823337US</u>	<u>17 de mayo de 2001</u>
No. del porte en el Correo por Expreso	Fecha del Depósito

Certifico que la solicitud/correspondencia aquí adjunta está siendo depositada en la Oficina de Correo Expreso del "Servicio Postal de los Estados Unidos" conforme al 37 CFR 1.10 en la fecha arriba indicada y está dirigida al Comisario Asistente de Patentes, Washington, D.C. 20231.

(Fdo.) Richard Zimmermann



III. ☒ Respuesta a una Invitación del RO/US

(Fdo.) Trevor B Joiker

Apoderado/Agente con Registro No. 25.542

OFICINA DE MARCAS Y PATENTES DE LOS ESTADOS UNIDOS (RO/US)

Con relación a la Solicitud Internacional de Patente No.

PCT/US01/09734

Fecha de Presentación Internacional: 27 de marzo de 2001

Título:

Retroalimentación de la Predicción Mejorada de Secciones

Solicitante: **Zenith Electronics Corporation**

Expediente No. **29471/37034**

Respuesta a una Invitación para Corregir Defectos

Comisario de Patentes
Box PTC
Washington, D.C. 20231

Este documento es en respuesta a la Invitación para Corregir Defectos fechada el 24 de abril de 2001.

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El funcionario Fridie ha identificado una discrepancia en la dirección identificada en el poder del Solicitante contra la dirección identificada en la Solicitud del mismo. Zenith Electronics Corporation recientemente se trasladó al 2000 Millbrook Drive, Lincolnshire, Illinois 60069. La dirección identificada en la Solicitud es la dirección actual del Solicitante.

Con agrado responderemos cualquier duda adicional.

Atentamente,

(Fdo.) Trevor B. Joike
Matrícula No. 25.542
MARHSALL, OTOOLE, GERSTEIN MURRAY & BORUN
Apoderado del Solicitante
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
(312) 474-6300

Fecha: 17 de mayo de 2001

Sigue acuse de recibo de la comunicación precedente.

Las 3 páginas siguientes se refieren también al cambio de dirección y al nombramiento general de Agente por parte de Zenith Electronics Corporation.

Maria del Pilar Iglesias
Maria del Pilar Iglesias

Maria del Pilar Iglesias
C. C. 41.339.183 de Bogotá 6
móstrate Oficial según Resolución No. 819 de
1971 del Ministerio de Justicia

PATENT COOPERATION TREATY

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From the INTERNATIONAL SEARCHING AUTHORITY

PCT

To:
MARSHALL O'TOOLE GERSTEIN
MURRAY & BORUN
Attn. Jolke, Trevor B.
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
UNITED STATES OF AMERICA

RECEIVED

MARSHALL GERSTEIN

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT
OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing
(day/month/year)

07/11/2001

Applicant's or agent's file reference

29471/37034

FOR FURTHER ACTION

See paragraphs 1 and 4 below

International application No.

PCT/US 01/09734

International filing date

(day/month/year)

27/03/2001

Applicant

ZENITH ELECTRONICS CORPORATION

1. ☒ The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 18:

The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 48):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Facsimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. ☐ With regard to the protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. Further action(s): The applicant is reminded of the following:

Shortly after 18 months from the priority date, the International application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the International application, or of the priority claim, must reach the International Bureau as provided in Rules 90bis.1 and 90bis.3, respectively, before the completion of the technical preparations for international publication.

Within 18 months from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within 20 months from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 18 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority



European Patent Office, P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3018

Authorized officer

Carina Bergström

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under Article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the PCT Applicant's Guide, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only.

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Administrative Instructions, Section 206(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/ may accompany the amendments?

Letter (Section 206(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

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[Signature]

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped), whether

- (i) the claim is unchanged;
- (ii) the claim is cancelled;
- (iii) the claim is new;
- (iv) the claim replaces one or more claims as filed;
- (v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."
2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."
3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."
4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 16 and 19 cancelled; claims 14, 15 and 18 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 48.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)".

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the same time of filing the amendments with the International Bureau, also file a copy of such amendments with the International Preliminary Examining Authority (see Rule 62.2(a), first sentence).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, where upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/selected Office, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/selected Office, see Volume II of the PCT Applicant's Guide.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 29471/37034	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/US 01/09734	International filing date (day/month/year) 27/03/2001	(Earliest) Priority Date (day/month/year) 18/04/2000
Applicant ZENITH ELECTRONICS CORPORATION		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

- a. With regard to the language, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

- b. With regard to any nucleotide and/or amino acid sequences disclosed in the international application, the international search was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

2. ☐ Certain claims were found unsearchable (See Box I).

3. ☐ Unity of invention is lacking (see Box II).

4. With regard to the title,

☐ the text is approved as submitted by the applicant.

☒ the text has been established by this Authority to read as follows:

METHOD OF MODULATION SELECTION AND DECODING

5. With regard to the abstract,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the drawings to be published with the abstract is Figure No.

☐ as suggested by the applicant.

☒ because the applicant failed to suggest a figure.

☐ because this figure better characterizes the invention.

1
☐ None of the figures.

INTERNATI NAL SEARCH REP RT

International Application No

PCT/US 01/09734

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04L27/02 H04L27/06 H04L25/06 H04N7/66 H04N7/52
H04N5/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04L H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 869 684 A (HEWLETT PACKARD CO) 7 October 1998 (1998-10-07) abstract column 1, line 38 - line 47 claim 1 figure 1	1
A		2-19
Y	US 5 923 711 A (WILLMING DAVID A) 13 July 1999 (1999-07-13) abstract column 1 column 2 claims 1,2 figure 4	1
A		2-19
	— — — — — -/-	

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents :

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

A document member of the same patent family

Date of the actual completion of the international search

30 October 2001

Date of mailing of the international search report

07/11/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patristaan 2
NL - 2280 HV Rijswijk
Tel (+31-70) 340-2040, Tx 31 651 epo nl
Fax (+31-70) 340-3016

Authorized officer

Reilly, D

INTERNATI NAL SEARCH REP RT

International Application No

PCT/US 01/09734

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 748 226 A (LIMBERG ALLEN LEROY) 5 May 1998 (1998-05-05) abstract column 1, line 1 - line 27 column 1, line 46 - line 61 column 4, line 65 -column 5, line 10 claim 1	1

Form PCTABR/210 (continuation of second sheet) (July 1998)

INTERNATIONAL SEARCH REP RT

Information on patent family members

International Application No

PCT/US 01/09734

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0869684	A	07-10-1998	US 6011868 A	04-01-2000
			EP 0869684 A2	07-10-1998
			JP 10285594 A	23-10-1998
US 5923711	A	13-07-1999	AU 2595597 A	22-10-1997
			BR 9702158 A	20-07-1999
			CA 2222029 A1	09-10-1997
			JP 11507194 T	22-06-1999
			WO 9737470 A1	09-10-1997
US 5748226	A	05-05-1998	CA 2220740 A1	12-05-1998
			US 5995135 A	30-11-1999

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TRATADO DE COOPERACIÓN DE PATENTES

De la AUTORIDAD DE BÚSQUEDA INTERNACIONAL:

Para: MARSHALL O'TOOLE, GERSTEIN, MURRAY & BORUN
Atención: Joike, Trevor B.
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
ESTADOS UNIDOS DE AMÉRICA

PCT

**NOTIFICACIÓN DE LA TRANSMISIÓN DEL INFORME DE
BÚSQUEDA INTERNACIONAL DE LA DECLARACIÓN (Regla 44 PCT)**

Fecha de porte al correo: 07/11/2001

Referencia del archivo del solicitante o del agente:

29471/37034

Solicitud Internacional No.: PCT/US 01/09734

Fecha de presentación internacional: 27/03/2001

Solicitante: **ZENITH ELECTRONICS CORPORATION**

1. ☒ Al solicitante por el presente se le notifica que se ha establecido el Reporte de Búsqueda Internacional y se transmite con este documento.

**Presentación de modificaciones y declaración conforme al
Artículo 19:**

El solicitante tiene derecho, si así lo desea, de
modificar las reivindicaciones de la Solicitud
Internacional (Ver Regla 46):

M. P. Iglesias.

María del Pilar Iglesias
ENCARGADA DE
ADMINISTRACIÓN
Sección de Búsqueda

¿Cuándo? El límite de tiempo para presentar esas modificaciones normalmente es de 2 meses contados a partir de la fecha de la transmisión del Reporte de Búsqueda Internacional; sin embargo, para más detalles ver las notas de la hoja adjunta.

¿Dónde? Directamente a: Oficina Internacional de la OMPI
 34, chemin des Colombettes
 1211 Ginebra 20, Suiza
 Fax No. (41-22) 740.14.35

Para más instrucciones detalladas, ver las notas de la hoja adjunta

Nota del traductor: vienen las instrucciones y más adelante aparece una casilla donde se indica que este Reporte de Búsqueda Internacional consiste de un total de tres (3) hojas y que esta Autoridad ha establecido que dicho reporte reza así:

MÉTODO DE SELECCIÓN DE ONDULACIÓN Y DECODIFICACIÓN

...

5. Con relación al resumen,

☒ El texto ha sido aprobado tal como fue presentado por el solicitante

...

6. La Figura No. 1 se ha de publicar con los dibujos del resumen,

☒ Porque el solicitante no sugirió una figura.

A. CLASIFICACIÓN DEL ASUNTO:

IPC 7 H04L27/02 H04L27/06 H04L25/06 H04N7/66 H04N7/52
 H04N5/00

B. ARCHIVO DE BÚSQUEDA:

Documentación mínima buscada (sistema de clasificación seguido por los símbolos de clasificación)

IPC 7 H04L H04N

Se consultó la base electrónica de datos durante la búsqueda internacional (nombre de la base de datos y, cuando sea práctico, indicar los términos de la búsqueda utilizados)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTOS QUE SE CONSIDERARON PERTINENTES

Categoría*	Citación del documento, indicando, cuando sea apropiado los pasajes pertinentes	Relacionado con la reivindicación No.
Y	EP 0 869 684 A (HEWLETT PACKARD CO) 7 de octubre de 1998 (1998-10-07) resumen columna 1, línea 38 - línea 47 reivindicaciones 1 figura 1	1
A	-----	2-19
Y	US 5 923 711 A (WILLMING DAVID A) 13 de Julio de 1999 (1999-07-13) resumen columna 1 columna 2 reivindicaciones 1, 2 figura 4	1
A	-----	2-19

[Handwritten signature] 178

Y	US 5 748 226 A (LIMBERG ALLEN LEROY) 5 de mayo de 1998 (1998-05-05) resumen columna 1, línea 1 - línea 27 columna 1, línea 46 - línea 61 columna 4, línea 65 - columna 5, línea 10 reivindicaciones 1	1
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- ☒ Los documentos adicionales se enumeran en la continuación de la casilla C.
- ☒ Los miembros de la familia de patentes se enumeran en el anexo

Fecha de la culminación de la búsqueda internacional:	Fecha del porte al correo del reporte de búsqueda internacional:
30 de octubre de 2001	07/11/2001

Nombre y dirección postal del ISA: Funcionario autorizado

Oficina Europea de Patentes, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel: (+31-70) 340-2040, Telex 31 651 epo nl, Fax: (+31-70) 340-3016	Reilly, D
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REPORTE DE BÚSQUEDA INTERNACIONAL

Información sobre los miembros de la familia de patentes

Solicitud Internacional No. PCT/US 01/09734					
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intérprete Oficial según Resolución No. 819 de

(19) Oficina de Patentes Europea

(11) EP 0 869 684 A2

(12) SOLICITUD DE PATENTE EUROPEA

(43) Fecha de Publicación (51) Int. Cl.6 H04N 17/00, H04N 7/50

179

07.10.1998 Boletín 1998/41

(21) Número de solicitud: 97121693.2

(22) Fecha de la solicitud: 09.12.1997

(84) Países Contratantes Designados AT BE CH DEDK ES FI FR GB GR IE IT LI LU MC NL PT SE Países designados por extensión AL LT LV MK RO SI (30) Prioridad: 04.04.1997 US 832624 (71) Solicitante: Hewlett-Packard Company Palo Alto, California 94034 (US) (72) Inventores: • Van Den Branden Lambrecht, Christian • Sunnyvale, Ca 94089 (US)	• Ong, Chong T. Richmond, British Columbia (CA) • Liu, Samson J. Menlo Park, Ca 94025 (US) • Leonard, Mark A. Richmond, British Columbia (CA) (74) Representante: Schoppe, Fritz, Dipl.-Ing. Schoppe & Zimmermann, Patentanwälte, Postfach 710867 81458 München (DE)
(54) Analizador de la calidad del flujo de bits (57) Un sistema de análisis de la calidad del flujo de bits incluye un desmultiplexor (180), un analizador de la calidad del flujo de bits (190), y una interfase para usuario gráfico (200). El desmultiplexor recibe un	exhibe los parámetros extractados, caracterizando el flujo de bits elemental del video. Un usuario puede monitorear el flujo de bits elemental del video a varios niveles de detalle y puede hacer análisis de calidad a distintos niveles en el flujo

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Los folios 179-249
no corresponden a la
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Junio 11/03. *llz.*

flujo de bits y separa del flujo de bits por lo menos un flujo elemental que incluye un flujo de bits elemental del video. El analizador de la calidad del flujo de bits recibe el flujo de bits elemental del video del desmultiplexor y fractura el flujo de bits elemental del video para extraer parámetros que caracterizan el flujo de bits elemental del video. El analizador de calidad del flujo de bits suministra los parámetros extractados a la interfase del usuario gráfico, que	de bits elemental del video. Dependiendo del nivel del monitoreo y del análisis de calidad seleccionado por el usuario, el analizador de calidad del flujo de bits provee información sobre el uso del dispositivo separador y la eficiencia de codificación y puede predecir la calidad de la secuencia del video completamente descodificada, sin descodificar totalmente el flujo de bits del video elemental y sin usar la secuencia del video original.
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FIGURA 5
(VER DIBUJO)

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Descripción ANTECEDENTES DEL INVENTO 1. Campo del Invento El presente invento está dirigido hacia métodos y aparatos de monitoreo y análisis del flujo de bits de un video. Más particularmente, el presente invento está dirigido hacia métodos y aparatos para monitorear un flujo de bits del video MPEG a varios niveles de detalle, basado en el nivel de monitoreo y	codificados MPEG-1. El MPEG-2 puede también manejar videos entrelazados y soporta la sintaxis escalable, que permite a un codificador crear capas de mejoramiento que pueden aumentar la calidad y la resolución espacial y temporal de la película. Tal posibilidad de escalación es muy útil en aplicaciones de video utilizadas en telecomunicaciones, servicio de video con cualidades múltiples, video en redes de
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análisis seleccionado por el usuario. Los niveles de monitoreo y análisis incluyen monitoreo de varias características y atributos del flujo de bits del video MPEG, prueba de funcionamiento de MPEG y decodificación en tiempo real, y predicción de la calidad visual de las secuencias descomprimadas del video contenidas en el flujo de bits del video MPEG.	cajeros automáticos y HDTV. La Figura 1 ilustra un decodificador MPEG convencional (el término MPEG es usado para denotar MPEG-1 ó MPEG-2, a menos que se especifique lo contrario). El decodificador (5) incluye un sistema decodificador (10) que fractura el flujo de bits MPEG y alimenta separadamente los flujos de bits de audio y video (conteniendo información comprimida de audio y video), junto con información de tiempo, a un decodificador de audio (15) y decodificador de video (20). Los decodificadores de audio y video (15), (20) descodifican entonces sus flujos de bits respectivos de audio y video y suministran información saliente.
<u>2. Discusión de la técnica conexas</u> Los estándares del MPEG (Grupo De Expertos en películas) son uno de los estándares de codificación de video digital más ampliamente aceptados e incluyen MPEG-1 y MPEG-2 (el MPEG-4 está aún siendo desarrollado) MPEG-2 soporta más alta calidad de video a mayores tasas de bits que el MPEG-1, permite más opciones en los formatos de codificación y decodificación que el MPEG-1, y es capaz de manejar los flujos de bits	Como aparece en la figura 2, un flujo de bits de video MPEG incluye seis capas: Una capa de secuencia de video, una capa para un grupo de
películas, un capa de películas, una capa para las secciones, un capa para el macrobloque, y una capa para el bloque. En la figura 2, esas porciones de la secuencia del video que se denotan entre paréntesis son opcionales. Las capas del nivel superior de un flujo de bits de un video MPEG difieren, dependiendo de si la secuencia del video es una	más macrobloques. Un macrobloque está conformado de varios bloques de 8 x 8 con coeficiente DCT (Transformación Discreta del Coseno) con un número de otros parámetros, tales como el código de escala de cuantificación, vectores en movimiento, etc. (ver Estándar ISO/IEC 13818-2). El número de bloques que forman un macro-bloque puede

secuencia MPEG-1 de video o una secuencia MPEG-2 de video. Las secuencias de video MPEG-1 y MPEG-2 comienzan con un encabezamiento de la secuencia y terminan con un código de terminación de secuencia. El encabezamiento de la secuencia MPEG-1 está seguido por al menos uno o más grupos de películas, cada grupo de películas comenzando con un encabezamiento e incluyendo por lo menos una película con cada imagen comenzando con un encabezamiento de película e incluyendo un o más secciones. En contraste, el encabezamiento de la secuencia de MPEG-2 está seguido por información de extensión de secuencia, y por lo tanto una secuencia de video MPEG-2 se puede diferenciar fácilmente de la secuencia de video MPEG-1. La extensión de secuencia está seguida por un encabezamiento GOP (opcional), una o más películas y el código de final de secuencia. Como se muestra, el encabezamiento GOP puede estar seguido por información del usuario (opcional). Cada película incluye un encabezamiento de la película, seguida por la información de la extensión codificada de la película, extensión e información del usuario (opcional) y por lo menos una sección.	variar, dependiendo de si la secuencia del video es MPEG-1 o MPEG-2. Para la MPEG-2 el número de bloques puede también variar dependiendo de del formato cromático. Cada bloque contiene valores de coeficiente DCT cuantificados que son codificados a varios largos. Hay una amplia disponibilidad de detalles adicionales sobre el MPEG, incluyendo el ESTANDAR DE COMPRESION DE VIDEO MPEG, Joan I. Mitchell et al., Champan & Hill, 1997, ISBN 0-412-08771-5, que se incorpora al presente por referencia. Un diagrama funcional simplificado de un decodificador convencional de video (50) se ilustra en la Figura 3. Los decodificadores convencionales de video son implementados generalmente como la "caja negra" en la que el decodificador de video (50) recibe un flujo de bits del video y suministra información saliente del video. Dentro de la caja negra, el decodificador (50) descodifica el flujo de bits del video sobre una base macrobloque-por-macrobloque, haciendo las siguientes operaciones: Primero, el decodificador del video lleva a cabo una Codificación Inversa de Largo Variable (IVLC por sus siglas en inglés) para expandir la información codificada de
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Sin tener en cuenta si la secuencia es una secuencia de video MPEG-1 o una secuencia de video MPEG-2, cada sección está conformada por uno o	largo variable. Luego, el decodificador del video descuantifica los coeficientes DCT cuantificados (llamada Cuantificación Inversa de
coeficientes DCT (IQDCT)), basado en las tablas de cuantificación apropiadas (matrices) y en la escala de cuantificación para reconstruir (tan cerca como sea posible) los coeficientes DCT. Luego, el decodificador del video lleva a cabo cálculos Inversos de DCT (IDCT) y compensación de movimiento para reconstruir la información del pixel, que se suministra como información saliente del video en el momento adecuado. Debido a que los estándares MPEG han sido tan ampliamente aceptados y su uso tan variado, y debido a que muchos vendedores diferentes hacen o venden productos MPEG, hay una significativa necesidad para monitorear y analizar la calidad de un flujo de bits MPEG a fin de verificar por lo menos que está en un mínimo conforme a los estándares. Debido a las demandas de un ancho de banda mayor del flujo de bits del video versus el flujo de bits del audio, esta necesidad es particularmente aguda con respecto al flujo de bits del video MPEG. Por Ejemplo, los diseñadores de los	de bits del video MPEG y aislar los problemas de inter-operabilidad. Más allá de este nivel de monitoreo y análisis de calidad, hay también una necesidad de suministrar información y análisis de calidad relativo a aquellos parámetros sobre los cuales los diseñadores de los codificadores MPEG tienen alguna escogencia. Estos parámetros pueden ser óptimos o no, dependiendo del proceso particular de codificación usado y el material subyacente del video que fue codificado. Tal información y análisis de calidad puede proveer una retro-alimentación para ayudar a los diseñadores a desarrollar algoritmos de codificación más eficientes que optimicen la calidad de la imagen por cierto número de bits. También hay necesidad de monitorear y evaluar la calidad de la información saliente del video, según se vea después de haber sido recibido y descodificado por un decodificador de video MPEG. Esta información es útil para los diseñadores de

codificadores de video MPEG quieren saber si su salida cumple con MPEG, mientras los diseñadores de los decodificadores de video MPEG quieren saber si la información que están usando para desarrollar y probar su diseño está, realmente, conforme con el estándar. Además, aunque la sintaxis del video MPEG está especificada en los estándares, pueden existir diferencias sutiles en la interpretación de los estándares, aunque cumplan aún con ellos, y por lo tanto es casi inevitable que existan problemas de interoperabilidad. Así, los diseñadores tanto de codificadores como de decodificadores necesitan una herramienta para analizar un flujo	los codificadores MPEG, así como para los transmisores de las transmisiones MPEG. Por ejemplo, una estación transmisora podría usar la información para economizar ancho de banda si la calidad de la información saliente del video fuera superior a la necesaria, y para aumentar el ancho de banda de la señal transmitida si la calidad de la información saliente del video fuera pobre. Aunque existen sistemas convencionales para evaluar la calidad de la información saliente del video después de los procesos de codificación y decodificación, estos sistemas se apoyan en una comparación de la información saliente del video descodificado frente a la información entrante del video original.
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De acuerdo con un aspecto adicional del invento, el analizador de la calidad del flujo de bits analiza la información proveída por el decodificador del video y calcula varias métricas permitiendo al usuario determinar la calidad del proceso de codificación. Basado en parámetros descodificados obtenidos de la decodificación del flujo de bits elemental del video a nivel IVLC, el analizador de calidad del flujo de bits calcula métricas pertenecientes a la cantidad de información comprimida en el decodificador del

video, qué tan bien el codificador calculó el tamaño del dispositivo separador del decodificador, qué tan bien el codificador calculó la tasa de los bits y si los bits codificados están siendo usados eficientemente.

De acuerdo con otro aspecto del invento, el analizador de calidad del flujo de bits además incluye un medidor de la calidad del dominio comprimido que predice la calidad de la secuencia del video totalmente descodificado, contenido dentro del flujo de bits elemental del video, sin descodificar totalmente el flujo de bits elemental del video y sin usar la secuencia del video original. Los métodos usados para predecir la calidad de la secuencia del video totalmente descodificado pueden ser utilizados en cualquier secuencia de video que haya sido comprimida de acuerdo con un esquema de compresión de bloque DCT, incluyendo el MPEG-1 y el MPEG-2, el H.261 y el H.263.

Basándose en los parámetros obtenidos de la decodificación del flujo de bits elemental del video al nivel IVLC, el medidor de calidad comprimido del dominio predice la cantidad de distorsión espacial en la secuencia del video totalmente descodificado, debido a la cuantificación de los coeficientes

DCT. Basándose en este mismo nivel de decodificación, el medidor de calidad del dominio comprimido también predice la cantidad de distorsión espacial en la secuencia del video totalmente descodificado que es capaz de ser percibido por un observador humano. El medidor de calidad comprimido del dominio también predice una tercera medida de la calidad de la secuencia del video totalmente descodificada que es indicativa de la cantidad de error en la predicción de movimiento en el proceso de codificación. Aunque la tercera medición requiere la cuantificación inversa de los coeficientes DCT, este paso se hace solamente en los bloques no-intra, y no requiere decodificación total del flujo de bits elemental del video, ni requiere la secuencia original del video.

Breve descripción de los Dibujos

A manera de ejemplo se describen incorporaciones ilustrativas del presente invento con referencia a los dibujos que las acompañan, en donde:

La Figura 1 ilustra un decodificador MPEG;

La Figura 2 ilustra varias capas de una secuencia de video MPEG

La Figura 3 ilustra un diagrama funcional simplificado de un decodificador de vídeo MPEG convencional;

La Figura 4 ilustra un ejemplo de una computadora personal al cual se le pueden implementar incorporaciones del presente invento;

La Figura 5 ilustra un diagrama de un bloque de alto nivel funcional de un sistema de análisis del flujo de bits de un video MPEG, de acuerdo con una incorporación del presente invento;

La Figura 6 ilustra un diagrama de un bloque de alto nivel funcional de un sistema de análisis del flujo de bits de un video MPEG, de acuerdo con otra incorporación del presente invento;

La Figura 7 ilustra un diagrama de un bloque funcional de un analizador de la calidad del flujo de bits, de acuerdo con una incorporación del presente invento;

La Figura 8 ilustra un diagrama de un bloque funcional de un medidor comprimido de la calidad del dominio, de acuerdo con una incorporación del presente invento;

La Figura 9 ilustra una vista a nivel superior, según la ve el usuario, de una interfase para el usuario gráfico, de acuerdo con una incorporación del presente invento; y

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Las Figuras 10 a 20 ilustran varias vistas, según las ve el usuario, de una interfase del usuario gráfico de un sistema de análisis del flujo de bits de un video, de acuerdo con la incorporación del presente invento.

Descripción Detallada

De acuerdo con un primer aspecto del presente invento, un analizador de la calidad del flujo de bits es implementado en software en una computadora personal (PC), activando el sistema operativo de Windows NT™. Un PC ilustrativo (100) en el que el presente invento pueda ser implementado aparece en la figura 4. El PC (100) incluye un procesador (110), una memoria (120), un dispositivo removible de almacenamiento (130), una pantalla (150) un dispositivo marcador (160), y un dispositivo de entrada (170), todos acoplados juntos a través de una barra de transmisión (bus). Deberá ser entendido que este PC (100) se muestra únicamente para fines ilustrativos y que el presente invento no está limitado a usarse en un sistema con esta configuración específica, pues son posibles otras configuraciones. Por ejemplo, la memoria (120) puede tener dispositivos de memoria tales como unidades de disco duro o unidades de disco óptico, RAM, ROM, u otros dispositivos de memoria y combinaciones de los mismos. El

dispositivo de entrada (170) puede incluir un teclado que permita al usuario interactuar con el sistema. El puntero del cursor (160) puede ser, por ejemplo, un "puck", una barra de control, una bola de ratón, o un ratón. La pantalla (150) puede ser una pantalla CRT o dispositivo similar que permita al usuario monitorear parámetros MPEG y visualizar sus interacciones con el analizador de calidad del flujo de bits. El dispositivo removible de almacenamiento (130) puede ser una unidad de CD-ROM, una unidad de cinta o de diskette. El dispositivo removible de almacenamiento (130) puede ser usado para cargar aplicaciones de software incluyendo software del analizador de calidad del flujo de bits.

El software, incluyendo el código que implementa el presente invento, puede ser almacenado en algún medio de almacenamiento removible, como un CD-ROM, cinta o diskette. El software puede ser copiado a un medio de almacenamiento permanente en el PC (por ejemplo en el disco duro) para preservar el medio removible de almacenamiento con fines de respaldo (back - up). Cuando el software del analizador de calidad del flujo de bits del invento esté realmente en uso, el software es generalmente y por lo menos almacenado parcialmente en RAM, y ejecutado en el procesador (110).

La figura 5 ilustra el diagrama de bloque funcional de alto nivel en un sistema de análisis del flujo de bits del video MPEG, de acuerdo con una incorporación del presente invento. El sistema de análisis del flujo de bits del video MPEG incluye una línea de interfase (175), un desmultiplexor (180) un analizador de la calidad del flujo de bits (190), y una interfase del usuario gráfico (200). La línea de interfase (175) recibe un flujo de bits MPEG y convierte el flujo de bits MPEG en un formato adecuado para procesar por parte del desmultiplexor (180). El desmultiplexor (180) separa el flujo de bits MPEG en varios flujos de bits elementales (audio, video, y/o flujos de bits elementales de audios múltiples o videos múltiples) y suministra el flujo de bits elemental del video que debe ser monitoreado en el analizador de calidad del flujo de bits (190). El analizador de calidad del flujo de bits (190) rompe y descodifica el flujo de bits elemental del video para extraer varios parámetros y ejecutar niveles variados de análisis de calidad en el flujo de bits. La información sobre el flujo de bits elemental del video MPEG monitoreado, así como los niveles variados de análisis de calidad, aparecen en la pantalla al usuario a través de la Interfase del Usuario Gráfico (GUI) (200). Adicionalmente a través del GUI (200), El usuario puede seleccionar el nivel

de monitoreo y análisis de calidad, para controlar el analizador de calidad del flujo de bits (190).

En incorporaciones corrientes del presente invento, la línea interfase (175) puede ser cualquiera de una tarjeta de interfase paralela sincrónica (SPI), una interfase serial sincrónica (SSI), una tarjeta de interfase serial asincrónica (ASI), o una tarjeta interfase G.703 conectada operativamente a la barra de transmisión (BUS) del microprocesador del PC. Debido a que la implementación real de la línea interfase (175) es dependiente del medio de transmisión en que se recibe el flujo de bits MPEG, y debido a que la implementación de dicha línea interfase (175) es conocida en la técnica, se omite en el presente una descripción más amplia. Similarmente, el desmultiplexor real (180) es implementado en software, y está basado en el Decodificador del Objetivo del Sistema MPEG (STD) que está bien documentado en el estándar MPEG. Por lo tanto se omite aquí una descripción más amplia del desmultiplexor (180).

El diagrama del bloque funcional ilustrado en la Figura 5 sugiere que el analizador de calidad del flujo de bits (190) sea capaz de estar a la par con el flujo de bits del video y

de operar en tiempo real. Dependiendo del nivel de monitoreo y del nivel de análisis de calidad deseado, se puede hacer la operación en tiempo real. Además, varios niveles de monitoreo y análisis de calidad pueden ser llevados a cabo en tiempo real, dependiendo de la resolución de la información de entrada del video, la tasa de bits de entrada, etc.

La figura 6 ilustra un diagrama del bloque funcional a alto nivel de un sistema de análisis de flujo de bits de video MPEG, de acuerdo con otra incorporación del presente invento, similar a la incorporación de la Figura 5, pero que no necesita operar en tiempo real. El sistema de análisis del flujo de bits de video MPEG, de la figura 6, incluye una línea interfase (175), un desmultiplexor (180), una memoria (120) un analizador de calidad de flujo de bits (190) y una Interfase para Usuario Gráfico (GUI) (200). Como en la Figura 5, la línea interfase (175) convierte el flujo de bits MPEG en un formato adecuado para procesar con el desmultiplexor (180). El desmultiplexor (180) separa el flujo de bits MPEG en varios flujos de bits elementales (audio, video, y/o flujos elementals de audio múltiple o de video múltiple) y escribe el flujo de bits elemental de video que debe ser monitoreado en la memoria (120). Así, el

analizador de calidad del flujo de bits (190) puede acceder el flujo de bits elemental del video desde la memoria, romper y decodificar el flujo de bits para extraer varios parámetros y llevar a cabo niveles varios de análisis de calidad del flujo de bits elemental del video a cualquier nivel de detalle deseado por el usuario, ya que no se requiere una operación de tiempo real. Varias informaciones referentes al flujo de bits elemental del video MPEG monitoreado y varios niveles de análisis de calidad aparecen en la pantalla del usuario a través del GUI (200). Adicionalmente, a través del GUI (200) el usuario puede seleccionar el nivel de monitoreo y análisis de calidad para controlar el analizador de calidad del flujo de bits (190). Por las mismas razones mencionadas con respecto a la figura 5, se omite una descripción más amplia de la línea interfase (175) y del desmultiplexor (180). Como se puede apreciar, la memoria (120) puede ser RAM, disco o cualquier otro tipo de almacenamiento donde se pueda escribir.

Desde un punto de vista funcional amplio, el analizador de calidad de flujo de bits (190) de las figuras 5 y 6, es un dispositivo que monitorea una transmisión de video y analiza la calidad de esa transmisión de video a niveles variables de

detalle, que el usuario selecciona a través del GUI (200). Como aparece en la Figura 7, el analizador de calidad de flujo de bits (190) incluye un decodificador de video MPEG (210) y un Medidor De Calidad de Dominio Comprimido (CDQM) (220). El decodificador (210) implementa todas las funciones de un decodificador de video convencional, incluyendo operación de codificación inversa de largos variables (IVLC) para expandir la información codificada de largo variable, hacer cuantificación inversa de los coeficientes DCT cuantificados (IQDCT) para obtener coeficientes DCT y hacer cálculos inversos DCT (IDCT) y compensación de movimiento para reconstruir la información de pixels. Sin embargo, en contraste con los decodificadores de video convencionales que reciben un flujo de bits de video comprimido y una información de salida de pixels, el decodificador (210) del analizador de calidad del flujo de bits (190) es capaz de realizar varios niveles de descodificación, basado en el nivel de monitoreo y análisis de calidad seleccionado por el usuario a través del GUI (200). Dentro del analizador de calidad del flujo de bits (190) el CDQM (220) estima varias medidas de distorsión de la salida resultante del video (por ejemplo como salida del pixel) usando únicamente el flujo comprimido de bits de video.

Como se ilustra funcionalmente en la Figura 7, la decodificación del flujo de bits de video se hace dentro del decodificador (210) del analizador de calidad del flujo de bits (190) en secciones, dependiendo del nivel de monitoreo y análisis de calidad seleccionado por el usuario a través del GUI (200). En consecuencia, si el usuario desea ver información perteneciente a los varios encabezamientos (encabezamiento de secuencia, encabezamiento GOP, etc.), la decodificación no se hace y el analizador de calidad del flujo de bits (190) simplemente rompe la información de los varios encabezamientos para proveerla al GUI (200). Si el usuario desea ver valores de coeficiente DCT cuantificados, entonces la decodificación se hace a través del nivel IVLC, y si el usuario desea ver los valores DCT en sí, entonces la decodificación se hace a través del nivel IQDCT. Si el usuario desea ver la información real, entonces se hace una decodificación total. Debido a que el analizador de calidad del flujo de bits (190) puede instruir al decodificador (210) que realice varios grados de decodificación parcial, pueden economizarse tiempo considerable y recursos de la computadora, dependiendo del nivel de monitoreo y análisis de calidad seleccionados por el usuario a través del GUI (200).

Así, la operación en tiempo real para ciertos niveles de monitoreo y análisis de calidad es posible.

El analizador de calidad de flujo de los bits (190) suministra medición y análisis de tres clases de calidad. En la clase 1, la sintaxis y semántica del MPEG, el analizador de calidad de flujo de bits (190) analiza el flujo de bits del video, verificando que esté conforme con el MPEG aplicable (MPEG-1 ó MPEG-2) estándar e identifica si el flujo de bits del video cumple con las especificaciones del MPEG estándar aplicable. En la clase 2, Comportamiento Dinámico, el analizador de la calidad del flujo de bits (190) analiza aquellos parámetros sobre los cuales el diseñador del codificador, o el transmisor de flujo de bits del video tuvo alguna escogencia y muestra en pantalla información que le permite a uno evaluar lo acertado de esas escogencias. En la Clase 3, la Calidad del Video, el analizador de la calidad del flujo de bits (190) analiza la calidad del flujo saliente resultante del video (por ejemplo la salida del pixel), pero suministrando cálculos de varias medidas de distorsión, incluyendo el error de la media al cuadrado, error de predicción de movimiento y una medición objetiva que está basada en la percepción visual humana. El análisis de la

Clase 3 se hace con el CDQM (220) dentro del analizador de calidad del flujo de bits (190).

En la Clase 1, el analizador de calidad de flujo de bits (190) determina si el flujo de bits del video se adhiere al estándar aplicable, analizando la información del encabezamiento, información de la extensión, si los códigos terminales apropiados están presentes, etc., y comparando esta información con el estándar aplicable. En la clase 1, el analizador de calidad del flujo de bits (190) examina tanto la sintaxis del flujo de bits del video y la semántica del mismo, para cumplimiento con el estándar aplicable. Por ejemplo, la información sintáctica examinada puede incluir si la información requerida es extraída de la posición esperada en el flujo de bits del video (por ejemplo, si están extractados los códigos de iniciación y reconocidos cuando deben ser extractados, o si hay un código de iniciación en una posición inesperada en el flujo de bits del video), de acuerdo con las reglas de sintaxis prescritas por el MPEG. La información semántica que es examinada puede incluir si los valores reales de los varios parámetros están dentro de los valores mínimo y máximo establecidos por el estándar MPEG (ejemplo, el número de secciones en una película, así sean

valores de coeficientes DCT descuantificados están dentro de los valores permitidos, etc.) y si las reglas del estándar han sido seguidas (ejemplo si un cuadro I viene inmediatamente después de un encabezamiento GOP, etc.). La información sobre los estándares MPEG aplicables es almacenada en la memoria 120 del PC (100).

Si el flujo de bits del video está conforme con un estándar MPEG, entonces la información detallada sobre el flujo de bits del video es suministrada al GUI (200) para aparecer en pantalla. Por ejemplo, la información suministrada a GUI (200) para aparecer en pantalla puede incluir si el flujo de bits del video es MPEG-1 ó MPEG-2, los valores del parámetro reales dentro de los varios encabezamientos (encabezamiento de la secuencia, encabezamiento del GOP (si está presente), encabezamiento de la imagen, encabezamiento de la sección, etc.) información de la extensión y extensión de la codificación de la película (si es MPEG-2)), así como información con base computarizada por ejemplo el número de secciones en un cuadro, etc. El nivel de detalle de la información que aparece en pantalla al usuario puede ser seleccionada por el usuario a través del GUI (200) y puede requerir diferentes niveles de decodificación, que oscilan

desde información que requiere sólo ruptura de la información del encabezamiento, hasta información que requiere la ejecución de codificación inversa de largos variados (IVLC) y cuantificación inversa de los coeficientes DCT (IQDCT).

El analizador de calidad de flujo de bits (190) también está disponible para monitorear y analizar ciertos flujos de bits de video que no cumplen con los estándares MPEG. Por ejemplo, los codificadores MPEG que fueron desarrollados antes de haber congelado un estándar, y que pueden no cumplir totalmente, si son suficientemente bien conocidos, pueden ser reconocidos y pueden aparecer en pantalla varios valores de parámetros, a través del GUI (200). El punto de falta de cumplimiento puede ser semántico o sintáxico, o ambos. En las incorporaciones de la figura 6, inclusive si el flujo de bits del video que no cumple no es reconocido, no existe un requerimiento para decodificación en tiempo real, y así el analizador de calidad del flujo de bits puede monitorear flujos de bits que no cumplen con los estándares, que no pudieron ser descodificados en tiempo real, debido a una variedad de razones. Cuando el flujo de bits del video que no está cumpliendo, puede ser reconocido o descodificado, una caja para diálogo de interacción es presentada al usuario por

cada parámetro incorrecto, con un mensaje informativo explicando la naturaleza del incumplimiento. Además, todos esos errores son escritos en un archivo para futura referencia y diagnóstico. Si el flujo de bits del video no cumple con estándares MPEG y no puede ser reconocido, entonces el mensaje informativo indicando este hecho aparece en pantalla por el GUI (200). En una incorporación actual del invento, se presenta un buzón de diálogo al usuario indicando que la decodificación del flujo de bits del video no fue posible y la razón más probable para no haber cumplido (por ejemplo, un código de iniciación no reconocido en algún punto en el flujo de bits del video). Obviamente, deberá tenerse en cuenta que el analizador de calidad del flujo de bits (190) puede ser modificado para monitorear y analizar otros tipos de flujos de bits, como los flujos de bits H.261 y H.263, cada uno de ellos es muy similar estructuralmente al MPEG e incluye flujo de bits elementales de video que son similares sintáxicamente a los de MPEG.

En la clase 2 el analizador de calidad del flujo de bits (190) analiza aquellos parámetros sobre los cuales el diseñador del codificador o el transmisor del flujo de bits del video tuvo alguna escogencia y suministra información al

GUI 200 permitiendo medir lo acertado de esas escogencias. Por ejemplo, en la Clase 2 el analizador de calidad del flujo de bits (190) suministra el tamaño mínimo del dispositivo separador de la información del video comprimido que el codificador consideraba suficiente para decodificar totalmente la información del flujo de bits del video (basado en `vbv_separador (buffer)-tamaño` y `vbv_separador(buffer)_tamaño_extensión`), y suministra sobre una base cuadro-por-cuadro, varios indicios de que el separador está lleno. Basados en el modelo STD, el tipo de cuadro (I, P, o B), y la cantidad de información comprimida del video en los varios tipos de cuadros, el analizador de calidad del flujo de bits (190) calcula la cantidad de información comprimida del video en el separador de la información comprimida del video y actualiza este cálculo en cada cuadro. El analizador de calidad de flujo de bits (190) también calcula una segunda medida de llenado del separador, basada en la cantidad de información comprimida del video en el separador de información comprimida del video y en la cantidad de tiempo en que el codificador consideró que se podía almacenar un cuadro en particular, dentro del separador de información comprimida del video, antes de que esa información comprimida fuera mostrada en pantalla y

descartada (basada en vbv_demora), y actualiza este cálculo en cada cuadro. Aunque estas dos mediciones deberían idealmente dar un resultado, en la práctica no lo hacen, y por eso, el analizador de calidad del flujo de bits (190) también calcula una diferencia entre estas dos medidas y actualiza esta diferencia en el cálculo de cada cuadro. Los diferentes tipos de información del separador que aparecen en pantalla a través del GUI (200) le permiten a uno identificar rápidamente si hay algún riesgo de poco flujo o flujo excesivo en el separador, y determinar si el codificador calculó bien el tamaño mínimo requerido para la información comprimida del video en el separador y qué tan bien el codificador calculó la cantidad de tiempo en que los cuadros permanecerían en el separador (buffer) de información comprimida del video. Además, cada una de estas mediciones del llenado del video le permiten a uno evaluar la posibilidad de descodificar en tiempo real el flujo de bits elemental del video.

Además de a suministrar varias mediciones relacionadas con la situación del separador, el analizador de calidad del flujo de bits (190) suministra información que identifica el tipo de cuadro (I, P, ó B), la cantidad de información comprimida

del video en cada tipo de cuadro y el nivel de llenado de bits (usado por el codificador para recibir la cantidad de cuadros programada) en cada tipo de cuadro. Esta información es suministrada al GUI (200) sobre una base cuadro-por-cuadro para cada uno de los cuadros más recientes y permite al usuario comparar la cantidad de información útil comprimida del video, en un cuadro en particular, con la cantidad de llenado de bits en ese cuadro particular. Basados en esta información, el usuario puede determinar si los bits codificados están siendo usados eficientemente. Esta información también permite al usuario tener una indicación aproximada de la resolución esperada del cuadro en particular, ya que la resolución del cuadro puede esperarse que sea mejor cuando la cantidad de información comprimida útil es alta en relación con la cantidad de llenado de bits. El analizador de calidad del flujo de bits (190) también identifica la cantidad de bits programada, establecida por el codificador y calcula un valor promedio redondeado de la cantidad real de bits en la cantidad de información comprimida del video recibida por el decodificador (210) por tiempo unitario. Esta información de la tasa de bits identifica qué tan bien el codificador cumplió con la tasa de bits programada. Así, en la clase 2, el analizador de

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calidad del flujo de bits provee varias mediciones, permitiendo al usuario evaluar prontamente la calidad del flujo de bits del video.

En la clase 3, los cálculos de la calidad de la corriente de salida del video resultante (ejemplo la salida del pixel) son suministrados usando varias mediciones de distorsión, incluyendo el error de la media al cuadrado, error de predicción de movimiento y una medición objetiva basada en la percepción visual humana. Los diferentes cálculos de la calidad de la corriente saliente resultante del video se hacen mediante el CDQM (220). Estos cálculos requieren varios niveles de decodificación y pueden ser seleccionados por el usuario a través del GUI (200). Por ejemplo, como se muestra en la figura 8, el cálculo de la media de error al cuadrado y la medida objetiva de distorsión, basada en la percepción visual humana requiere decodificación del flujo de bits del video únicamente al nivel IVLC, mientras el cálculo del error de predicción de movimiento requiere decodificación del nivel de coeficiente del DCT (por ejemplo, llevando a cabo el IVLC y el IQDCT).

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Sin tener en cuenta qué medida de calidad es seleccionada, ninguna de las medidas requiere la decodificación completa del flujo de bits del video a nivel del pixel. Además, ninguna de las medidas de calidad requiere la presencia del flujo de bits de entrada original, antes de codificar, para juzgar la calidad puesto que el flujo de bits de entrada original puede no estar disponible en el decodificador. Así, el análisis llevado a cabo por el CDQM (220) puede ser hecho por una estación transmisora o una estación receptora, o ambas, para calcular la calidad del flujo de bits saliente del video en tiempo mínimo, con procesamiento mínimo y sin requerir el flujo de bits entrante original del video, antes de codificar. En esta forma una estación transmisora puede usar la información para economizar ancho de banda si la calidad de la información de salida del video es mayor a la necesaria, y para aumentar el ancho de banda de la señal transmitida si la calidad de la información de salida del video es pobre.

El CDQM (220) provee tres cálculos diferentes prediciendo la cantidad de distorsión en el flujo de bits de salida del video, debido al proceso de codificación. El primer cálculo predice la cantidad de distorsión espacial de la corriente de

salida resultante del video, debido a error en la cuantificación y está basado en el análisis de error de la media al cuadrado. El error de cuantificación para un coeficiente DCT sencillo (en el dominio DCT), se da en Ecuación (1):

$$Q_{\text{error}} = |DCT_i - IQDCT_i| \quad (1)$$

Donde DCT_i es el valor original del coeficiente a la " i " antes de cuantificación y $IQDCT_i$ es el valor del coeficiente a la " i " después de la cuantificación inversa. Sin embargo, este análisis de error exacto es de poco uso si el valor original del coeficiente antes de la cuantificación (DCT_i) no está disponible. Así, el error de cuantificación por un solo coeficiente DCT (DCT_i) de un bloque e codificado de un macrobloque (en el dominio DCT) es más bien aproximado como aparece en la Ecuación (2):

$$Q_{\text{error}} \approx \frac{1}{2} \Delta_i \quad (2)$$

donde Δ_i es el paso de cuantificación (el número por el cual el coeficiente DCT, DCT_i fue cuantificado) por el coeficiente a la " i ", y $\Delta_i = M \cdot Q_i$, donde M es el factor de escala de cuantificación actual y Q_i , es el valor de cuantificación (de

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la matriz de cuantificación) del coeficiente a la "i". Así en el dominio Pixel, el error de la media al cuadrado (MSE) de un solo bloque e codificado de un macrobloque es dado por ecuación (3):

$$(3) \quad e = N \sum_{i=1}^{64} \frac{IDCT \left(\frac{1}{2} MQ_i \right)^2}{2} = N \frac{M^2}{4} , \sum_{i=1}^4 IDCT (Q_i)^2$$

Donde N representa el número de bloques realmente codificado para ese macrobloque. El MSE es computado separadamente para los componentes de luminancia (Y) y crominancia (Cr Cb). El valor de N puede cambiar cuando uno computa el MSE por la señal de luminancia versus la señal de crominancia, y puede también cambiar dependiendo de si todos los bloques de un macrobloque están codificados. Así, N representa el número de bloques que están realmente codificados en un determinado macrobloque. La cantidad

$\sum IDCT(Q_i)^2$ DE $i=1$ a 64 puede ser computada una vez para cada una de las matrices de cuantificación (intra y no-intra).

Adicionalmente, debido a que las matrices de cuantificación pueden cambiar con una frecuencia máxima de una vez en cada cuadro, esta computación no necesita ser hecha muy frecuentemente.

Aunque el cálculo descrito atrás suministra una predicción útil de la distorsión espacial de la corriente saliente del video debido a error de cuantificación, es posible una mejora adicional. La teoría de la tasa de distorsión está inversamente relacionada con la tasa del bit; esto es, mientras más bits por unidad de tiempo usados en representar la información comprimida del video, menor la distorsión y viceversa. Análogamente, mientras más bits sean usados en codificar los coeficientes DCT de un determinado bloque, menor la distorsión esperada y viceversa. Basados en esta relación, un refinado cálculo MSE usa una combinación lineal del cálculo anterior (ecuación 3) y una señal que es la inversa del número de bits que han sido usados en codificar los coeficientes DCT. El número de bits usado en codificar coeficientes DCT es fácilmente determinado al romper el flujo de bits. Sin embargo, este número varía significativamente de un bloque a otro, e inclusive de un macrobloque a otro. En consecuencia, basados en un análisis de regresión de

información empírica, el cálculo refinado MSE usa una suma pesada del cálculo MSE dado por la ecuación (3), el inverso del número de los bits DCT codificados por cuadro filtrado, por el largo 3 - filtro de la media, y el inverso del número de los bits DCT codificados por cuadro filtrado por un largo - 4 filtro de la media. El número de bits usado para codificar coeficientes DCT de cada cuadro es sumado y las sumas del número de bits codificados por cuadro son filtradas usando los filtros de la media largo-3 y largo-4. Los filtros de la media toman la suma de la media de los últimos 3 cuadros (largo-3 y los últimos 4 cuadros (largo-4), incluyendo el cuadro actual, las suaves variaciones en el número de bits usados para codificar los coeficientes DCT. Las sumas de la media son luego pesadas y agregadas al valor pesado del cálculo del MSE.

El cálculo MSE refinado es hecho por el CDQM (220) para cada macrobloque y es suministrado al GUI (200) para mostrar en pantalla por el analizador de calidad del flujo de bits (190). El GUI (200) muestra en pantalla el cálculo refinado MSE tanto en una base cuadro-por-cuadro como a nivel de macrobloque para el cuadro actual. Antes de mostrar en pantalla a nivel macrobloque, el cálculo refinado MSE para

cada macrobloque es suavizado promediando espacialmente el cálculo MSE refinado para un determinado macrobloque a través de los macrobloques vecinos, para reflejar mejor la distorsión que aparecería al usuario.

El segundo cálculo de la suma de distorsión predicha del flujo de bits de salida del video está basado en el cálculo refinado del MSE, e incorpora un modelo sencillo de percepción visual humana. Esta medición se refiere a un patrón de sensibilidad (ejemplo la sensibilidad del ojo humano como función de frecuencia espacial y temporal) y multiplica el espectro de error por una función de sensibilidad de contraste (CSF) del ojo humano y computa su energía. El CSF mide la sensibilidad del sistema visual frente a estímulos, como función de su frecuencia. La suma calculada de distorsión, basada en cuantificación de error ($e(x, y, t)$), puede ser determinada por cada macrobloque de cada cuadro basado en el cálculo refinado MSE, donde x , y son coordenadas de frecuencia espacial y t es una frecuencia temporal. Una medida de distorsión es con base en la sensibilidad es suministrada en la Ecuación (4):

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$$e_s = \int \int \int S(f_x, f_y, f_t) |e(f_x, f_y, f_t)|^2 df_x df_y df_t \quad (4)$$

donde $S(f_x, f_y, f_t)$ representa el CSF del ojo humano, y $|e(f_x, f_y, f_t)|^2$ es similar al MSE refinado, pero en el dominio de frecuencia. Debido a que la Ecuación (4) está definida en el dominio de frecuencia y el MSE refinado es calculado en el dominio pixel, el CDQM (220) implementa más bien a la ecuación (4) como una convolución en el dominio del pixel con un filtro digital de respuesta finita al impulso que aproxima el CSF. El CSF real que es usado para determinar este segundo cálculo de distorsión está basado en la superficie espacio-temporal descrita en "Características Espacio-temporales de los Mecanismos Visuales: Modelo Excitatorio-Inhibitorio", por Christina A. Burbek y D. H. Kelly, Journal of the Optical Society of America, volumen 70 No 9 páginas 1121 - 1126, Septiembre 1980. La respuesta de impulsos del filtro digital es luego obtenida mediante ventaneo usando ventanas Kaiser en largo 16, de acuerdo con bien conocidas técnicas de procesamiento de señales. Obviamente, deberá tenerse en cuenta que otras funciones de sensibilidad de contraste y diferentes técnicas de procesamiento de señales pueden ser usadas. Similar al cálculo MSE refinado, esta medición objetiva (por ejemplo, el segundo estimado) es

calculado por el CDQM (220) para cada macrobloque y es proveído al GUI 200 para mostrar en pantalla por el analizador de calidad del flujo de bits (190). La medición objetiva, si la selecciona el usuario, aparece en pantalla sobre una base cuadro-por-cuadro, y al nivel de macrobloque para el cuadro actual.

El tercer estimado de la cantidad de distorsión predicha del flujo de bits de salida del video también está basada en el cálculo MSE refinado y predice la cantidad de distorsión del flujo de bits de salida del video debido a predicción de error de movimiento (también llamada "Diferencia de Cuadro Desplazado" DFD)). El DFD es transmitido en forma cuantificada al decodificador para los bloques non-intra y representa el error de la predicción de movimiento hecha por el codificador (ejemplo, lo que no sería posible predecir). Así, si DFD $[n_1, n_2]$ representa la señal de error en la predicción de movimiento en el dominio pixel antes de la cuantificación (n_1, n_2 representa los mecanismos coordinados pixel, por ejemplo x, y), y DFD_c $[n_1, n_2]$ representa la misma señal (también en el dominio pixel) después de cuantificación (y IQDCT e IDCT), la información que describe DFD_c $[n_1, n_2]$ es contenida en el flujo de bits, en la forma de coeficientes

DCT en los bloques non-intra. La diferencia entre DFD $[n_1, n_2]$ y DFD_c $[n_1, n_2]$ es igual al error de cuantificación $e[n_1, n_2]$, que puede obtenerse del cálculo refinado MSE. Así la distorsión debido a error en la predicción de movimiento puede ser calculada (en el dominio pixel) usando la ecuación (5)

$$\text{DFD } [n_1, n_2] = \text{DFD}_c [n_1, n_2] + e[n_1, n_2] \quad (5)$$

Debido a que DCT es una transformación unitaria, la computación de la energía de DFD $[n_1, n_2]$ (es decir, la cantidad de error en la predicción del movimiento) puede ser fácilmente hecha en el dominio de frecuencia, usando directamente las muestras de los coeficientes DCT de los bloques non-intra. Así, un estimado de la cantidad de error en la predicción del movimiento puede ser determinado, con base en macrobloque-por-macrobloque, basados en el cálculo refinado MSE y en los coeficientes DCT de los bloques non-intra, sin tener que computar el IDCT. Este conocimiento del error en la predicción del movimiento suministra un entendimiento en el comportamiento del cálculo de movimiento por parte del codificador. Igual al cálculo del MSE refinado y del segundo cálculo (medición objetiva), el DFD es

calculado por el CDQM (220) para cada macrobloque y es proveído al GUI (200) para mostrar en pantalla por parte del analizador de calidad del flujo de bits (190). Si el cálculo DFD es seleccionado por el usuario, aparece en pantalla en una base cuadro-por cuadro, y al nivel de macrobloque para el cuadro actual.

Aunque los cálculos de la distorsión anteriormente descritos fueron basados en las aproximaciones de la ecuación (3), hay otros métodos de calcular la cantidad de distorsión espacial del flujo saliente del video debido a error en la cuantificación. Basados en el trabajo anterior de Gregory S. Yovanoff y Sam Liu (descrito en "Análisis Estadístico de los Coeficientes DCT y su Error en la cuantificación", Tema de la 30ª Conferencia Asilomar sobre Señales, Sistemas y Computadoras, 1996) sobre la distribución del coeficiente JPEG DCT se puede asumir que la distribución del coeficiente MPEG DCT puede ser calculada también con base en un modelo estadístico de la distribución del coeficiente DCT y la distribución del error de cuantificación. Por ejemplo, asumiendo que tenemos un cálculo de la distribución del coeficiente DCT conociendo la función de la probabilidad de la densidad (pdf), $f_i(x)$, de cada coeficiente, donde i es

el índice del coeficiente de DCT, Yovanoff y Liu han demostrado que este pdf puede ser aproximado por una función gaussiana generalizada (GGF). Denotando Q_i como el valor cuantificado para el coeficiente x del DCT considerado, del índice i (es decir, después de la cuantificación en el codificador y de la cuantificación inversa en el decodificador) el error de la cuantificación puede ser expresado así (como Q_i es conocido desde el flujo de bits):

$$e = \int_{Q_i - \frac{\Delta_i}{2}}^{Q_i + \frac{\Delta_i}{2}} (x - Q_i)^2 f_i(x|Q_i) dx \quad (6)$$

Donde Δ_i es el paso de cuantificación para el coeficiente considerado (que es conocido desde el flujo de bits) y x es el valor real del coeficiente del DCT original correspondiente a Q_i antes de la cuantificación. La función condicional de la probabilidad de la densidad $f_i(x|Q_i)$ en la Ecuación (6) se relaciona con el pdf anterior por la ecuación (7):

$$f_i(x|Q_i) = \frac{f_i(x)}{\Delta_i}$$

$$\frac{\Delta_i}{Q_i} = \frac{\int_{-Q_i}^{Q_i} f_i(x) dx}{2} \quad (7)$$

Donde $f_i(x)$ es la distribución de los coeficientes DCT antes de la cuantificación. El error de cuantificación puede así ser estimado, dando el cálculo del pdf $f_i(x)$. Un cálculo fijo del pdf $f_i(x)$ que esté basado en medidas de algunas secuencias de video original puede ser usado, o alternativamente el pdf $f_i(x)$ puede ser calculado durante el proceso de decodificación. El segundo método puede proveer potencialmente un mejor cálculo del pdf para la secuencia considerada y puede ser determinado durante el proceso de decodificación midiendo el histograma de los coeficientes de DCT cuantificados y estimando los parámetros del GGF por cálculo de máximo parecido.

La figura 8 ilustra la relación funcional del CDQM (220) y el decodificador (210) dentro del analizador de calidad del flujo de bits (190), y los niveles variantes de decodificación que son requeridos para predecir los diferentes cálculos de distorsión de la salida resultante del

video. Como puede verse, el cálculo del MSE refinado y la medición Objetiva sólo requiere la decodificación IVLC (a menos que el usuario definiera que están presentes las matrices de cuantificación), mientras el cálculo de error DFD requiere decodificación IQDCT adicional. Teniendo en cuenta un flujo de bits de video MPEG típico, ninguna de las predicciones de error de distorsión mencionadas atrás requiere cálculo IDCT. Además, ninguna de las predicciones de distorsión requiere el flujo de bits de salida del video original antes de codificar.

Debería ser aparente para un conocedor experimentado de la técnica que los métodos usados por el CDQM (220) para predecir distorsión y descritos anteriormente son válidos para cualquier esquema de compresión de bloque DCT, incluyendo los esquemas de compresión DCT para bloque compensado de movimiento, como MPEG-1 y MPEG-2, y H.261 y H.263, etc. Además, deberá ser también aparente que el analizador de calidad del flujo de bits capaz de monitorear y analizar estos otros tipos de corrientes de video puede ser implementado.

La Figura 9 ilustra una pantalla, como la ve el usuario, de un sistema de análisis de flujo de bits, similar al ilustrado en la figura 6, cuando el analizador de calidad de flujo de bits (190) está en ejecución. En el nivel superior, el GUI (200) presenta al usuario una ventana del Tablero de Control de Análisis (300) en la que se monitorean y muestran varias informaciones, varias funciones de control pueden ser seleccionadas, y en la que varios niveles de monitoreo y análisis pueden ser seleccionados. La ventana del Tablero de Control de Análisis (300) incluye un número de menús incluyendo el menú de Archivo (305), un menú de Análisis (310) y un menú de Ayuda (315). El menú de Archivo (305) incluye las opciones que permiten al usuario abrir un archivo en particular, por ejemplo un archivo conteniendo un flujo de bits de un video que ha sido escrito a la memoria (120), o Salir del analizador de calidad del flujo de bits (190). Otras opciones dentro del menú de Archivo (305) (que no se muestran) pueden incluir, obviamente, borrar un archivo, renombrar un archivo, etc. El menú de Análisis (310) incluye varios niveles de análisis que pueden ser seleccionados por el usuario, incluyendo Análisis de Macro-bloque, Análisis el Separador, Análisis del Error de la media CDQM al cuadrado, y análisis de la Diferencia del Cuadro CDQM en Pantalla. Las

opciones dentro del menú de Ayuda (314) no aparecen, pero obviamente, incluyen información que describe las varias opciones y la operación del analizador de calidad del flujo de bits (190).

Dentro de la ventana de Panel de Control de Análisis (300), los usuarios pueden seleccionar qué información aparece en la ventana a nivel cuadro o a nivel de grupo de imágenes accedendo los botones de función de control (320). Por predeterminación el nivel máximo de la ventana del Tablero de Control de Análisis (300) incluye varios campos que describen el flujo de bits del video monitoreado, incluyendo un campo de Información General (325), un campo de Encabezamiento de la Secuencia (330), un campo de Encabezamiento GOP (335), un campo de Encabezamiento de la Película (340) y un campo de Encabezamiento de la Sección (345). La información que aparece en pantalla dentro del campo de la Información General (325), el campo del Encabezamiento de la Secuencia (330), el campo del Encabezamiento GOP (335), el campo del Encabezamiento de la Película (340), está basada en información rota con los encabezamientos adecuados y no necesita explicación más amplia. Como aparece en la Figura 9, el campo del Encabezamiento de la Sección (345) incluye valores mínimos y máximos de la escala de cuantificación para todas las secciones en un cuadro en particular, que estén siendo monitoreadas, así como el número total de secciones dentro del cuadro en particular. Si los cuadros deben incluir únicamente una sección, entonces los valores

mínimos y máximos en la escala de cuantificación serían los mismos. También están ilustrados dentro del campo de Encabezamiento de la sección (345) los valores de la escala de cuantificación, por sección, para cada una de las secciones de un cuadro específico. Los valores adicionales en la escala de cuantificación, más allá de las seis secciones que se muestran, pueden ser visualizados recorriendo la pantalla hacia abajo. Debe hacerse énfasis en que toda la información que aparece en pantalla en la parte superior de la ventana del Tablero de Control de Análisis (300) y descrita hasta este punto, se obtiene rompiendo el flujo de bits de video comprimido y sin ninguna decodificación. Así, esta información requiere muy poco tiempo para aparecer.

La ventana del Tablero de Control de Análisis (300) también provee al usuario la capacidad de mostrar la película representada por el flujo de bits del video, seleccionando Display Video (350). Sin embargo, se tendrá en cuenta que para ver el video se requiere una decodificación completa del flujo de bits del video comprimido. Un ejemplo de tal selección aparece en la Figura 10, en la que un área de visión (355) es presentada al usuario a través de una ventana con el Título del Video (360). Aunque no se muestra, la

película aparece en pantalla en el área de visión (355) y es controlada por los botones de función de control (320) (figura 9).

Las figuras 11 y 12 ilustran las ventanas del menú de la Extensión de Secuencia y la Extensión de Codificación de la película (365) y (370) que pueden verse desde adentro de la ventana del Tablero de Control de Análisis (300) seleccionando la Información sobre Extensión dentro del campo de Encabezamiento de la Secuencia (330), o la Extensión de Codificación de la Película, dentro del Campo del Encabezamiento de la Película (340), respectivamente.

La Figura 13 ilustra una ventana de Análisis del Bit/Separador (375) del flujo de bits del video, cuando el usuario selecciona análisis del Separador dentro del menú de Análisis que se puede bajar (310). Como aparece en la porción de Análisis del Separador (380) de la ventana de Análisis del Bit/Separador (375), el GUI (200) muestra cuadro por cuadro, curvas que representan el tamaño del Separador (385) (basadas en `vbv_separador_tamaño` y en `vb_separador_tamaño_extensión`), Estatus del Separador del Decodificador Std. (390) (basados en el modelo de

Decodificador STD), un cálculo de la demora vbv (Cálculo de Demora VBV (395)), y una Diferencia Calculada de la Ocupación del Separador (400), todos relativos al estado del separador de la información comprimida del video del decodificador (210). La Diferencia Calculada de la Ocupación del Separador (400) representa la diferencia entre el Estatus Separador del Decodificador STD (390) y el Cálculo de la Demora VBV (395). Como se puede ver en la figura 13, la información que se muestra en pantalla permite ver rápidamente el nivel de llenado del separador del video comprimido usando dos diferentes mediciones, para identificar los riesgos del separador dentro del flujo y del flujo excesivo, para evaluar la eficiencia de la utilización del separador por el flujo de bits del video codificado, y para evaluar la posibilidad de decodificación en tiempo real, del flujo de bits de video codificado.

La porción de análisis de los Bits (405 de la Figura 13 muestra en pantalla dos mediciones diferentes relacionadas con el uso de los bits. La porción inferior izquierda (410) de la porción del Análisis de Bits (404) muestra en pantalla el número de bits y el tipo de cuadro de los más recientes, con las áreas oscurecidas representando el número de bits

contenidos en cada uno de los cuadros más recientes. La porción inferior derecha (415) de la Porción del Análisis de Bits (405) muestra la tasa de bits que se debe alcanzar (420) (basados en un encabezamiento de secuencia y en información de extensión de secuencia), comparado con un valor promedio redondeado de la tasa de bits real (425).

La Figura 14 ilustra una ventana para Análisis de Macrobloque (430) para el flujo de bits del video, cuando el usuario selecciona Análisis de Macrobloque dentro del menú de Análisis que se puede descargar (310). Hay disponible una cantidad importante de información para el usuario dependiendo en las Opciones de Pantalla (435) seleccionadas por el usuario. La Región 440 de la ventana del Análisis del Macrobloque (430) muestra varios tipos de macrobloques y el porcentaje de macrobloques de ese tipo dentro del cuadro actual. El área visual (440) corresponde al área visual (355) en la Figura 10 en que se muestra el video.

La Figura 15 ilustra una ventana de Opciones de Visión en Pantalla (455) que se muestra al usuario cuando el botón de Opciones de Visualización en Pantalla (435) es seleccionado en la ventana de Análisis de Macrobloque (430), que aparece

en la Figura 14. Las varias opciones de pantalla que puede seleccionar el usuario incluyen visualización Tipo Macrobloque, valor de cuantificación del macrobloque MQQUANT, macrobloué Tipo Movimiento, y el Vector de Movimiento del macrobloque. De igual manera, el usuario puede seleccionar la granularidad del análisis de la ubicación de los bits, que, según se ilustró en la leyenda de Bits por Macrobloque (450) de la ventana de Análisis de Macrobloque (430) en la figura 14, granularidad en los controles del sombreado en la ventana de Análisis de Macrobloque (430).

La información real que muestra la figura 14 corresponde a una selección del Tipo Macrobloque únicamente. Dependiendo de las opciones de pantalla seleccionadas por el usuario, el nivel de decodificación que hace el analizador de calidad del flujo de bits (190) y que muestra en pantalla el GUI (200) varía desde cero hasta decodificación a través del nivel IVLC.

La figura 16 muestra una ventana instantánea de Información Macrobloque Adicional (460) que aparece al usuario cuando el Botón de Información MB Adicional (445) es seleccionado en la ventana de Análisis de Macrobloque (430) que aparece en la

Figura 14. La información contenida en esta ventana se explica por sí misma y requiere decodificación IVLC y decodificación IQDCT.

La figura 17 muestra una ventana de Análisis de Cálculo de Distorsión Espacial (465) cuando el usuario selecciona el análisis CDQM MSE, dentro del menú de Análisis (310) que se puede bajar. Como se ilustra, la porción de mano izquierda (470) muestra el cálculo refinado de MSE-480 de la distorsión espacial y de la Medida Objetiva (485) de la distorsión espacial, sobre una base cuadro-por-cuadro, para los componentes de luminancia con un marcador del Cuadro Actual (490) que ilustra el cuadro actual. La porción de mano derecha (475) ilustra la distorsión espacial del cuadro actual (según lo indica el marcador del Cuadro Actual (490)) a un nivel de detalle de macrobloque usando la medida MSE refinada de la distorsión espacial, aunque la Medida Objetiva habría podido ser seleccionada más bien a través del botón de Opciones de Pantalla (495). Como mencionamos anteriormente, antes de mostrar en pantalla a nivel de macrobloque, el cálculo refinado MSE para cada macrobloque es redondeado promediando espacialmente el cálculo refinado MSE para un determinado macrobloque a través de sus macrobloques vecinos,

para reflejar mejor la distorsión que le aparecería al usuario.

La figura 18 muestra una ventana de Opciones en Pantalla de Distorsión Espacial (500) cuando el botón de Opciones de Pantalla (495) es seleccionado en la ventana de Análisis de Cálculo de Distorsión Espacial (465). La ventana de Opciones en Pantalla de Distorsión Espacial (500) permite al usuario personalizar las varias medidas de distorsión espacial a sus requerimientos particulares.

La figura 19 ilustra una ventana de Análisis de Error Predicho de la Diferencia de Cuadros desplazados (505) cuando el usuario selecciona el análisis CEQM DFD dentro del menú de Análisis (310) que puede bajar. Como se aprecia, la porción de mano izquierda (510) muestra el cálculo de la diferencia del cuadro desplazado de la predicción de distorsión del movimiento (520) sobre una base cuadro-por-cuadro, con un marcador de cuadro actual (525) que ilustra el cuadro actual. La porción de mano derecha (515) ilustra la predicción de distorsión de movimiento calculada del cuadro actual (como lo indica el marcador del cuadro actual (525)) a nivel de detalle de macrobloque. Las varias opciones de pantalla que

se pueden seleccionar por parte del usuario están ilustradas en la Figura 20 de una ventana de Opciones de Pantalla para Errores Predichos DFD (535) seleccionando la ventana de Opción de Pantalla (530) en la ventana de Análisis de Error Predicho para la Diferencia de Cuadro Desplazado (505) de la Figura 19.

Habiendo descrito así por lo menos una incorporación ilustrativa de la invención, varias alteraciones, modificaciones y mejoras ocurrirán pronto para aquellos conocedores de la técnica. Esas alteraciones, modificaciones y mejoras deberán estar dentro del espíritu y cobertura del invento. Así, la anterior descripción es a manera de ejemplo únicamente y no se pretende que sea limitante. La invención está limitada únicamente según se define en las siguientes reivindicaciones y en sus equivalentes.

REIVINDICACIONES

1. Un sistema de análisis de calidad del flujo de bits, que comprende:

Un desmultiplexor (180) para recibir un flujo de bits y separar del flujo de bits por lo menos un flujo elemental de bits, en por lo menos un flujo de bits elemental incluyendo un flujo de bits elemental de video;

Un analizador de calidad del flujo de bits (190), acoplado operativamente al desmultiplexor, para recibir el flujo de bits elemental del video del multiplexor y fracturar el flujo de bits elemental del video, el analizador de calidad del flujo de bits, extrayendo parámetros fracturados caracterizando el flujo de bits elemental del video; y

Una interfase para el usuario gráfico (200), acoplado operativamente al analizador del flujo de bits, para recibir los parámetros fracturados del analizador de calidad del flujo de bits y mostrar en pantalla los parámetros fracturados.

2. El sistema de análisis de calidad del flujo de bits de la reivindicación 1, donde un nivel de análisis hecho en el flujo de bits elemental del video es seleccionado por el usuario, y en el que el analizador de calidad del flujo de bits incluye:

Un decodificador de video MPEG (210) que es acoplado operativamente a la interfase del usuario gráfico, el decodificador de video receptor del flujo de bits del video elemental y decodificando selectivamente el flujo de bits elemental del video en capas, hasta una capa de

decodificación que corresponde al nivel de análisis seleccionado, el decodificador de video que suministra parámetros decodificados a la interfase del usuario gráfico correspondiente a la capa de decodificación llevada a cabo por el decodificador de video.

3. El sistema de análisis de calidad del flujo de bits de la reivindicación 2, donde el analizador de calidad del flujo de bits incluye además:

Un medidor de calidad del dominio comprimido (220) que está acoplado operativamente al decodificador del video y a la interfase del usuario gráfico, el medidor de calidad del dominio comprimido recibiendo los parámetros descodificados correspondientes a la capa de decodificación hecha por el decodificador del video y calculando por lo menos una medición de una cantidad de distorsión en una escena de video decodificado contenida en el flujo de bits elemental de video basado en los parámetros decodificados y sin decodificación total por parte del decodificador del video, el medidor del dominio comprimido suministrando por lo menos la medición a la interfase del usuario gráfico para mostrar en pantalla.

4. Un método de monitoreo del flujo de bits que contiene los siguientes pasos:

Separar del flujo de bits por lo menos un flujo de bits elemental, en por lo menos un flujo de bits elemental incluyendo un flujo de bits elemental de video;

Fracturar el flujo de bits elemental del video para extraer parámetros caracterizando el flujo de bits elemental del video; y

Mostrar en pantalla los parámetros extractados en una pantalla.

5. El método de la reivindicación 4, conformando además los pasos de:

Decodificación en largo variable del flujo de bits elemental del video para proveer información decodificada que es codificada en largo variable en el flujo de bits elemental del video;

Determinación de una escala de calificación de un macrobloque contenido en el flujo de bits de video elemental basado en uno de los parámetros extractados y la información decodificada;

Cálculo del primer indicativo métrico de distorsión de una cantidad de distorsión en el flujo de bits elemental de

video debido a error de cuantificación, basado en la escala de cuantificación del macrobloque y valores de cuantificación de los coeficientes DCT dentro del macrobloque; y

Aparición en pantalla de la primera medida de distorsión de la pantalla.

6. El método de la reivindicación 4, conformando además los pasos de:

Decodificación de largo variable del flujo de bits elemental del video, para proveer información decodificada que está codificada en largo variable en el flujo de bits elemental del video;

Determinación de una escala de cuantificación de un macrobloque contenido en el flujo de bits elemental del video basado en uno de los Cálculos de una cantidad de distorsión en el flujo de bits elemental del video debido a error de cuantificación basado en la escala de cuantificación del macrobloque y valores de cuantificación de los coeficientes DCT dentro del macrobloque;

Multiplicación de la cantidad de distorsión mediante una función de sensibilidad de contraste de la percepción visual humana para calcular un indicativo métrico de distorsión en la cantidad de distorsión en el flujo de

bits elemental del video debido a error de cuantificación y capacidad de percepción visual humana; y
Mostrar en pantalla la medida de distorsión.

7. El método de la reivindicación 4, conformando además los pasos de:

Decodificación del largo variable del flujo de bits elemental del video para proveer información decodificada que está codificada en largo variable en el flujo de bits elemental del video;

Determinación de la escala de cuantificación de un macrobloque predicho, contenido en el flujo de bits elemental del video, basado en uno de los parámetros extractados y en la información decodificada:

Cálculo de una cantidad de distorsión en el flujo de bits elemental del video debido a error de cuantificación basado en la escala de cuantificación del macrobloque predicho y en los valores de cuantificación de los coeficientes DCT dentro del macrobloque predicho;

Cuantificación inversa de los coeficientes DCT dentro del macrobloque predicho para proveer coeficientes DCT decuantificados;

Cálculo de la cantidad de distorsión en el flujo de bits elemental del video debido a error de predicción de movimiento basado en la cantidad de distorsión y a la decuantificación de los coeficientes DCT; y aparición en pantalla de la cantidad de distorsión en el flujo de bits elemental del video, debido a error en la predicción del movimiento en la pantalla.

8. Un método controlado por computadora para predicción de distorsión en una secuencia de video que está comprimida por un esquema de compresión de bloque DCT, método que comprende los pasos de:

Recepción de flujo de bits de video codificado conteniendo una secuencia de video comprimida, correspondiente a la secuencia del video;

Decodificación de largo variado del flujo de bits de video codificado para extraer la secuencia comprimida del video; y

Cálculo de una cantidad de distorsión en la secuencia de video debido a la cuantificación del coeficiente DCT basado en la secuencia de video comprimida extractada y sin descomprimir la secuencia de video comprimida.

9. El método de reivindicación 8, controlado en computadora, conteniendo además los pasos de:

Decuantificación de los coeficientes DCT contenidos dentro de la secuencia de video comprimida; y

Cálculo de la cantidad de distorsión en la secuencia de video debido a error en la predicción de movimiento, basado en los coeficientes DCT decuantificados, y la cantidad de distorsión en la secuencia del video debido a la cuantificación de los coeficientes DCT.

10. El método de Reivindicación 8 controlado por computadora conteniendo además los pasos de:

Cálculo de una función de densidad probable de la distribución del coeficiente DCT para cada coeficiente DCT de los coeficientes DCT; y

Cálculo de la función condicional de la probabilidad de densidad del error de cuantificación del coeficiente DCT basado en la función de la densidad de la probabilidad de la distribución del coeficiente DCT;

Donde el paso de calcular la cantidad de distorsión en la secuencia del video, debido a cuantificación de los coeficientes DCT calcula la cantidad de distorsión, con base en la secuencia comprimida extractada del video y la función condicional de probabilidad de densidad y sin descomprimir la secuencia comprimida del video..

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 TRADUCCION Y
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 Registrada No. 209 Subregistro

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 C. C. 41.339.183 de Bogotá
 intérprete Oficial según Resolución No. 819 de
 15 de Abril de 1971 del Ministerio de Justicia



(19)

Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 869 684 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
07.10.1998 Bulletin 1998/41

(51) Int. Cl.⁶: H04N 17/00, H04N 7/50

(21) Application number: 97121893.2

(22) Date of filing: 09.12.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC
NL PT SE
Designated Extension States:
AL LT LV MK RO SI

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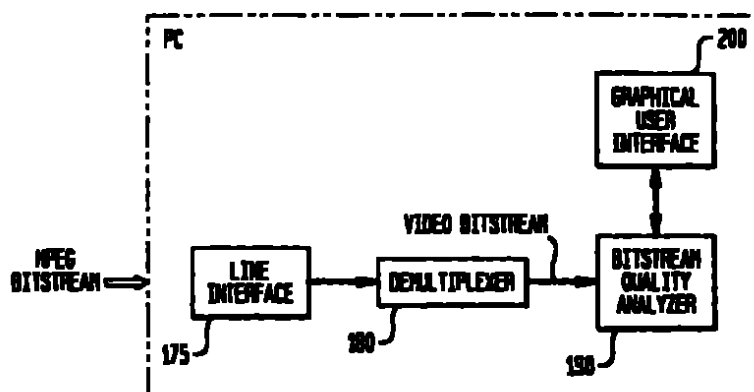
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(54) Bitstream quality analyzer

(57) A bitstream quality analysis system includes a demultiplexer (180), a bitstream quality analyzer (190), and a graphical user interface (200). The demultiplexer receives a bitstream and separates from the bitstream at least one elementary bitstream that includes a video elementary bitstream. The bitstream quality analyzer receives the video elementary bitstream from the demultiplexer and parses the video elementary bitstream to extract parameters characterizing the video elementary bitstream. The bitstream quality analyzer provides the extracted parameters to the graphical user interface, which displays the extracted parameters char-

acterizing the video elementary bitstream. A user can monitor the video elementary bitstream at varying levels of detail, and can perform varying levels of quality analysis on the video elementary bitstream. Dependent on the level of monitoring a quality analysis selected by the user, the bitstream quality analyzer provides information relating to buffer usage and coding efficiency, and can predict the quality of the fully decoded video sequence without fully decoding the video elementary bitstream and without using the original video sequence.

FIG. 5



Printed by Xerox (UK) Business Services
2.10.304

EP 0 869 684 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is directed to methods and apparatus for monitoring and analyzing a video bitstream. More particularly the present invention is directed to methods and apparatus for monitoring an MPEG video bitstream and providing metrics and analysis of the MPEG video bitstream at varying levels of detail based on the level of monitoring and analysis selected by a user. Levels of monitoring and analysis include monitoring the various characteristics and attributes of the MPEG video bitstream, testing for MPEG compliance and real-time decodability, and predicting the visual quality of decompressed video sequences contained in the MPEG video bitstream.

2. Discussion of the Related Art

The MPEG (Moving Picture Experts Group) standards are some of the most widely accepted digital video encoding standards and include MPEG-1 and MPEG-2 (MPEG-4 is still in development). MPEG-2 supports higher video quality at higher bit rates than MPEG-1, allows more options in encoding and decoding formats than MPEG-1, and is capable of handling existing MPEG-1 encoded bitstreams. MPEG-2 can also handle interlaced video and supports the scalable syntax, which allows an encoder to create enhancement layers that can both increase the quality and the spatial and temporal resolution of the motion picture. Such scalability is very useful in video applications involving telecommunications, video service with multiple qualities, video on ATM networks, and HDTV.

Fig. 1 illustrates a conventional MPEG (the term MPEG is used to denote MPEG-1 or MPEG-2, unless specifically noted otherwise) decoder 5. The decoder 5 includes a system decoder 10 that parses the MPEG bitstream and feeds separated audio and video bitstreams (containing compressed audio and video data), along with timing information, to an audio decoder 15 and a video decoder 20. The audio and video decoders 15, 20 then decode their respective audio and video bitstreams to provide output data.

As shown in Fig. 2, an MPEG video bitstream includes six layers: a video sequence layer, a group of pictures layer, a picture layer, a slice layer, a macroblock layer, and a block layer. In Fig. 2, those portions of the video sequence that are denoted parenthetically are optional. The upper level layers of an MPEG video bitstream differ, dependent upon whether the video sequence is an MPEG-1 video sequence or an MPEG-2 video sequence. Both MPEG-1 and MPEG-2 video sequences start with a sequence header and end in a sequence end code. The MPEG-1 sequence header is

followed by at least one or more groups of pictures, each group of pictures starting with a group of pictures header and including at least one picture, with each picture starting with a picture header and including one or more slices. In contrast, the MPEG-2 sequence header is followed by sequence extension information, and therefore, an MPEG-2 video sequence is easily differentiated from an MPEG-1 video sequence. The sequence extension is followed by a GOP header (optional), one or more pictures and the sequence end code. As shown, the GOP header may be followed by user data (optional). Each picture includes a picture header, followed by picture coding extension information, extension and user data (optional) and at least one slice.

Regardless of whether the sequence is an MPEG-1 video sequence or an MPEG-2 video sequence, each slice is made up of one or more macroblocks. A macroblock is made up of several 8 by 8 Discrete Cosine Transform (DCT) coefficient blocks along with a number of other parameters, such as quantization scale code, motion vectors, etc. (See ISO/IEC Standard 13818-2). The number of blocks forming a macroblock can vary, dependent on whether the video sequence is MPEG-1 or MPEG-2. For MPEG-2, the number of blocks can also vary dependent on the chroma format. Each block contains quantized DCT coefficient values that are variable-length encoded. Further details concerning MPEG are widely available, including MPEG VIDEO COMPRESSION STANDARD, Joan L. Mitchell et al., Chapman & Hill, 1997, ISBN 0-412-08771-5, which is incorporated herein by reference.

A simplified functional diagram of a conventional video decoder 50 is illustrated in Fig. 3. Conventional video decoders are generally implemented as a 'black box' in which the video decoder 50 receives a video bitstream and provides output video data. Within the black box, the decoder 50 decodes the video bitstream on a macroblock-by-macroblock basis by performing the following operations. First, the video decoder performs Inverse Variable Length Coding (IVLC) to expand the variable-length encoded data. Then, the video decoder dequantizes the quantized DCT coefficients (termed Inverse Quantization of DCT coefficients (IQDCT)) based on the appropriate quantization tables (matrices) and the quantization scale to reconstruct (as near as possible) DCT coefficients. Next, the video decoder performs Inverse DCT (IDCT) calculations and motion compensation to reconstruct the pixel data, which is provided as output video data at the appropriate time.

Because the MPEG standards have been so widely accepted and their use so varied, and because many different vendors make or sell MPEG products, there is a significant need to both monitor and analyze the quality of an MPEG bitstream to verify at least minimal conformance with the standards. Due to the greater bandwidth demands of the video bitstream versus the audio bitstream, this need is particularly acute with respect to the MPEG video bitstream. For example,

designers of MPEG video encoders want to know that their output is MPEG compliant, while designers of MPEG video decoders want to know whether the data they are using to develop and test their design is, in fact, compliant with the standard. Furthermore, although the MPEG video syntax is specified in the standards, subtle differences in interpretation of the standards can exist while still conforming to the standard, and therefore inter-operability problems are almost inevitable. Accordingly, designers of both encoders and decoders need a tool to analyze an MPEG video bitstream and isolate inter-operability problems.

Beyond this level of monitoring and quality analysis, there is also a need to provide information and quality analysis relating to those parameters over which designers of MPEG encoders have some choice. These parameters may or may not be optimal, dependent on the particular encoding process used and the underlying video material that was encoded. Such information and quality analysis can provide feedback to help designers develop more efficient encoding algorithms that optimize picture quality for a given number of bits.

There is also a need to monitor and assess the quality of the resulting video output data as it is seen after it has been received and decoded by an MPEG video decoder. This information is useful to designers of MPEG encoders as well as to broadcasters of MPEG transmissions. For example, a broadcasting station could use the information to save bandwidth if the quality of the video output data was higher than necessary, and to increase the bandwidth of the transmitted signal if the quality of video output data was poor. Although conventional systems are available to assess the quality of video output data after encoding and decoding processes, these systems rely on a comparison of the decoded output video data to the original input video data. This sort of comparison is computationally expensive inasmuch as it requires the full decoding of the received video bitstream and a bit-by-bit comparison with the input data. The time required for such a bit-by-bit analysis can be prohibitive. In addition, from a decoding point of view, the original input video data may simply not be available to the recipient of the MPEG bitstream.

Summary Of The Invention

According to an illustrative embodiment of the invention, a bitstream quality analysis system includes a demultiplexer, a bitstream quality analyzer, and a graphical user interface. The demultiplexer receives a bitstream and separates the bitstream into at least one elementary bitstream that includes a video elementary bitstream. The bitstream quality analyzer receives the video elementary bitstream from the demultiplexer and parses the video elementary bitstream to extract parameters characterizing the video elementary bitstream. The bitstream quality analyzer provides the extracted

parameters to the graphical user interface, which displays the extracted parameters characterizing the video elementary bitstream.

According to an aspect of the invention, the bitstream quality analyzer compares the extracted parameters to parameter values allowed by the MPEG (MPEG-1 and MPEG-2) standard and notifies the user, via the graphical user interface when the video elementary bitstream does not conform to the standard. Even when the video elementary bitstream does not conform to the MPEG standard, the bitstream quality analyzer may extract parameters and provide them to the graphical user interface for display, depending on the amount of non-conformance.

According to another aspect of the invention, the bitstream quality analyzer includes an MPEG video decoder that receives the video elementary bitstream and selectively decodes the video elementary bitstream according to the level of monitoring and quality analysis selected by the user via the graphical user interface. Thus, if the user desires to view information pertaining to the various headers (sequence header, GOP header, etc), decoding is not performed at all and the bitstream quality analyzer simply parses information from the various headers to provide to the graphical user interface for display. If the user desires to view quantized DCT coefficient values, then decoding is performed through the VLC level, and if the user desires to view the DCT values themselves, then decoding is performed through the IQDCT level. If the user desires to view the actual data, then full decoding is performed. Because the decoder selectively decodes the video elementary bitstream to the level required by the user, considerable time and computational resources are saved.

According to a further aspect of the invention, the bitstream quality analyzer analyzes information provided by the video decoder and calculates various metrics allowing the user to determine the quality of the encoding process. Based on decoded parameters obtained from decoding the elementary video bitstream to the VLC level, the bitstream quality analyzer calculates metrics pertaining to the amount of compressed data in the video decoder, how well the encoder estimated the size of the decoder buffer, how well the encoder estimated the bit rate, and whether coded bits are being used efficiently.

According to another aspect of the invention, the bitstream quality analyzer further includes a compressed domain quality meter that predicts the quality of the fully decoded video sequence contained within the video elementary bitstream without fully decoding the video elementary bitstream and without using the original video sequence. The methods used to predict the quality of the fully decoded video sequence may be used on any video sequence that has been compressed according to a block DCT compression scheme, including MPEG-1 and MPEG-2, H.261, and H.263.

Based on parameters obtained from decoding the

elementary video bitstream to the VLC level, the compressed domain quality meter predicts the amount of spatial distortion in the fully decoded video sequence due to quantization of the DCT coefficients. Based on this same level of decoding, the compressed domain quality meter also predicts the amount of spatial distortion in the fully decoded video sequence that is capable of being perceived by a human observer. The compressed domain quality meter also predicts a third metric of the quality of the fully decoded video sequence that is indicative of the amount of motion prediction error in the encoding process. Although the third metric requires the inverse quantization of DCT coefficients, this step is performed only on the non-Intra blocks, and does not require full decoding of the video elementary bitstream, nor does it require the original video sequence.

Brief Description Of The Drawings

Illustrative embodiments of the present invention are described by way of example with reference to the accompanying drawings, in which:

- Fig. 1 illustrates a conventional MPEG decoder;
- Fig. 2 illustrates various layers of an MPEG video sequence;
- Fig. 3 illustrates a simplified functional diagram of a conventional MPEG video decoder;
- Fig. 4 illustrates an example of a personal computer on which embodiments of the present invention can be implemented;
- Fig. 5 illustrates a high level functional block diagram of an MPEG video bitstream analysis system according to an embodiment of the present invention;
- Fig. 6 illustrates a high level functional block diagram of an MPEG video bitstream analysis system according to another embodiment of the present invention;
- Fig. 7 illustrates a functional block diagram of a bitstream quality analyzer according to an embodiment of the present invention;
- Fig. 8 illustrates a functional block diagram of a compressed domain quality meter according to an embodiment of the present invention;
- Fig. 9 illustrates a top level view, as seen by a user, of a graphical user interface of a video bitstream analysis system according to an embodiment of the present invention; and
- Figs. 10-20 illustrate various views, as seen by a user, of a graphical user interface of a video bitstream analysis system according to an embodiment of the present invention.

Detailed Description

According to a first aspect of the present invention,

a bitstream quality analyzer is implemented in software on a personal computer (PC) running the Windows NT™ operating system. An illustrative PC 100 in which the present invention can be implemented is shown in Fig. 4. The PC 100 includes a processor 110, a memory 120, a removable storage device 130, a display (150), a pointing device 160, and an input device (170) all coupled together via a bus (140). It should be understood that this PC 100 is shown merely for illustrative purposes, and that the present invention is not limited to use with a system having this specific configuration, as other configurations are possible. For example, the memory (120) may consist of memory devices such as hard disk drives or optical disk drives, RAM, ROM, or other memory devices and combinations thereof. The input device 170 may include a keyboard that allows a user to interact with the system. The pointing device (160) may, for example, be a puck, joystick, trackball, or mouse. The display (150) may be a CRT screen, or similar device, that allows the user to monitor MPEG parameters and visualize his/her interactions with the bitstream quality analyzer. The removable storage device 130 may be a CD-ROM drive, a tape drive, or a diskette drive. The removable storage device 130 can be used to load application software including the bitstream quality analyzer software.

Software, including code that implements the present invention, may be stored on some type of removable storage media such as a CD-ROM, tape, or diskette. The software can be copied to a permanent form of storage media on the PC (e.g., a hard disk) to preserve the removable storage media for back-up purposes. When the bitstream quality analyzer software of the invention is actually in use, the software is generally and at least partially stored in RAM, and is executed on the processor 110.

Fig. 5 depicts a high level functional block diagram of an MPEG video bitstream analysis system according to an embodiment of the present invention. The MPEG video bitstream analysis system includes a line interface 175, a demultiplexer 180, a bitstream quality analyzer 190, and a graphical user interface 200. The line interface 175 receives an MPEG bitstream and converts the MPEG bitstream into a format suitable for processing by the demultiplexer 180. The demultiplexer 180 separates the MPEG bitstream into various elementary bitstreams (audio, video, and/or multiple audio or multiple video elementary bitstreams) and provides the video elementary bitstream that is to be monitored to the bitstream quality analyzer 190. The bitstream quality analyzer 190 parses and decodes the video elementary bitstream to extract various parameters and perform varying levels of quality analysis on that bitstream. Information concerning the monitored MPEG video elementary bitstream, as well as varying levels of quality analysis, are displayed to a user via a Graphical User Interface (GUI) 200. In addition, through the GUI 200, the user is able to select the level of monitoring and

quality analysis to control the bitstream quality analyzer 190.

In current embodiments of the present invention, the line interface 175 can be any one of a synchronous parallel interface (SPI) card, a synchronous serial interface (SSI) card, an asynchronous serial interface (ASI) card, or a G.703 interface card that is operatively connected to the PC's microprocessor bus. Because the actual implementation of the line interface 175 is dependent on the transmission medium on which the MPEG bitstream is received, and because the implementation of such a line interface 175 is known in the art, further description is omitted herein. Similarly, the actual demultiplexer 180 is implemented in software, and is based on the MPEG System Target Decoder (STD) which is well documented in the MPEG standard. Therefore, further description of the demultiplexer 180 is omitted herein.

The functional block diagram depicted in Fig. 5 suggests that the bitstream quality analyzer 190 is capable of keeping up with the video bitstream and operating in real time. Depending on the level of monitoring and the level of quality analysis desired, real time operation can be performed. Furthermore, various levels of monitoring and quality analysis can be performed in real time, depending on the resolution of the input video data, the input bit rate, etc.

Fig. 6 depicts a high level functional block diagram of an MPEG video bitstream analysis system according to another embodiment of the present invention that is similar to the embodiment of Fig. 5, but which does not need to operate in real time. The MPEG video bitstream analysis system of Fig. 6 includes a line interface 175, a demultiplexer 180, a memory 120, a bitstream quality analyzer 190, and a Graphical User Interface (GUI) 200. As in Fig. 5, the line interface 175 converts the MPEG bitstream into a format suitable for processing by the demultiplexer 180. The demultiplexer 180 separates the MPEG bitstream into various elementary bitstreams (audio, video, and/or multiple audio or multiple video elementary bitstreams) and writes the video elementary bitstream that is to be monitored to the memory 120. Accordingly, the bitstream quality analyzer 190 can access the video elementary bitstream from memory, parse and decode the bitstream to extract various parameters, and perform varying levels of quality analysis of the video elementary bitstream to any level of detail desired by the user, as real time operation is not required. Various information concerning the monitored MPEG video elementary bitstream and various levels of quality analysis are displayed to a user via the GUI 200. In addition, through the GUI 200, the user may select the level of monitoring and quality analysis to control the bitstream quality analyzer 190. For the same reasons mentioned with respect to Fig. 5, further description of the line interface 175 and the demultiplexer 180 is omitted. As can be appreciated, the memory 120 may be RAM, disk, or other type of writable storage.

In broad functional overview, the bitstream quality analyzer 190 of Figs. 5 and 6 is a device that monitors a video transmission and analyzes the quality of that video transmission at varying levels of detail, selectable by a user via the GUI 200. As shown in Fig. 7, the bitstream quality analyzer 190 includes an MPEG video decoder 210 and a Compressed Domain Quality Meter (CDQM) 220. The decoder 210 implements all of the functions of a conventional video decoder, including performing inverse variable length coding (IVLC) to expand the variable-length encoded data, performing inverse quantization of the quantized DCT coefficients (IQDCT) to obtain the DCT coefficients, and performing inverse DCT calculations (IDCT) and motion compensation to reconstruct the pixel data. However, in contrast to conventional video decoders that receive a compressed video bitstream and output pixel data, the decoder 210 of the bitstream quality analyzer 190 is capable of performing various levels of decoding, based on the level of monitoring and quality analysis selected by the user via the GUI 200. Within the bitstream quality analyzer 190, the CDQM 220 estimates various measures of distortion of the resulting video output (i.e. as pixel output) using only the compressed video bitstream.

As functionally depicted in Fig. 7, decoding of the video bitstream is performed within the decoder 210 in layers, dependent on the level of monitoring and quality analysis selected by the user via the GUI 200. Accordingly, if the user desires to view information pertaining to the various headers (sequence header, GOP header, etc), decoding is not performed at all and the bitstream quality analyzer 190 simply parses information from the various headers to provide to the GUI 200. If the user desires to view quantized DCT coefficient values, then decoding is performed through the IVLC level, and if the user desires to view the DCT values themselves, then decoding is performed through the IQDCT level. If the user desires to view the actual data, then full decoding is performed. Because the bitstream quality analyzer 190 can instruct the decoder 210 to perform varying degrees of partial decoding, considerable time and computational resources may be saved, depending on the level of monitoring and quality analysis selected by the user via the GUI 200. Thus, real time operation for certain levels of monitoring and quality analysis are possible.

The bitstream quality analyzer 190 provides metrics and analysis for three classes of quality. At class 1, MPEG Syntax and Semantics, the bitstream quality analyzer 190 analyzes the video bitstream for conformance with the applicable MPEG (MPEG-1 or MPEG-2) standard and identifies whether the video bitstream meets the specifications of the applicable MPEG standard. At class 2, Dynamic Behavior, the bitstream quality analyzer 190 analyzes those parameters over which the designer of the encoder, or the broadcaster of the video bitstream had some choice, and displays information

allowing one to assess the wisdom of those choices. At class 3, Video Quality, the bitstream quality analyzer 190 analyzes the quality of the resulting video output stream (i.e. pixel output) by providing estimates of various measures of distortion including mean square error, motion prediction error, and an objective metric that is based on human visual perception. Class 3 analysis is performed by the CDQM 220 within the bitstream quality analyzer 190.

At class 1, the bitstream quality analyzer 190 determines whether the video bitstream adheres to the applicable standard by analyzing header information, extension information, whether the appropriate end codes are present, etc., and comparing this information to the applicable standard. At class 1, the bitstream quality analyzer 190 examines both the syntax of the video bitstream and the semantics of the video bitstream for compliance with the applicable standard. For example, syntactical information that is examined may include whether the required information is extracted from the expected position in the video bitstream (e.g., are start codes extracted and recognized when they are supposed to be extracted, or is there a start code at an unexpected position in the video bitstream) according to the syntax rules prescribed by MPEG. Semantic information that is examined may include whether actual values of the various parameters are within minimum and maximum values established by the MPEG standard (e.g., the number of slices in a picture, whether values of dequantized DCT coefficients are within allowed values, etc.) and whether the rules of the standard have been followed (e.g., whether an I frame comes immediately after a GOP header, etc). Information regarding the applicable MPEG standards is stored in memory 120 of PC 100.

If the video bitstream conforms to an MPEG standard, then detailed information about the video bitstream is provided to the GUI 200 for display. For example, information that is provided to the GUI 200 for display may include whether the video bitstream is MPEG-1 or MPEG-2, actual parameter values within the various headers (sequence header, GOP header (if present), picture header, slice header, etc), extension information (sequence extension and picture coding extension (if MPEG-2)), as well as computationally based information such as the number of slices in a frame, etc. The level of detail of the information displayed to the user is selectable by the user via the GUI 200 and can require different levels of decoding, ranging from information that requires only parsing of the header information, to information that requires performance of inverse variable length coding (VLC) and inverse quantization of the DCT coefficients (IQDCT).

The bitstream quality analyzer 190 is also able to monitor and analyze certain video bitstreams that are not compliant with MPEG standards. For example, MPEG encoders that were developed before a standard was frozen, and which may not be fully compliant can, if

sufficiently well known, be recognized and the various parameter values displayed via the GUI 200. The extent of non-compliance may be semantic or syntactic, or both. In the embodiment of Fig. 6, even if the non-compliant video bitstream isn't recognized, there is no requirement for real-time decoding, and thus the bitstream quality analyzer can monitor non-compliant bitstreams that could not be decoded in real-time due to a variety of reasons. When the non-compliant video bitstream can be recognized or decoded, a dialog box is presented to the user for each incorrect parameter, with an informational message explaining the nature of the non-compliance. Moreover, all such errors are written to a log file for future reference and diagnosis. If the video bitstream is not compliant with MPEG standards, and it can not be recognized, then an informational message stating this fact is displayed by the GUI 200. In a current embodiment of the invention, a dialog box is presented to the user indicating that decoding of the video bitstream was not possible, and the most likely reason for non-compliance (e.g., an un-recognized start code at some point in the video bitstream). Of course, it should be realized that the bitstream quality analyzer 190 may be modified to monitor and analyze other types of bitstreams, like H.261 and H.263 bitstreams, each of which are structurally quite similar to MPEG and include video elementary bitstreams that are syntactically similar to those of MPEG.

At class 2, the bitstream quality analyzer 190 analyzes those parameters over which the designer of the encoder, or the broadcaster of the video bitstream had some choice, and provides information to the GUI 200 allowing one to assess the wisdom of those choices. For example, at class 2, the bitstream quality analyzer 190 provides the minimum size of the compressed video data buffer that the encoder believed sufficient to fully decode the video bitstream data (based on vbv_buffer_size and vbv_buffer_size_extension), and provides, on a frame-by-frame basis, various indicia of buffer fullness. Based on the STD model, the type of frame (I, P, or B), and the amount of compressed video data in the various types of frames, the bitstream quality analyzer 190 calculates the amount of compressed video data in the compressed video data buffer and updates this calculation each frame. The bitstream quality analyzer 190 also calculates a second metric of buffer fullness based on the amount of compressed video data in the compressed video data buffer and the amount of time the encoder believed a particular frame would be stored within the compressed video data buffer before that compressed data would be displayed and discarded (based on vbv_delay), and updates this calculation each frame. Although these two metrics should ideally yield the same result, in practice they do not, and hence, the bitstream quality analyzer 190 also calculates a difference between these two metrics and updates this difference calculation each frame. The different types of buffer information that is displayed via

the GUI 200 readily allows one to identify if there is a risk of buffer underflow or overflow, and to determine how well the encoder estimated the minimum size required for the compressed video data buffer and how well the encoder estimated the amount of time that frames would remain in the compressed video data buffer. Furthermore, each one of these metrics of buffer fullness allow one to assess the real-time decodability of the video elementary bitstream.

In addition to providing various metrics relating to buffer status, the bitstream quality analyzer 190 provides information identifying the type of frame (I, P, or B), the amount of compressed video data in each type of frame, and the amount of bit stuffing (used by the encoder to achieve the target frame rate) in each type of frame. This information is provided to the GUI 200 on a frame-by-frame basis for each of the most recent frames, and allows the user to compare the amount of useful compressed video data in a particular frame to the amount of bit stuffing in that particular frame. Based on this information, the user can determine whether encoded bits are being used efficiently. This information also allows the user to get a rough indication of the expected resolution of the particular frame, as the resolution of the frame may be expected to be better when the amount of useful compressed data is high in relation to the amount of bit stuffing. The bitstream quality analyzer 190 also identifies the target bit rate set by the encoder and calculates a smoothed average value of the actual bit rate based on the amount of compressed video data received by the decoder 210 per unit time. This bit rate information identifies how well the encoder met the target bit rate. Accordingly, at class 2, the bitstream quality analyzer provides various metrics allowing the user to readily assess the quality of the video bitstream.

At class 3, estimates of the quality of the resulting video output stream (i.e. pixel output) are provided using various measures of distortion, including mean square error, motion prediction error, and an objective metric based on human visual perception. The different estimates of the quality of the resulting video output stream are performed by the CDQM 220. These estimates require varying levels of decoding and are selectable by the user through the GUI 200. For example, as shown in Fig. 8, the estimation of the mean square error and the objective measure of distortion based on human visual perception require decoding of the video bitstream to only the IVLC level, while the estimation of the motion prediction error requires decoding to the DCT coefficient level (i.e. performing IVLC and IQDCT).

Regardless of which measure of quality is selected, none of the measures requires the full decoding of the video bitstream to the pixel level. Furthermore, none of the measures of quality requires the presence of the original input bitstream, prior to encoding, to judge quality, as the original input bitstream may be unavailable at

the decoder. Accordingly, the analysis performed by the CDQM 220 may be performed either at a transmitting station or a receiving station, or both, to estimate the quality of the resulting output video bitstream in minimal time, with minimal processing, and without requiring the original input video bitstream prior to encoding. Thus, a broadcasting station may use the information to save bandwidth if the quality of the video output data is higher than necessary, and to increase the bandwidth of the transmitted signal if the quality of video output data is poor.

The CDQM 220 provides three different estimations predicting the amount of distortion in the resulting video output bitstream due to the encoding process. The first estimation predicts the amount of spatial distortion of the resulting video output stream due to quantization error, and is based on a mean square error analysis. The quantization error for a single DCT coefficient (in the DCT domain) is given by Eq. (1):

$$Q_{error} = |DCT_i - IQDCT_i| \quad (1)$$

where DCT_i is the original value of the i -th coefficient before quantization and $IQDCT_i$ is the value of the i -th coefficient after inverse quantization. However, this exact error analysis is of little use if the original coefficient value before quantization (DCT_i) is not available. Thus, the quantization error for a single DCT coefficient (DCT_i) of a coded block e of a macroblock (in the DCT domain) is instead approximated as shown in Eq. (2):

$$Q_{error} \approx \frac{1}{2} \Delta_i \quad (2)$$

where Δ_i is the quantization step (the number by which the DCT coefficient, DCT_i , was quantized) for the i -th coefficient, and $\Delta_i = M \cdot Q_i$, where M is the current quantization scale factor and Q_i is the quantization value (from the quantization matrix) of the i -th coefficient. Thus, in the pixel domain, the Mean Square Error (MSE) of a single coded block e of a macroblock is given by Eq. (3):

$$e = N \sum_{i=1}^{64} IDCT\left(\frac{1}{2} M Q_i\right)^2 = N \frac{M^2}{4} \sum_{i=1}^{64} IDCT(Q_i)^2 \quad (3)$$

where N represents the number of blocks actually coded for that macroblock. The MSE is computed separately for luminance (Y) and chrominance (C_u , C_v) components. The value of N may change when one computes the MSE for the luminance signal versus the chrominance signal, and may also change depending on whether all the blocks of a given macroblock are coded. Thus, N represents the number of blocks that are actually coded in a given macroblock. The quantity $\sum IDCT(Q_i)^2$ from $i=1$ to 64 can be computed once for each of the quantization matrices (intra and non-intra).

Furthermore, because the quantization matrices can change no more frequently than once each frame, this computation does not need to be performed very frequently.

Although the previously described estimation provides a useful prediction of the spatial distortion of resulting video output stream due to quantization error, further improvement is possible. Rate-distortion theory provides that the distortion is inversely related to the bit rate; that is, the more bits per unit time used in representing the compressed video data, the less the distortion, and vice versa. Analogously, the more bits used in coding the DCT coefficients of a given block, the less the expected distortion, and vice versa. Based on this relationship, a refined MSE estimate uses a linear combination of the previous estimation (Eq. 3) and a signal that is the inverse of the number of bits that have been used in coding the DCT coefficients. The number of bits used in coding DCT coefficients is easily determined when parsing the bitstream. However, this number varies significantly from one block to another, and even from one macroblock to another. Accordingly, based on a regression analysis of empirical data, the refined MSE estimate uses a weighted sum of the MSE estimate given by Eq. (3), the inverse of the number of coded DCT bits per frame filtered by length-3 median filter, and the inverse of the number of coded DCT bits per frame filtered by a length-4 median filter. The number of bits used to code the DCT coefficients of each frame are summed and the sums of the number of coded bits per frame are filtered using length-3 and length-4 median filters. The median filters take the median sum of the last 3 frames (length-3) and the last 4 frames (length-4), including the current frame, to smooth variations in the number of bits being used to code DCT coefficients. The median sums are then weighted and added to a weighted value of the MSE estimate.

The refined MSE estimate is calculated by the CDQM 220 for each macroblock, and is provided to the GUI 200 for display by the bitstream quality analyzer 190. The GUI 200 displays the refined MSE estimate on both a frame-by-frame basis, and at the macroblock level for the current frame. Prior to display at the macroblock level, the refined MSE estimate for each macroblock is smoothed by spatially averaging the refined MSE estimate for a given macroblock across its neighboring macroblocks, to better reflect the distortion that would appear to the user.

The second estimate of the predicted amount of distortion of the resulting video output bitstream is based on the refined MSE estimate, and incorporates a simple model of human visual perception. This metric accounts for pattern sensitivity (i.e., the sensitivity of the human eye as a function of spatial and temporal frequency) and multiplies the error spectrum by a contrast sensitivity function (CSF) of the human eye and computes its energy. The CSF measures the sensitivity of the visual system to stimuli as a function of their fre-

quency. The estimated amount of distortion based on quantization error, $e(f_x, f_y, f_t)$, can be determined for each macroblock of each frame based on the refined MSE estimate, where f_x, f_y are spatial frequency coordinates, and f_t is the temporal frequency. A sensitivity based distortion measure e_s is given by Eq. (4):

$$e_s = \int \int \int S(f_x, f_y, f_t) |e(f_x, f_y, f_t)|^2 \quad (4)$$

where $S(f_x, f_y, f_t)$ represents the CSF of the human eye, and $e(f_x, f_y, f_t)^2$ is similar to the refined MSE, but in the frequency domain. Because Eq. (4) is defined in the frequency domain, and the refined MSE is calculated in the pixel domain, the CDQM 220 instead implements Eq. (4) as a convolution in the pixel domain with a finite impulse response digital filter which approximates the CSF. The actual CSF that is used to determine this second estimate of distortion is based on the spatio-temporal surface described in "Spatiotemporal Characteristics of Visual Mechanisms: Excitatory-Inhibitory Model", by Christina A. Burbeck and D.H. Kelly, *Journal of the Optical Society of America*, Vol. 70, No. 9, pp. 1121-1126, September 1980. The impulse response of the digital filter is then obtained by windowing using Kaiser windows of length 16, according to well known signal processing techniques. Of course, it should be realized that other contrast sensitivity functions and different signal processing techniques may be used. Similar to the refined MSE estimate, this objective metric (i.e., the second estimate) is calculated by the CDQM 220 for each macroblock and is provided to the GUI 200 for display by the bitstream quality analyzer 190. The objective metric, if selected by the user, is displayed on a frame-by-frame basis, and at the macroblock level for the current frame.

The third estimate of the predicted amount of distortion of the resulting video output bitstream is also based on the refined MSE estimate and predicts the amount of distortion of the resulting video output bitstream due to motion prediction error (also termed "Displaced Frame Difference" (DFD)). The DFD is transmitted in a quantized form to the decoder for the non-intra blocks and represents the error of the motion prediction performed by the encoder (i.e., what could not be predicted). Accordingly, if $DFD[n_1, n_2]$ represents the motion prediction error signal in the pixel domain prior to quantization (n_1, n_2 represent pixel coordinate axes, e.g. x, y), and $DFD_q[n_1, n_2]$ represents the same signal (also in the pixel domain) after quantization (and IQDCT and IDCT), information describing $DFD_q[n_1, n_2]$ is contained in the bitstream in the form of DCT coefficients in the non-intra blocks. The difference between $DFD[n_1, n_2]$ and $DFD_q[n_1, n_2]$ is equal to the quantization error $e[n_1, n_2]$, which can be obtained from the refined MSE estimation. Accordingly, the distortion due to motion prediction error can be estimated (in the pixel domain) using

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Eq. (5).

$$DFD[n_1, n_2] = DFD_e[n_1, n_2] + e[n_1, n_2] \quad (5)$$

Because the DCT is a unitary transform, computation of the energy of $DFD[n_1, n_2]$, (i.e., the amount of motion prediction error) can be easily carried out in the frequency domain by directly using the samples of the DCT coefficients of the non-intra blocks. Thus, an estimate of the amount of motion prediction error can be determined, macroblock-by-macroblock, based on the refined MSE estimate and DCT coefficients of the non-intra blocks, without having to compute the IDCT. This knowledge of the motion prediction error gives useful insight on the performance of motion estimation by the encoder. Similar to the refined MSE estimate and the second estimate (objective metric), the DFD is calculated by the CDQM 220 for each macroblock and is provided to the GUI 200 for display by the bitstream quality analyzer 190. The DFD estimate, if selected by the user, is displayed on a frame-by-frame basis, and at the macroblock level for the current frame.

Although the previously described estimations of distortion were based on the approximations of Eq. (3), there are other methods of estimating the amount of spatial distortion of the resulting video output stream due to quantization error. Based on previous work by Gregory S. Yovanoff and Sam Liu (described in "Statistical Analysis of the DCT Coefficients and their Quantization Error", Proceedings of the 30th Asilomar Conference on Signals, Systems, and Computers, 1996) on the distribution of JPEG DCT coefficient distribution, it can be assumed that MPEG DCT coefficient distribution can also be estimated based on a statistical modeling of the DCT coefficient distribution and the distribution of the quantization error. For example, assuming that we have an estimate of the DCT coefficient distribution by knowing the probability density function (pdf), $f_i(x)$, of each coefficient, where i is the index of the DCT coefficient, Yovanoff and Liu have shown that this pdf can be approximated by a generalized gaussian function (GGF). Denoting Q_i as the quantized value for the considered DCT coefficient x , of index i , (i.e., after quantization at encoder and inverse quantization at decoder) the quantization error can be expressed as (since Q_i is known from the bitstream):

$$e = \int_{Q_i - \frac{\Delta_i}{2}}^{Q_i + \frac{\Delta_i}{2}} (x - Q_i)^2 f_i(x|Q_i) dx \quad (6)$$

where Δ_i is the quantization step for the considered coefficient (which is known from the bitstream) and x is the actual value of the original DCT coefficient corresponding to Q_i , before quantization. The conditional

probability density function $f_i(x|Q_i)$ in Eq. (6) is related to the previous pdf by Eq. (7):

$$f_i(x|Q_i) = \frac{f_i(x)}{\int_{Q_i - \frac{\Delta_i}{2}}^{Q_i + \frac{\Delta_i}{2}} f_i(x) dx} \quad (7)$$

where $f_i(x)$ is the distribution of DCT coefficients before quantization. The quantization error can thus be estimated, given an estimation of the pdf $f_i(x)$. A fixed estimate of the pdf $f_i(x)$ that is based on measurements of some original video sequences can be used, or alternatively, the pdf $f_i(x)$ can be estimated during the decoding process. The second method may potentially provide a better estimation of the pdf for the considered sequence and may be determined during the decoding process by measuring the histogram of the quantized DCT coefficients and estimating the parameters of the GGF by maximum likelihood estimation.

Fig. 8 illustrates the functional relationship of the CDQM 220 and the decoder 210 within the bitstream quality analyzer 190, and the varying levels of decoding that are required to predict the different estimates of distortion of the resulting video output. As can be seen, the calculation of the refined MSE and the Objective metric only require VLC decoding (unless user defined quantization matrices are present), while the DFD error estimation further requires IQDCT decoding. Given a typical MPEG video bitstream, none of the aforementioned predictions of distortion error requires IDCT calculations. In addition, none of the predictions of distortion requires the original input video bitstream prior to encoding.

It should be apparent to one of ordinary skill in the art that the methods used by the CDQM 220 to predict distortion and described above are valid for any block DCT compression scheme, including motion compensated block DCT compression schemes like MPEG-1 and MPEG-2, and H.261, H.263, etc. Furthermore, it should also be apparent that a bitstream quality analyzer capable of monitoring and analyzing these other types of video streams can be implemented.

Fig. 9 illustrates a display screen, as seen by a user, of a bitstream analysis system similar to the one depicted in Fig. 6 when the bitstream quality analyzer 190 is executing. At the top level, the GUI 200 presents the user with an Analysis Control Panel window 300 in which various information is monitored and displayed, various control functions may be selected, and in which varying degrees of monitoring and analysis may be selected. The Analysis Control Panel window 300 includes a number of pull-down menus including a File menu 305, an Analysis menu 310 and a Help menu 315. The File menu 305 includes options allowing the user to

Open a particular file, for example, a file containing a video bitstream that has been written to memory 120, or to Exit the bitstream quality analyzer 190. Other options within the File menu 305 (not shown) may, of course, include deleting a file, renaming a file, etc. The Analysis menu 310 includes varying levels of analysis that may be selected by the user, including Macroblock Analysis, Buffer Analysis, CDQM Mean Square Error Analysis, and CDQM Displayed Frame Difference Analysis. Options within the Help menu 315 are not shown, but would of course, include information describing the various options and the operation of the bitstream quality analyzer 190.

Within the Analysis Control Panel window 300, users can select what information is displayed at the frame level or the group of pictures level by accessing the control function buttons 320. By default, the top level of the Analysis Control Panel window 300 includes various fields describing the monitored video bitstream including a General Information field 325, a Sequence Header field 330, a GOP Header field 335, a Picture Header field 340, and a Slice Header field 345. The information displayed within the General Information field 325, the Sequence Header field 330, the GOP Header field 335, and the Picture Header field 340 is based on information parsed from the appropriate headers and needs no further explanation. As shown in Fig. 9, the Slice Header field 345 includes minimum and maximum quantization scale values for all the slices in the particular frame being monitored, as well as the total number of slices within the particular frame. Were the frame to include only one slice, then the minimum and maximum quantization scale values would be the same. Also depicted within the Slice Header field 345 are the quantization scale values, by slice, for each of the slices in the particular frame. Additional quantization scale values, beyond the six slices shown, can be viewed by scrolling downward. It should be emphasized that all the information displayed in the top level of the Analysis Control Panel window 300 and described thus far is obtained by parsing the compressed video bitstream and without any decoding. Accordingly, this information requires negligible time to display.

The Analysis Control Panel window 300 also provides the user with the ability to display the motion picture represented by the video bitstream by selecting Display Video 350. However, it will of course be realized that the display of the video requires full decoding of the compressed video bitstream. An example of such a selection is shown in Fig. 10, in which a viewing area 355 is presented to the user via a Video Title window 360. Although not shown, the motion picture is displayed in the viewing area 355 and is controlled by the control function buttons 320 (Fig. 9).

Figs. 11 and 12 illustrate Sequence Extension and Picture Coding Extension drop down menu windows 365, 370 that are viewable from within the Analysis Control Panel window 300 by selecting Extension Informa-

tion within the Sequence Header field 330, or Picture Coding Extension within the Picture Header field 340, respectively.

Fig. 13 illustrates a Bit/Buffer Analysis window 375 of the video bitstream when the user selects Buffer Analysis within the Analysis pull-down menu 310. As shown in the Buffer Analysis portion 380 of the Bit/Buffer Analysis window 375, the GUI 200 displays, on a frame-by-frame basis, curves representing Buffer Size 385 (based on `vbv_buffer_size` and `vbv_buffer_size_extension`), Std. Decoder Buffer Status 390 (based on the STD Decoder model), an estimate of the vbv delay (VBV Delay Estimate 395), and an Estimated Buffer Occupancy Difference 400, all relating to the state of the compressed video data buffer of the decoder 210. The Estimated Buffer Occupancy Difference 400 represents the difference between Std. Decoder Buffer Status 390 and VBV Delay Estimate 395. As can be seen from Fig. 13, the information that is displayed allows one to quickly view the fullness of the compressed video buffer using two different metrics, to identify risks of buffer under flow or overflow, to assess the efficiency of buffer utilization by the encoded video bitstream, and to assess the real-time decodability of the encoded video bitstream.

The Bit Analysis portion 405 of Fig. 13 displays two different metrics regarding bit usage. The lower left portion 410 of the Bit Analysis portion 405 displays the number of bits and the frame type of the most recent frames, with the darkened areas representing the number of stuffed bits in each of the most recent frames. The lower right portion 415 of the Bit Analysis portion 405 displays the target bit rate 420 (based on sequence header and sequence extension information) as compared to a smoothed average value of the actual bit rate 425.

Fig. 14 illustrates a Macroblock Analysis window 430 for the video bitstream when the user selects Macroblock Analysis within the Analysis pull-down menu 310. A wealth of information is available to the user depending on the Display Options 435 selected by the user. Region 440 of the Macroblock Analysis window 430 shows various types of macroblocks and the percentage of macroblocks of that type within the current frame. Viewing area 440 corresponds to the viewing area 355 in Fig. 10 in which the video is displayed.

Fig. 15 illustrates a Display Options pop-up window 455 that is displayed to the user when the Display Options button 435 is selected in the Macroblock Analysis window 430 shown in Fig. 14. The various display options that may be selected by the user include displaying Macroblock Type, macroblock quantization value MQQUANT, macroblock Motion Type, and macroblock Motion Vector(s). Similarly, the user may select the granularity of bit allocation analysis, which, as depicted in the Bits per Macroblock legend 460 of the Macroblock Analysis window 430 in Fig. 14, controls granularity of the shading in the Macroblock Analysis window 430.

The actual information displayed in Fig. 14 corresponds to a selection of Macroblock Type only. Depending upon the display options selected by the user, the level of decoding that is performed by the bitstream quality analyzer 190 and displayed by the GUI 200 will vary from none to decoding through the IVLC level.

Fig. 16 shows an Additional Macroblock Information pop up window 460 that is displayed to the user when the Additional MB Info button 445 is selected in the Macroblock Analysis window 430 shown in Fig. 14. The information contained in this window is self explanatory and requires IVLC decoding and IQDCT decoding.

Fig. 17 shows a Spatial Distortion Estimation Analysis window 465 when the user selects CDQM MSE Analysis within the Analysis pull-down menu 310. As illustrated, the left hand portion 470 displays the refined MSE 480 estimation of spatial distortion and the Objective Measure 485 estimation of spatial distortion, on a frame-by-frame basis, for the luminance components, with a Current Frame marker 490 depicting the current frame. The right hand portion 475 illustrates spatial distortion of the current frame (as indicated by the Current Frame marker 490) at a macroblock level of detail using the refined MSE measure of spatial distortion, although the Objective Measure could have been selected instead via the Display Options button 495. As mentioned previously, prior to display at the macroblock level, the refined MSE estimate for each macroblock is smoothed by spatially averaging the refined MSE estimate for a given macroblock across its neighboring macroblocks, to better reflect the distortion that would appear to the user.

Fig. 18 illustrates a Spatial Distortion Display Options window 500 when the Display Options button 495 is selected in the Spatial Distortion Estimation Analysis window 465. The Spatial Distortion Display Options window 500 allows the user to customize the various spatial distortion metrics to their particular requirements.

Fig. 19 illustrates a Displaced Frame Difference Predicted Error Analysis window 505 when the user selects CDQM DFD Analysis within the Analysis pull-down menu 310. As illustrated, the left hand portion 510 displays the displaced frame difference estimation of motion prediction Distortion 520 on a frame-by-frame basis, with a Current Frame marker 525 depicting the current frame. The right hand portion 515 illustrates the estimated motion prediction Distortion of the current frame (as indicated by the Current Frame marker 525) at a macroblock level of detail. The various display options that are selectable by the user are illustrated in Fig. 20 in a DFD Predicted Error Display Options window 535 by selecting the Display Option button 530 in the Displaced Frame Difference Predicted Error Analysis window 505 of Fig. 19.

Having thus described at least one illustrative embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and

improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

Claims

1. A bitstream quality analysis system comprising:

a demultiplexer (180) to receive a bitstream and separate from the bitstream at least one elementary bitstream, the at least one elementary bitstream including a video elementary bitstream;
a bitstream quality analyzer (190), operatively coupled to the demultiplexer, to receive the video elementary bitstream from the demultiplexer and parse the video elementary bitstream, the bitstream quality analyzer extracting parsed parameters characterizing the video elementary bitstream; and
a graphical user interface (200), operatively coupled to the bitstream analyzer, to receive the parsed parameters from the bitstream quality analyzer and display the parsed parameters.

2. The bitstream quality analysis system of claim 1, wherein a level of analysis performed on the video elementary bitstream is selected by a user, and wherein the bitstream quality analyzer includes:

an MPEG video decoder (210) that is operatively coupled to the graphical user interface, the video decoder receiving the video elementary bitstream and selectively decoding the video elementary bitstream in layers, to a layer of decoding that corresponds to the selected level of analysis, the video decoder providing decoded parameters to the graphical user interface corresponding to the layer of decoding performed by the video decoder.

3. The bitstream quality analysis system of claim 2, wherein the bitstream quality analyzer further includes:

a compressed domain quality meter (220) that is operatively coupled to the video decoder and the graphical user interface, the compressed domain quality meter receiving the decoded parameters corresponding to the layer of decoding performed by the video decoder and calculating at least one metric of an amount of distortion in a fully decoded video scene that is contained in the video elementary bitstream based on the decoded parameters and without

full decoding by the video decoder, the compressed domain quality meter providing the at least one metric to the graphical user interface for display.

4. A method of monitoring a bitstream comprising the steps of:

separating from the bitstream at least one elementary bitstream, the at least one elementary bitstream including a video elementary bitstream;
parsing the video elementary bitstream to extract parameters characterizing the video elementary bitstream; and
displaying the extracted parameters on a display.

5. The method of claim 4, further comprising the steps of:

variable length decoding the video elementary bitstream to provide decoded data that is variable length encoded in the video elementary bitstream;
determining a quantization scale of a macroblock contained in the elementary video bitstream based on one of the extracted parameters and the decoded data;
calculating a first distortion metric indicative of an amount of distortion in the elementary video bitstream due to quantization error based upon the quantization scale of the macroblock and quantization values of DCT coefficients within the macroblock; and
displaying the first distortion metric on the display.

6. The method of claim 4, further comprising the steps of:

variable length decoding the video elementary bitstream to provide decoded data that is variable length encoded in the video elementary bitstream;
determining a quantization scale of a macroblock contained in the elementary video bitstream based on one of the extracted parameters and the decoded data;
calculating an amount of distortion in the elementary video bitstream due to quantization error based upon the quantization scale of the macroblock and quantization values of DCT coefficients within the macroblock;
multiplying the amount of distortion by a contrast sensitivity function of human visual perception to calculate a distortion metric indicative of the amount of distortion in the ele-

mentary video bitstream due to the quantization error and capable of human visual perception; and
displaying the distortion metric.

7. The method of claim 4, further comprising the steps of:

variable length decoding the video elementary bitstream to provide decoded data that is variable length encoded in the video elementary bitstream;
determining a quantization scale of a predicted macroblock contained in the elementary video bitstream based on one of the extracted parameters and the decoded data;
calculating an amount of distortion in the elementary video bitstream due to quantization error based upon the quantization scale of the predicted macroblock and quantization values of DCT coefficients within the predicted macroblock;
inversely quantizing DCT coefficients within the predicted macroblock to provide dequantized DCT coefficients;
calculating an amount of distortion in the elementary video bitstream due to motion prediction error based on the amount of distortion and the dequantized DCT coefficients; and
displaying the amount of distortion in the elementary video bitstream due to motion prediction error on the display.

8. A computer controlled method of predicting distortion in a video sequence that is compressed by a block DCT compression scheme, the method comprising the steps of:

receiving an encoded video bitstream containing a compressed video sequence corresponding to the video sequence;
variable length decoding the encoded video bitstream to extract the compressed video sequence; and
calculating an amount of distortion in the video sequence due to quantization of DCT coefficients based on the extracted compressed video sequence and without decompressing the compressed video sequence.

9. The computer controlled method of claim 8, further comprising the steps of:

dequantizing DCT coefficients contained within the compressed video sequence; and
calculating an amount of distortion in the video sequence due to motion prediction error based on the dequantized DCT coefficients and the

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amount of distortion in the video sequence due to the quantization of DCT coefficients.

10. The computer controlled method of claim 8, further comprising steps of:

calculating a probability density function of DCT coefficient distribution for each DCT coefficient of the DCT coefficients; and calculating a conditional probability density function of DCT coefficient quantization error based on the probability density function of DCT coefficient distribution;

wherein the step of calculating the amount of distortion in the video sequence due to quantization of DCT coefficients calculates the amount of distortion based on the extracted compressed video sequence and the conditional probability density function and without decompressing the compressed video sequence.

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35

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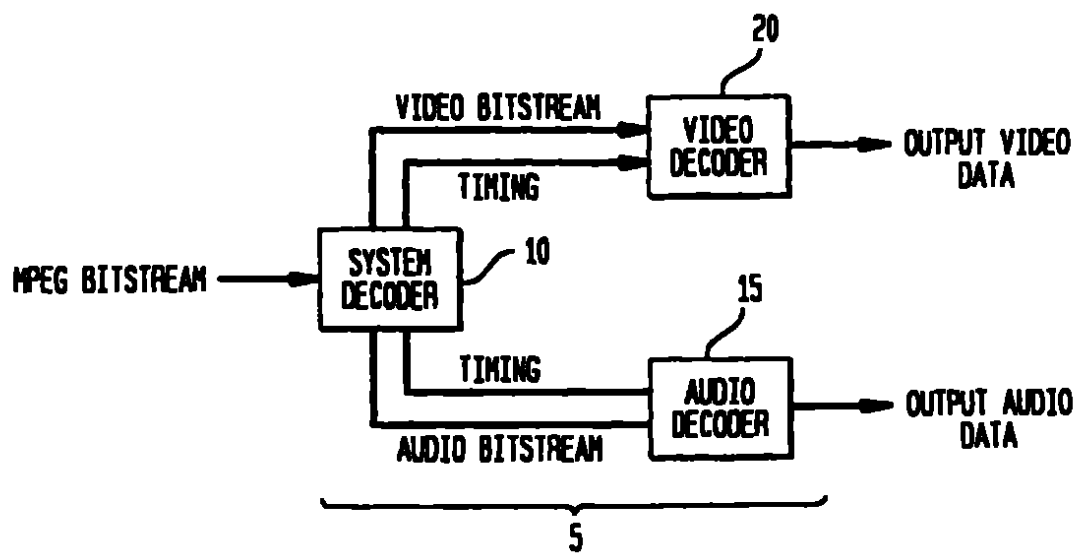
45

50

55

13

FIG. 1



243

FIG. 2

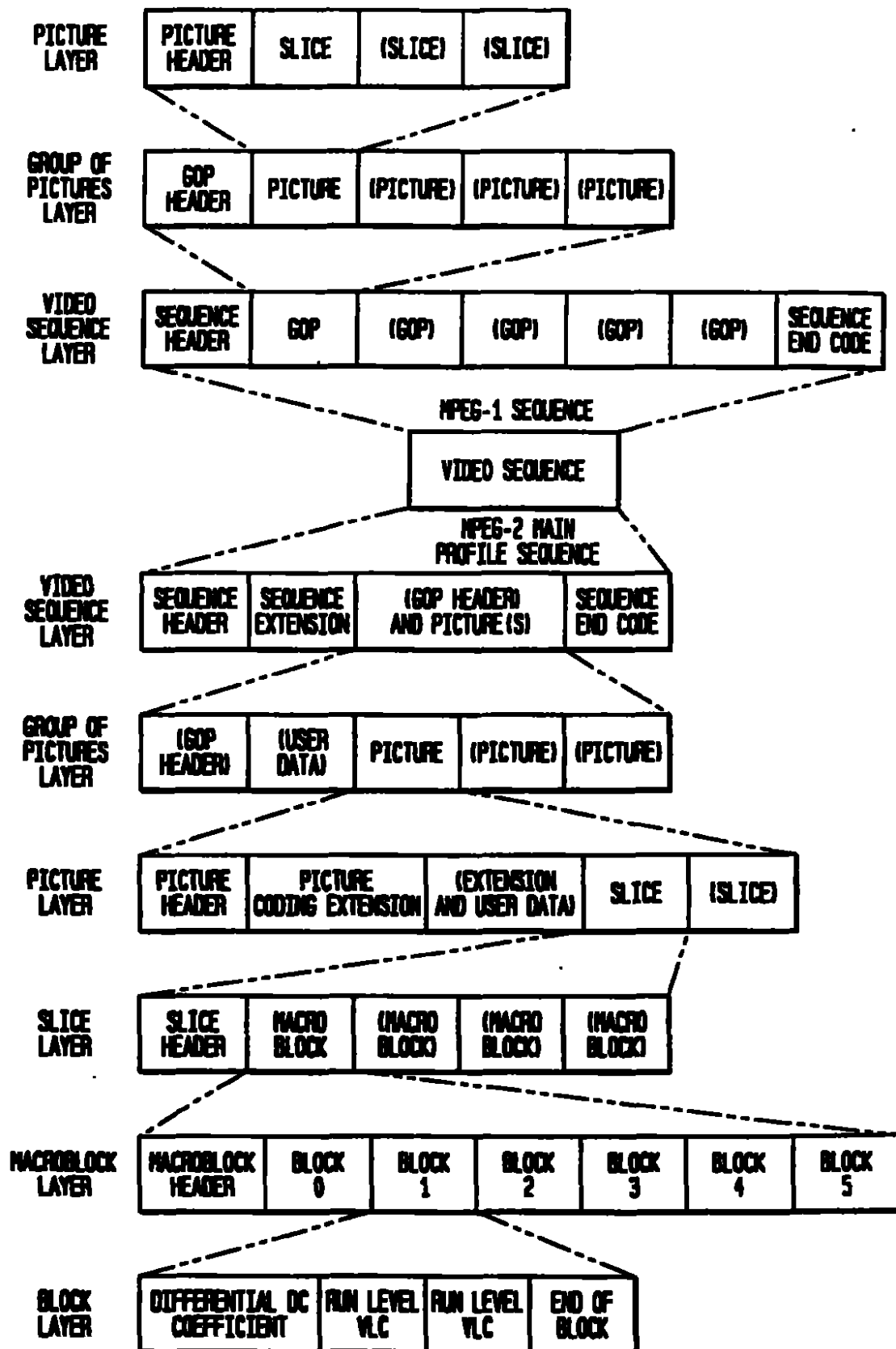


FIG. 3

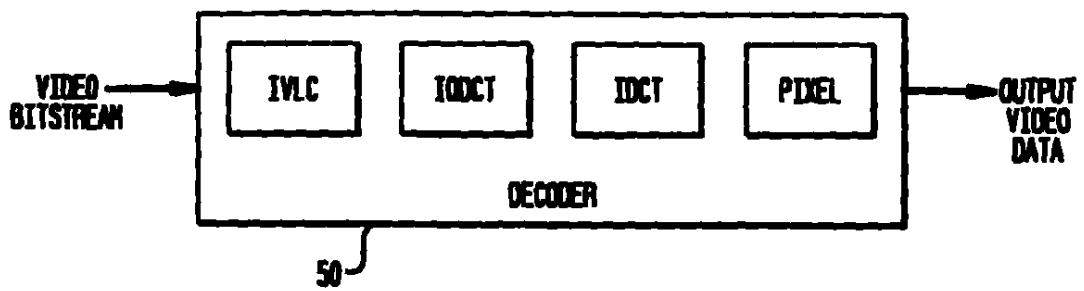


FIG. 7

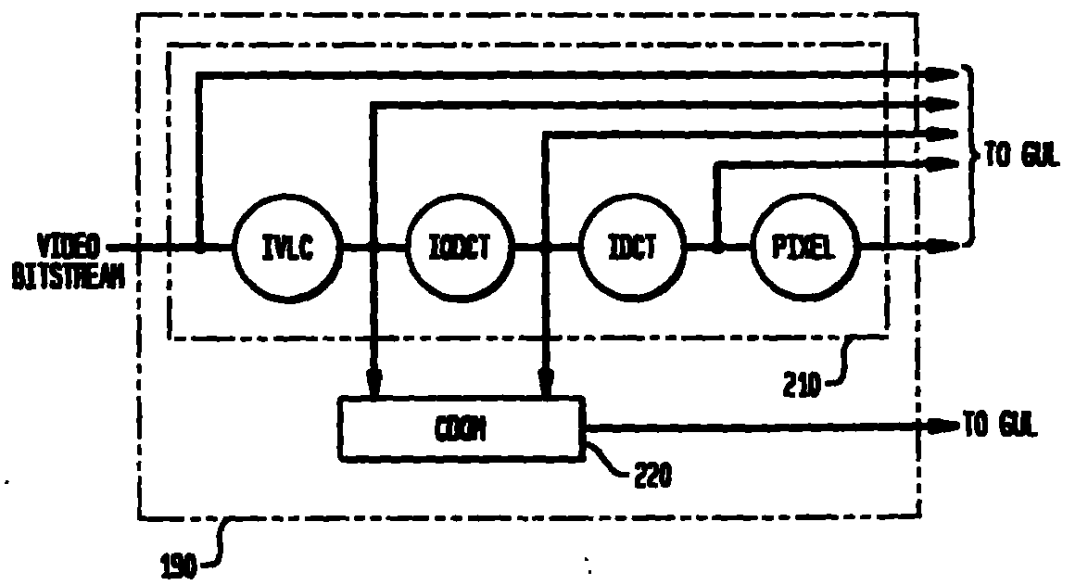


FIG. 4

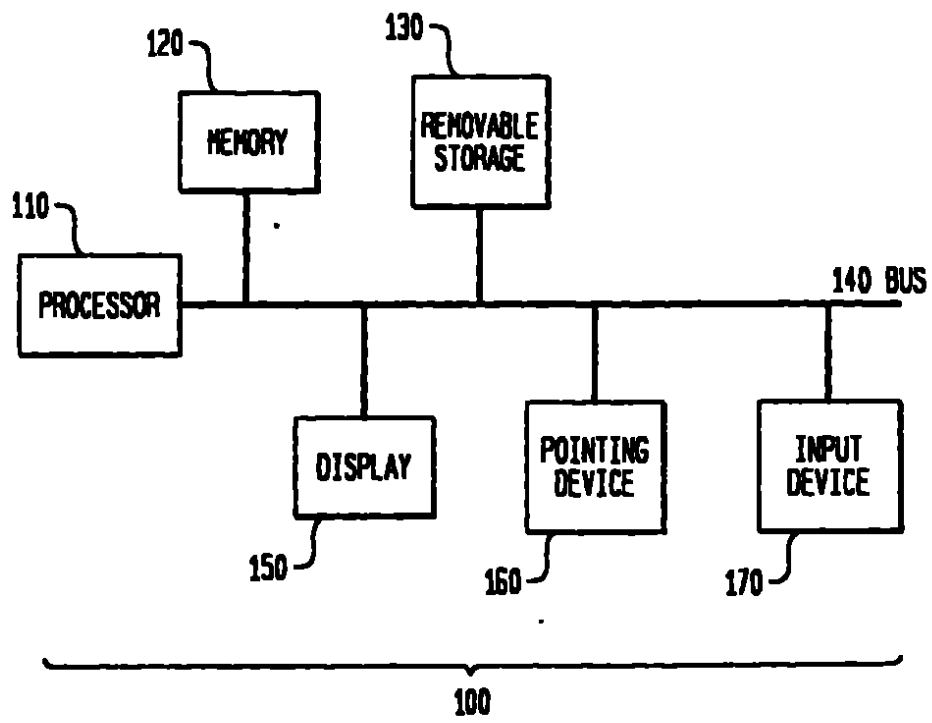


FIG. 5

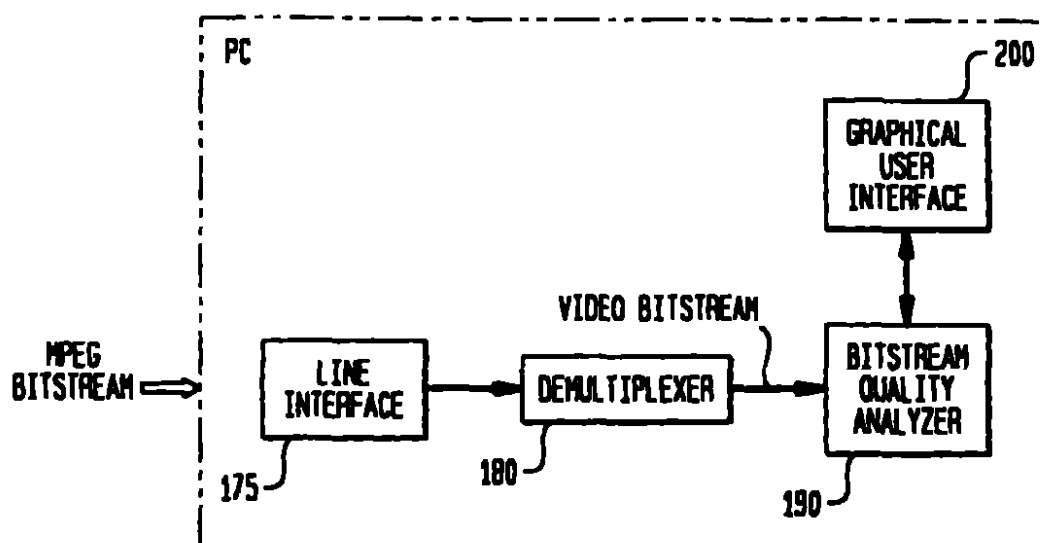
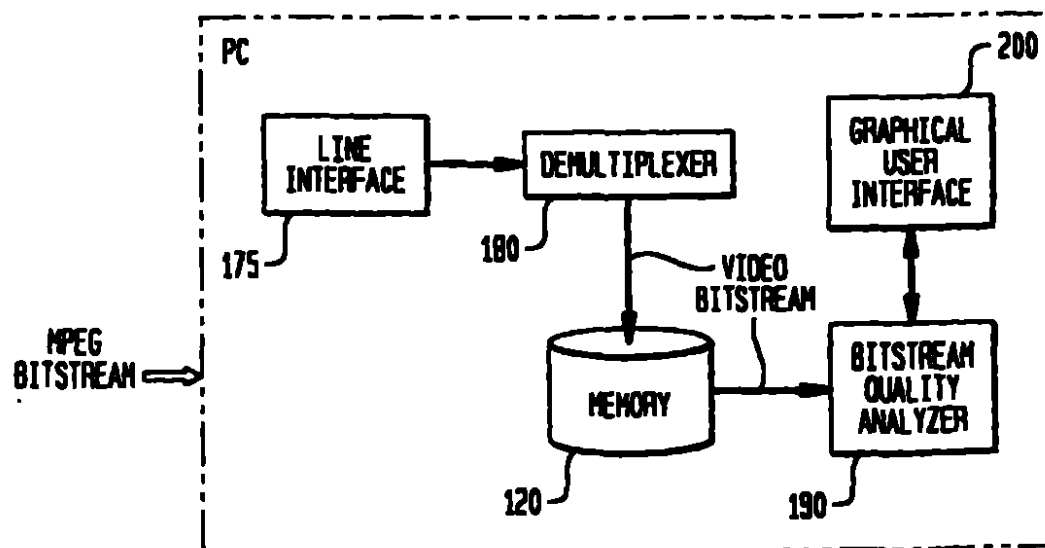
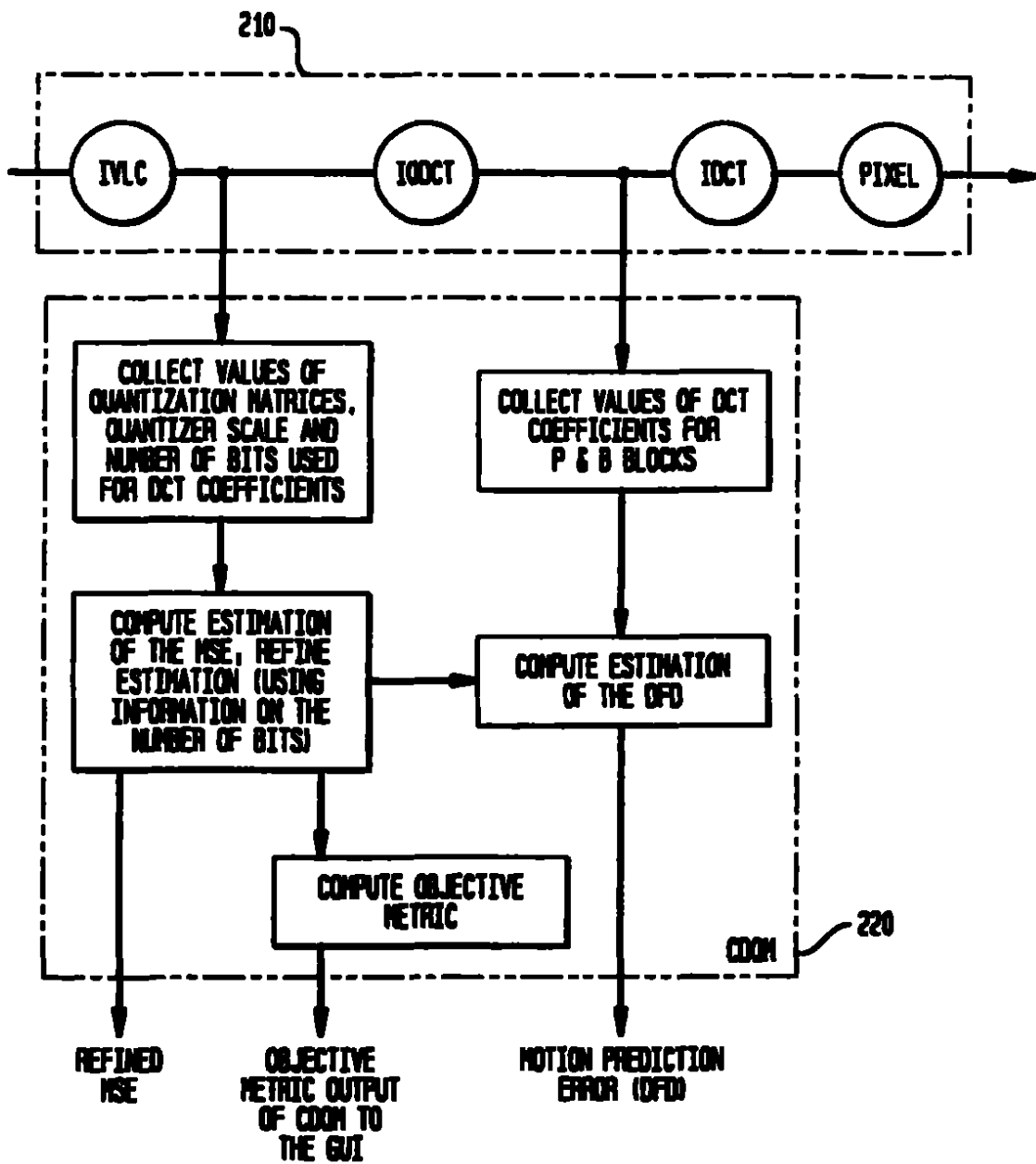


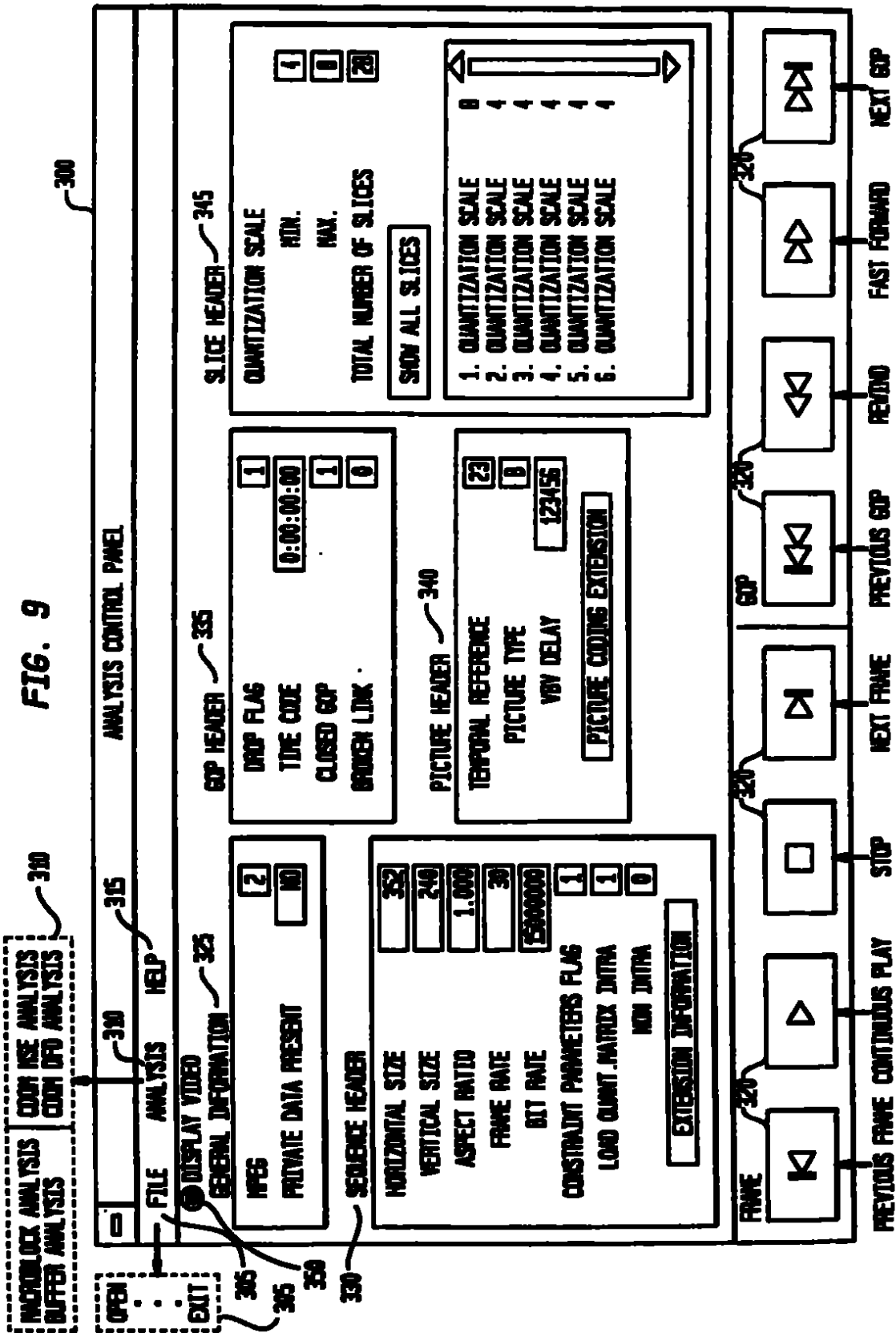
FIG. 6



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FIG. 8





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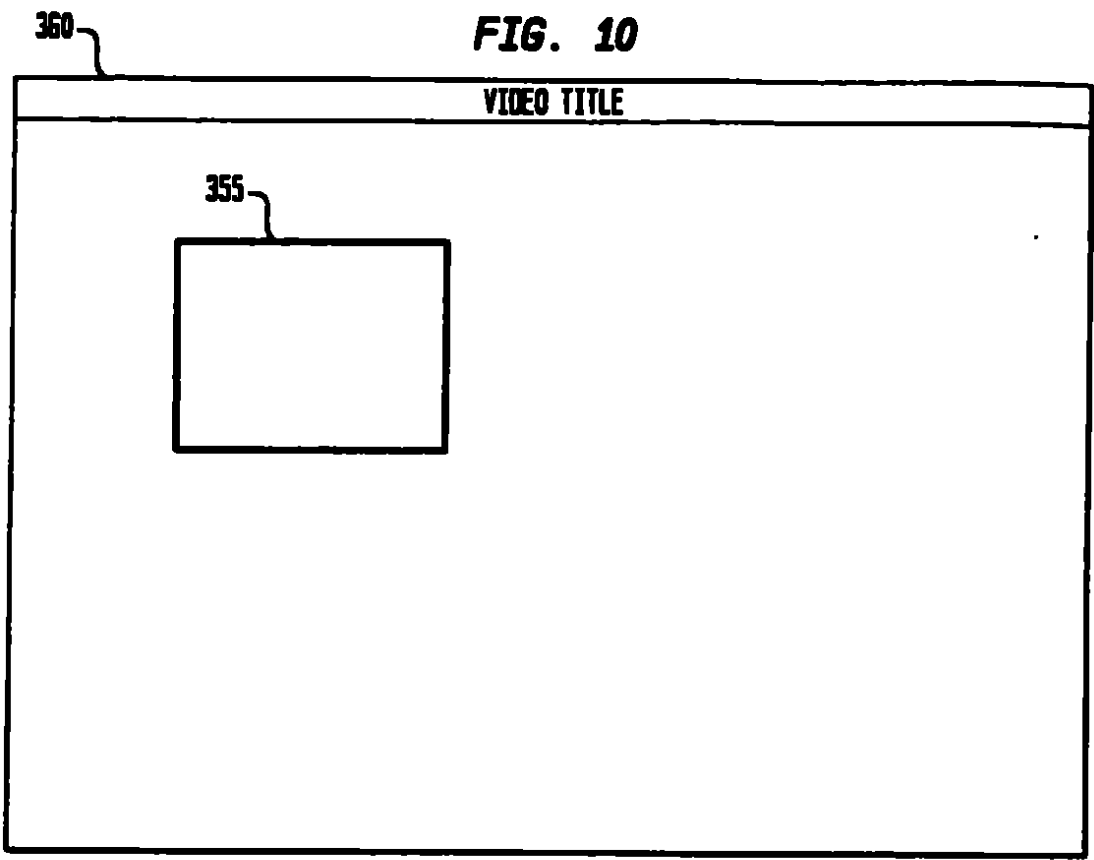


FIG. 11

365

SEQUENCE EXTENSION

PROFILE	HP	LEVEL	HL
PROGRESSIVE SEQUENCE	1		
CHROMA FORMAT	4:2:0		
HORIZONTAL SIZE EXTENSION	2		
VERTICAL SIZE EXTENSION	2		
BIT RATE EXTENSION	8100		
VBV BUFFER SIZE EXTENSION	510		
LOW DELAY	1		
FRAME RATE EXTENSION n	3		
FRAME RATE EXTENSION d	60		

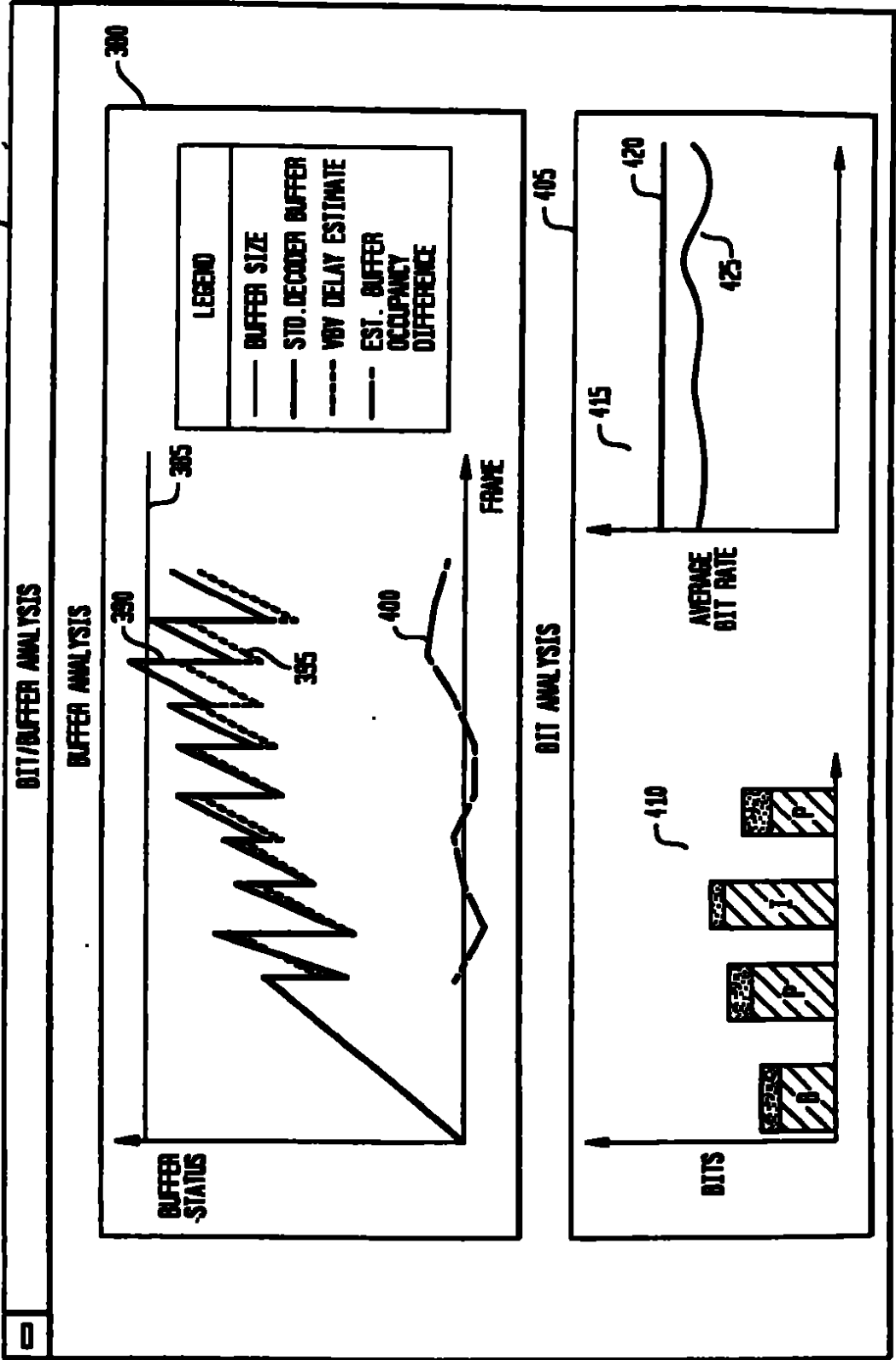
FIG. 12

370

PICTURE CODING EXTENSION

f_code[0][0]	15
f_code[0][1]	15
f_code[1][0]	15
f_code[1][1]	15
INTRA DC PRECISION	8
PICTURE STRUCTURE	TOP FIELD
TOP FIELD FIRST	0
FRAME PRED FRAME DCT	1
CONCEALMENT MOTION VECTORS	0
Q SCALE TYPE	0
INTRA VLC FORMAT	0
ALTERNATE SCAN	0
REPEAT FIRST FIELD	1
CHROMA 420 TYPE	1
PROGRESSIVE FRAME	1
COMPOSITE DISPLAY FLAG	0

FIG. 13



247

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FIG. 14

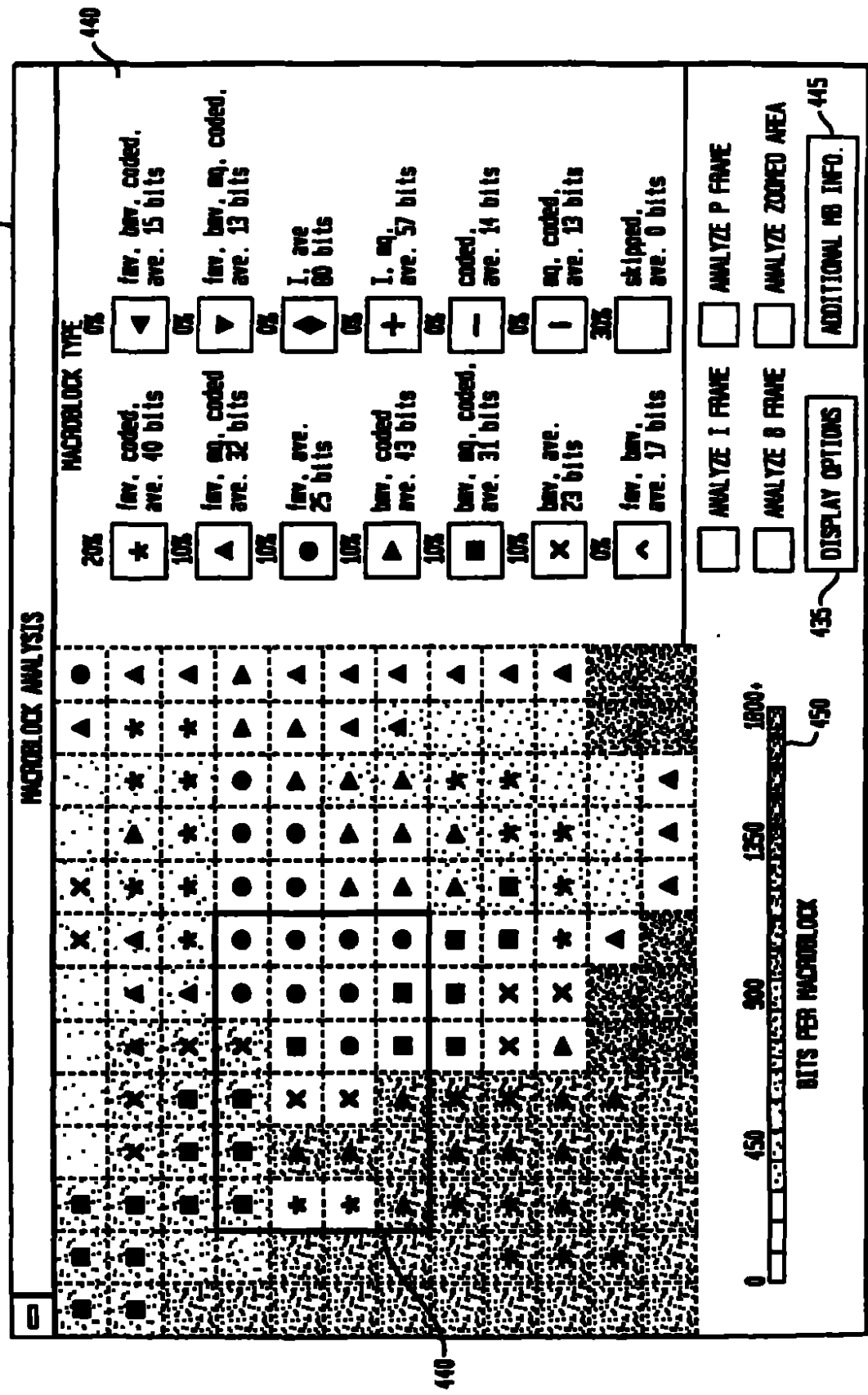
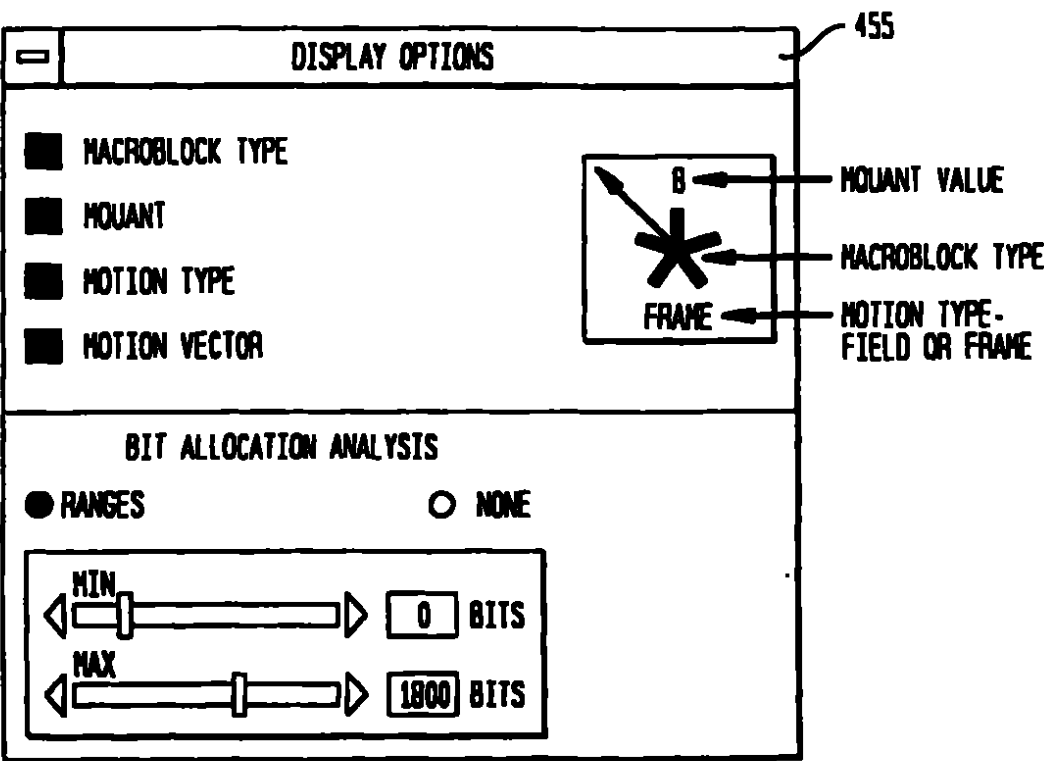


FIG. 15



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FIG. 16

460

ADDITIONAL MACROBLOCK INFORMATION

☒ MACROBLOCK PATTERN

1

☒ DCT TYPE

0

☒ MOTION VERTICAL SELECT

FORWARD

BACKWARD

TOP FIELD/FRAME

BOTTOM FIELD

☒ MOTION VECTORS

FORWARD

BACKWARD

TOP FIELD/FRAME

(5.6)

(5.6)

BOTTOM FIELD

☒ DCT DC PRECISION

8

☒ DUAL PRIME PREDICTION

0

☒ DCT COEFFICIENTS

4

BLOCK

3.1245673.1245673.1245673.124567

3.1245673.1245673.1245673.124567

3.1245673.1245673.1245673.124567

3.124567

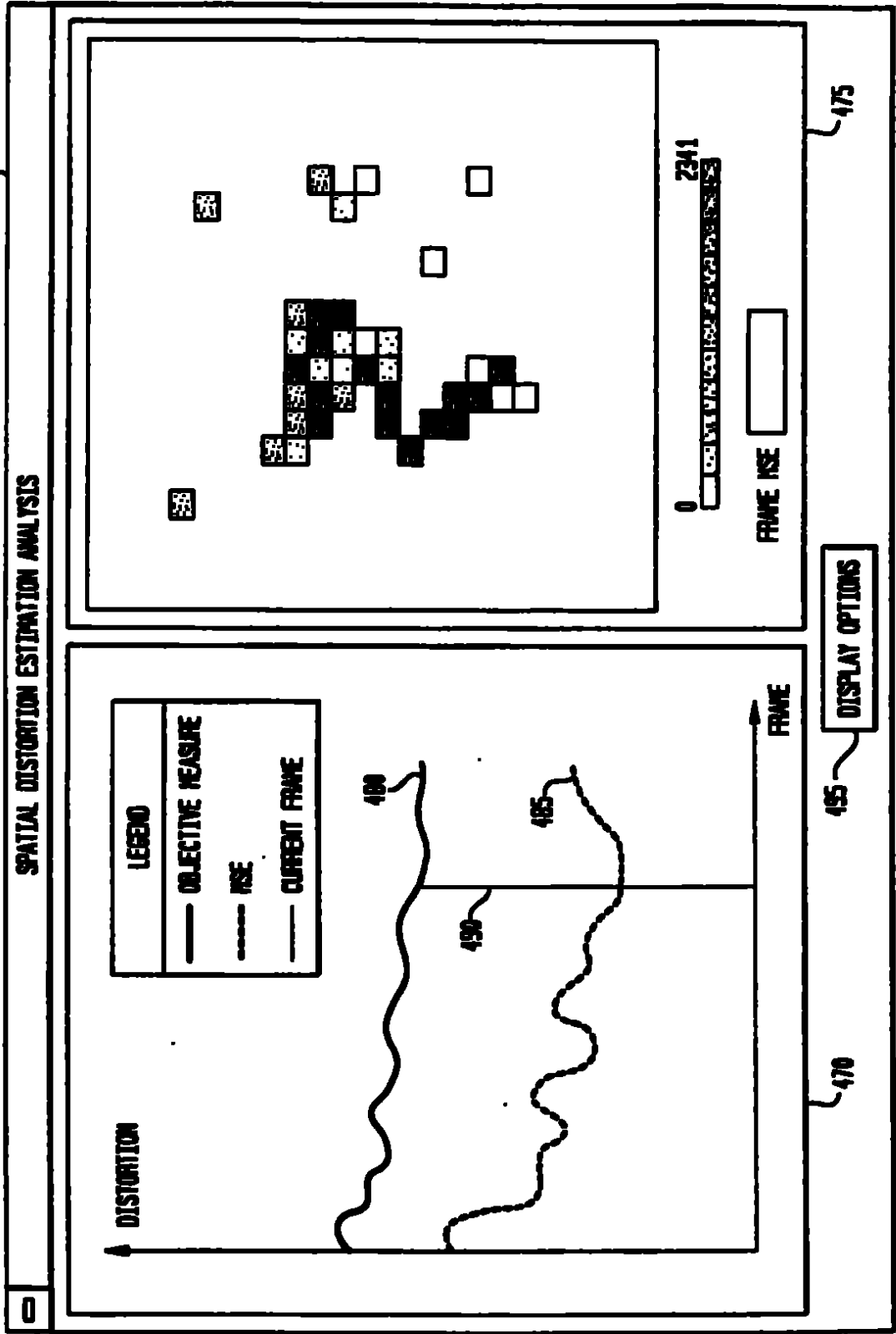
3.124567

3.124567

3.124567

3.1245673.124567

FIG. 17



249

FIG. 18

500

SPECIAL DISTORTION DISPLAY OPTIONS

☒ Y ☐ Cr ☐ Cb

FRAME

☒ MSE
☒ OBJECTIVE MEASURE

☒ DISTORTION
☐ DECIBELS

BLOCK

☒ MSE
☐ OBJECTIVE MEASURE

MIN MAX

FIG. 20

535

DFD PREDICTED ERROR DISPLAY OPTIONS

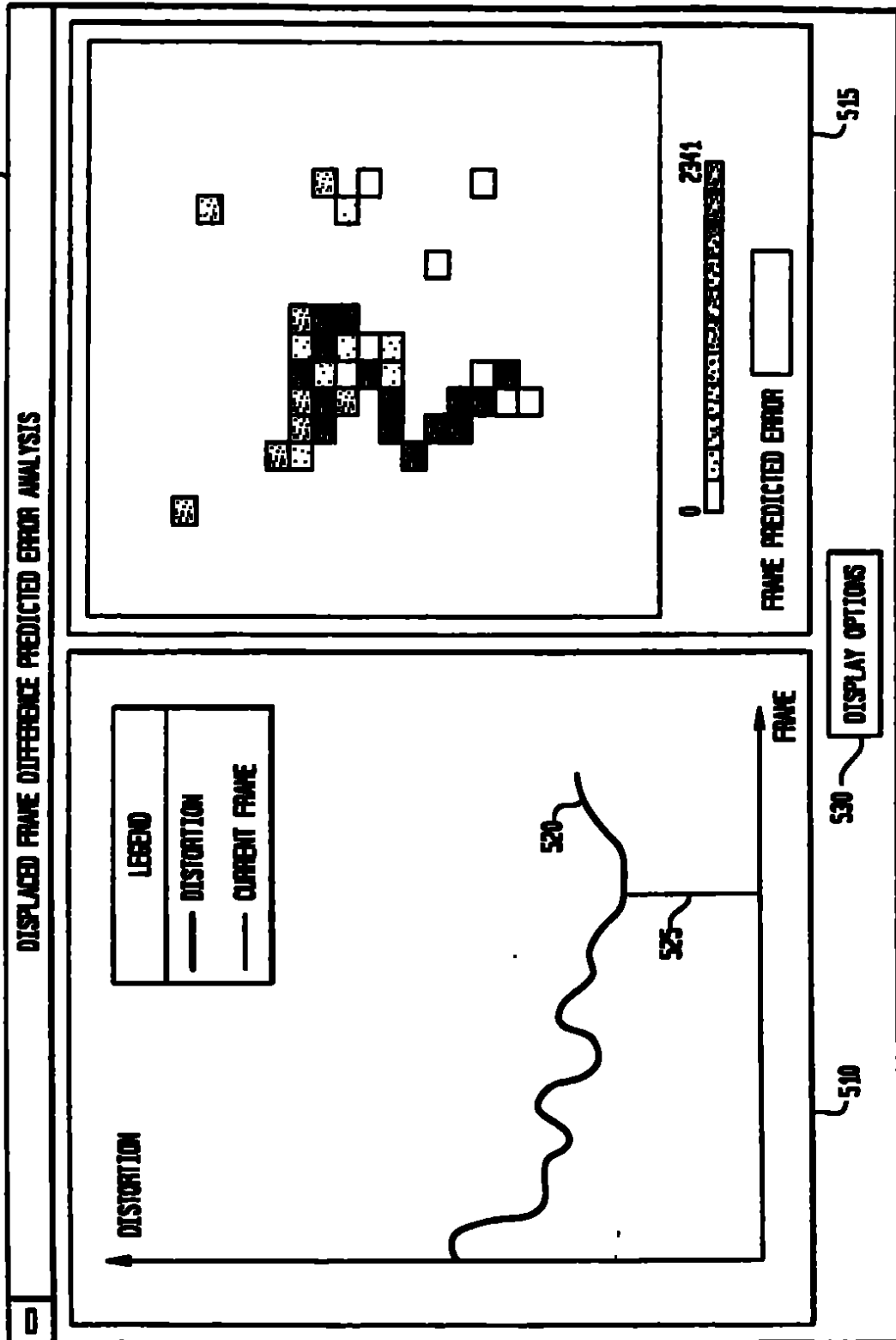
FRAME

☒ DISTORTION
☐ DECIBELS

BLOCK

MIN MAX

FIG. 19



PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 29471/37034	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/US01/09734	International filing date (day/month/year) 27/03/2001	Priority date (day/month/year) 18/04/2000
International Patent Classification (IPC) or national classification and IPC H04L27/02		
Applicant ZENITH ELECTRONICS CORPORATION		
1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36. 2. This REPORT consists of a total of 4 sheets, including this cover sheet. ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 807 of the Administrative Instructions under the PCT). These annexes consist of a total of sheets.		
3. This report contains indications relating to the following items: - I ☒ Basis of the report - II ☐ Priority - III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability - IV ☐ Lack of unity of invention - V ☐ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement - VI ☐ Certain documents cited - VII ☐ Certain defects in the international application - VIII ☐ Certain observations on the international application		
Date of submission of the demand 05/10/2001	Date of completion of this report 11.07.2002	
Name and mailing address of the international preliminary examining authority:  European Patent Office D-80298 Munich Tel. +49 89 2369 - 0 Tlx 523658 epmu d Fax: +49 89 2369 - 4465	Authorized officer Snell, T Telephone No. +49 89 2369 8902 	

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT**

International application No. PCT/US01/09734

I. Basis of the report

1. With regard to the elements of the international application (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*)

Description, pages:

1-45 as originally filed

Claims, No.:

1-19 as originally filed

Drawings, sheets:

1/12-12/12 as originally filed

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
☐ the language of publication of the international application (under Rule 48.3(b)).
☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
☐ filed together with the international application in computer readable form.
☐ furnished subsequently to this Authority in written form.
☐ furnished subsequently to this Authority in computer readable form.
☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
☐ the claims, Nos.:

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT**

International application No. PCT/US01/09734

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☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

☐ the entire international application.

☒ claims Nos. 1-19.

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (*specify*):

☒ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. 1-19 are so unclear that no meaningful opinion could be formed (*specify*):
see separate sheet

☒ the claims, or said claims Nos. 1-19 are so inadequately supported by the description that no meaningful opinion could be formed.

☐ no international search report has been established for the said claims Nos. .

2. A meaningful international preliminary examination cannot be carried out due to the failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

☐ the written form has not been furnished or does not comply with the standard.

☐ the computer readable form has not been furnished or does not comply with the standard.

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT - SEPARATE SHEET**

International application No. PCT/US01/09734

Re Item III

**Non-establishment of opinion with regard to novelty, inventive step and
Industrial applicability**

1. The formulation of claim 1 is too obscure and lacking support in the description to enable a meaningful opinion as to novelty and inventive step to be formed, for the following reasons (Article 6 PCT).
 - (i) It is not clear what should be understood by the terms "first and second data" in the context of the embodiments described (for example, this could relate to data decoded by the inner and outer decoders, or to data from different sources, eg video and auxiliary data (cf fig. 3 "Discard:")).
 - (ii) Furthermore, there is no apparent support in the description for their having different bit rates, since the input signal contains data at a particular single symbol rate.
 - (iii) It is unclear what the purpose of the "first data" is, since they play no role in the method as currently claimed.
 - (iv) The feature "in response to the input and the decoder" is not clear or supported by the description; the embodiment of claim 1 appears to be based on figure 19, but this embodiment does not show the prediction enhancer as being responsive to the input signal. Moreover it is not clear which decoder is referred to.
2. As claims 2-19 are dependent on claim 1, they suffer from the same objection of lack of clarity and support as claim 1 (Article 6 PCT).

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TRATADO DE COOPERACIÓN DE PATENTES

PCT

INFORME DEL EXAMEN INTERNACIONAL PRELIMINAR

(PCT Artículo 36 y Regla 70)

Referencia del archivo del solicitante o del agente:

29471/37034

Solicitud de Patente Internacional:

PCT/US01/09734

Fecha de presentación internacional: 27/03/2001

Fecha de prioridad: 18/04/2000

Clasificación de Patente Internacional(IPC) o clasificación nacional IPC: **H04L27/02**

Solicitante: **ZENITH ELECTRONICS CORPORATION**

...

3. Este informe contiene indicaciones relacionadas con los siguientes ítems:

I ☒ Base del reporte

III ☒ No se estableció una opinión con relación a la novedad, el paso inventivo y la aplicabilidad industrial

...

M. P. Johnson
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EXAMINADOR
EXAMEN OFICIAL
Washington, D. C. 20540



Fecha de presentación:

05/10/2001

Fecha en que se completó este
informe:

11.07.2002

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I. Base del Informe

1. Descripción, páginas:

1-45 tal como se presentaron originalmente

Reivindicaciones Nos.:

1.19 tal como se presentaron originalmente

Hojas de dibujos:

1/12-12/12 tal como se presentaron originalmente

2. Con relación al idioma, todos los elementos marcados arriba se suministraron a esta Autoridad en el idioma en que se presentó la solicitud original, a menos que se indique algo diferente en este ítem.

...

3. Con relación a cualquier secuencia nucleótida y/o de aminoácido revelada en la solicitud internacional, el examen internacional preliminar se llevó a cabo sobre la base de la secuencia, listando lo siguiente:

(aparecen seis casillas, pero no está marcada ninguna de ellas)

...

III. No se estableció una opinión con relación a la novedad, el paso inventivo y la aplicabilidad industrial

...

☒ Reivindicaciones Nos. 1-19.

Porque:

☒ La descripción, reivindicaciones o dibujos (*indicar los elementos particulares a continuación*) o las mencionadas reivindicaciones Nos. 1-19 son confusas y no se pudo expedir una opinión significativa (especificar):
ver hoja separada

☒ Las reivindicaciones Nos. 1-19 están tan inadecuadamente sustentadas por la descripción que no se pudo formar una opinión con significado.

...

Re ítem III

...

1. La formulación de la reivindicación 1 es demasiado oscura y carece de soporte en la descripción para permitir una opinión significativa en cuanto a la novedad y paso inventivo, por las siguientes razones: (Artículo 6 del PCT).

- (i) no es claro lo que debe entenderse por los términos "primeros y segundos datos" en el contexto de las incorporaciones descritas (por ejemplo, esto podría relacionarse con datos decodificados por decodificadores internos y externos, o con datos de diferentes fuentes, como por ejemplo video y datos auxiliares (cf fig. 3 "Descartar..."))).
- (ii) Además, no existe un soporte evidente en la descripción para que tengan diferentes tasas de bits, puesto que la señal de entrada contiene datos a una tasa de símbolo particular simple.
- (iii) No es claro cuál es el propósito de los "primeros datos" puesto que no juegan ningún papel en el método, tal como actualmente se reivindica.
- (iv) La característica "en respuesta a la entrada y al decodificador" no es clara ni está sustentada por la descripción; la incorporación de la reivindicación 1 parece basarse en la figura 19, pero no muestra la mejora de la predicción como una respuesta a la señal de entrada. Además no es claro a qué decodificador se refiere.

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2. Como las reivindicaciones 2-19 dependen de la reivindicación 1, sufren de la misma objeción de carencia de claridad y de soporte de la reivindicación 1 (Artículo 6 PCT).

María del Pilar Iglesias
María del Pilar Iglesias

María del Pilar Iglesias
C. C. 41.339.183 de Bogotá
Intérprete Oficial según Resolución No. 819 de
15 de Abril de 1971 del Ministerio de Justicia

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**(12) SOLICITUD INTERNACIONAL PUBLICADA BAJO EL TRATADO DE
COOPERACIÓN DE PATENTES (PCT)**

(19) Organización Mundial de Propiedad Intelectual

Oficina Internacional

(43) Fecha de Publicación Internacional:

25 de octubre de 2001 (25.10.2001)

(10) Número de Publicación Internacional

WO 01/78495 A2

(51) Clasificación Internacional de Patente: No se Clasificó

(21) Número de Solicitud Internacional: PCT/US01/09734

(22) Fecha de Presentación Internacional:

27 de marzo de 2001 (27.03.2001)

(25) Idioma del Registro: Inglés

(26) Idioma de la Publicación: Inglés

(30) Datos de Prioridad

60/198.014 18 de abril de 2000 (18.04.2000) US

60/255.476 13 de diciembre de 2000 (13.12.2000) US

60/255.464 13 de diciembre de 2000 (13.12.2000) US

09/804.237 13 de marzo de 2001 (13.03.2001) US

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(81) **Estados Designados (nacionales):** AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, L., LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) **Estados Designados (regionales):** Patente ARIPO (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Patente Euroasiática (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), Patente Europea (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), Patente OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Publicado:

- sin informe de búsqueda internacional y se volverá a publicar cuando se reciba ese informe.

Para los códigos de dos letras y para las demás abreviaturas refiérase a la "Guía de Notas sobre los Códigos y Abreviaturas" que aparece al comienzo de cada emisión regular de la Gaceta del PCT.

(54) **Título: RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES**

(57) **Resumen:** La predicción mejorada de secciones se basa en datos VSB 8 ATSC cuando los datos robustos VSB 8 no están disponibles y se basa en datos robustos VSB 8 cuando estos están disponibles.

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RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

Solicitudes Relacionadas

Esta solicitud reivindica el beneficio la Solicitud Provisional Norteamericana No. 60/198.014, presentada el 18 de abril de 2000, la Solicitud Provisional Norteamericana No.

60/255.476 presentada el 13 de diciembre de 2000 y la
Solicitud Provisional Norteamericana No. 60/255.464
presentada el 13 de diciembre de 2000.

Campo Técnico del Invento

Este invento está relacionado con la transmisión y/o
recepción de datos digitales.

Antecedentes del Invento

La norma para transmisión de señales digitales de
televisión en los Estados Unidos se conoce como datos 8 VSB
(Norma A/53 para Televisión Digital ATSC). Estos datos 8 VSB
tienen una constelación que consiste de ocho niveles de
símbolos posibles. En un sistema VSB los ocho millones de
símbolos posibles se encuentran todos en la misma fase. Sin
embargo, en un sistema QAM, los símbolos se transmiten en una
relación de fase de cuadratura.

La norma arriba indicada especifica el formateo y
modulación de datos digitales de video y audio. Los datos se
transmiten en la forma de símbolos con cada símbolo
representando dos bits de datos que son cuadrículas
codificadas en tres bits de datos codificados en cuadrícula.
Cada tres bits de datos codificados en cuadrícula se mapean
en un símbolo que tiene un nivel correspondiente entre los

ocho niveles. La codificación e intercalación Reed/Solomon también se proveen para incrementar la robustez de la información transmitida.

Los datos auxiliares (diferentes de video digital o datos de audio) también pueden transmitirse en un canal de televisión digital. Estos datos se formatean y modulan de conformidad con la norma en la misma forma que los datos de video y audio. Los receptores fabricados de conformidad con la norma 8 VSB pueden leer identificaciones de paquetes (PIDs) que les permiten diferenciar entre datos de audio, video y datos auxiliares.

Sin embargo, mientras que la robustez de las señales de televisión digital transmitidas es suficiente para la recepción de televisión digital, esta robustez puede no ser suficiente para la transmisión de datos auxiliares, particularmente cuando dichos datos sean críticos. De acuerdo con lo anterior, una de las aplicaciones del presente invento es la transmisión de datos auxiliares en un formato VSB con codificación exterior para mayor robustez. Los datos auxiliares transmitidos de acuerdo con la aplicación del presente invento se referirán en este documento como los datos VSB robustos (RVSB).

Resumen del Invento

En un aspecto del presente invento un método para proporcionar predicción mejorada de secciones comprende lo siguiente: recibir una entrada que contiene los primeros y los segundos datos, en donde los primeros y los segundos datos tienen diferentes tasas de bits y están definidos por la misma contestación de nivel n ; decodificar únicamente los segundos datos con un decodificador; producir una salida en respuesta a la entrada y al decodificador en donde la salida está confinada a al menos uno pero menos de $n/2$ de los niveles de constelación n y en donde $n > 2$; y proporcionar la salida como la predicción mejorada de secciones.

En otro aspecto del presente invento un aparato para proporcionar la predicción mejorada de secciones comprende un decodificador interno, un decodificador externo y un predictor mejorado de secciones. El decodificador interno codifica una señal recibida para proporcionar una salida interna decodificada. El decodificador interno produce $n/2$ estados de decodificación posibles con base en la señal recibida y la señal recibida contiene datos con n niveles en donde $n > 2$. El decodificador externo decodifica externamente la salida decodificada interna. El predictor mejorado de

secciones elige al menos uno pero menos de $n/2$ de los $n/2$ estados de decodificación posibles con base en una salida del decodificador externo y proporciona el estado o estados elegidos como la predicción mejorada de secciones.

En otro aspecto del presente invento, un aparato que suministra la predicción mejorada de secciones incluye un decodificador interno, un decodificador externo y un predictor mejorado de secciones. El decodificador interno decodifica una señal recibida que contiene los primeros y los segundos datos para proporcionar dichos datos decodificados internamente. El decodificador externo decodifica externamente únicamente los segundos datos. El predictor mejorado de secciones proporciona una salida de predicción con base en los primeros datos cuando los segundos datos no están disponibles y con base en los segundos datos decodificados externamente cuando los segundos datos están disponibles.

Breve Descripción del Plano

Estas y otras características y ventajas serán más visibles desde una consideración detallada del invento cuando sean tomadas en su conjunto con el plano en el cual:

La Figura 1 muestra un transmisor VSB robusto para transmisión de datos VSB robustos y datos ATSC de conformidad con el presente invento;

La Figura 2 muestra un receptor estándar ATSC para recibir los datos ATSC transmitidos por el transmisor VSB robusto de la Figura 1;

La Figura 3 muestra un receptor VSB robusto para el recibo de datos VSB robustos transmitidos por el transmisor VSB robusto de la Figura 1;

La Figura 4 muestra el codificador con tasa de 2/3 de tasa de la Figura 1 con detalles adicionales;

La Figura 5 muestra la función de mapeo desempañada por el mapeador de la Figura 4;

La Figura 6 muestra la operación de los decodificadores de tasa 2/3 de las Figuras 2 y 3;

La Figura 7 muestra otro transmisor VSB robusto para transmitir datos VSB robustos y datos ATSC de acuerdo con el presente invento.

La Figura 8 muestra un receptor ATSC estándar para recibir los datos ATSC transmitidos por el transmisor VSB robusto de la Figura 7;

La Figura 9 muestra un receptor VSB robusto para recibir los datos VSB robustos transmitidos por el transmisor VSB robusto de la Figura 7;

La Figura 10 muestra un circuito para la generación de la señal de control adecuada en la línea de control de descarte de la Figura 9;

La Figura 11 muestra otro transmisor VSB robusto para la transmisión de datos VSB robustos y de datos ATSC de acuerdo con el presente invento;

La Figura 12 muestra un ejemplo de cuatro segmentos de datos que contienen datos codificados externos de tasa 1/2 que pueden transmitirse por un transmisor VSB robusto de acuerdo con el presente invento;

La Figura 13 muestra un ejemplo de cuatro segmentos de datos que contienen datos codificados externos de tasa 1/4 que pueden transmitirse mediante un transmisor VSB robusto de acuerdo con el presente invento;

La Figura 14 muestra un ejemplo de cuatro segmentos de datos que contienen datos codificados externos de tasa 3/4 que pueden transmitirse mediante un transmisor VSB robusto de conformidad con el presente invento;

La Figura 15 muestra los intercaladores (I_r) de las Figuras 1, 9 y 11 con mayor detalle;

La Figura 16 muestra los desintercaladores (D_r) de las Figuras 3 y 9 con más detalle;

La Figura 17 muestra una estructura de definición de mapa de un primer paquete de datos VSB robustos de una trama;

La Figura 18 muestra una parte del segmento sincronizado de una trama que porta un mapa que indica en qué parte de la trama pueden encontrarse los datos VSB robustos;

La Figura 19 ilustra un predictor mejorado de secciones de acuerdo con una incorporación del presente invento;

La Figura 20 muestra las cuadrículas del decodificador interno de la Figura 19;

La Figura 21 muestra transiciones de estado posibles para el decodificador externo de la Figura 19; y

La Figura 22 ilustra un predictor mejorado de secciones de acuerdo con otra incorporación del presente invento.

Descripción Detallada

Transmisión y Recepción de Datos RVSB y ATSC

La Figura 1 muestra un transmisor VSB (10) que transmite tanto datos ATSC como datos VSB robustos de acuerdo con una incorporación del presente invento. La Figura 2 muestra un receptor ATSC estándar (12) que recibe los datos ATSC transmitidos por el transmisor VSB robusto (10), y la Figura 3 muestra un receptor VSB robusto (14) que recibe los datos VSB robustos transmitidos por el transmisor VSB robusto (10).

El transmisor VSB robusto (10) incluye un codificador Reed/Solomon (16) que codifica los bytes de datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a los bytes de datos auxiliares no codificados. Los bytes de datos auxiliares no codificados y los bytes de paridad Reed/Solomon son intercalados por un intercalador (18). Entonces los bytes de datos auxiliares sin codificar intercalados y los bytes de paridad Reed/Solomon se codifican con bits por un codificador externo (20) utilizando ya sea un código convolucional u otro código de corrección de errores. El codificador externo (20) mejora la robustez de los bytes

de datos auxiliares no codificados y de los bytes de paridad Reed/Solomon, convirtiéndolos en bytes de datos robustos (en adelante denominados bytes de datos VSB robustos) y en bytes de paridad Reed/Solomon.

El codificador externo (20) puede por ejemplo, ser un codificador con una tasa de $1/2$ que produzca dos bits de salida por cada bit de entrada, o un codificador, con una tasa de $1/4$ que produzca cuatro bits de salida por cada bit de entrada, o un codificador con tasa de $3/4$ de tasa que produzca 4 bits de salida por cada tres bits de entrada. Otros codificadores podrán utilizarse en lugar de estos.

En la salida del codificador externo (20), se adiciona una cabecera de transporte (tx) de tres bytes a cada grupo de 184 datos VSB robustos codificados y bytes Reed/Solomon para formar paquetes de datos VSB robustos. Un multiplexor (24) multiplexa estos paquetes de datos VSB robustos con paquetes de datos ATSC (típicamente video y audio) cada uno de los cuales comprende una cabecera de transporte de tres bytes y 184 bytes de datos ATSC. Cualquiera de estas entradas al multiplexor (24) puede seleccionarse sobre la base de paquete por paquete y cada entrada seleccionada se suministra a un transmisor ATSC (26). La selección por parte del multiplexor

(24) por cuya entrada pasa hacia el transmisor ATSC (26) está basada en un mapa VSB robusto que se describirá más adelante.

El transmisor ATSC (26), típicamente incluye un codificador (28) Reed/Solomon, un intercalador (30) y un codificador interno (32) de tasa 2/3, todo lo cual opera de conformidad con la norma ATSC.

Un receptor de la norma ATSC, tal como el receptor (12) de la norma ATSC que aparece en la Figura 2, recibe y procesa los datos ATSC y descarta los datos VSB robustos. De acuerdo con lo anterior, el receptor de la norma ATSC (12) incluye un decodificador interno de tasa 2/3 (34), un desintercalador (36) y un decodificador Reed/Solomon (38) todos los cuales operan de conformidad con la norma ATSC. Sin embargo, el receptor de la norma ATSC (12) está programado para decodificar las cabeceras de transporte de datos VSB robustos y de datos ATSC (lo cual incluye el paquete de identificaciones o PIDs que no han sido codificados por el codificador externo (20)). El receptor de la norma ATSC (12) lee los PIDs de todos los paquetes y en el (40), descarta aquellos paquetes que tengan los PIDs de datos VSB robustos. El receptor de la norma ATSC (12) incluye también un predictor de secciones (42) (tal como el predictor de

secciones de la Patente Norteamericana No. 5.923.711) que responde a los datos decodificados internos y que proporciona una salida de vuelta al rastreador de fase y/o ecualizador, tal como se conoce en la técnica.

Los paquetes de datos VSB robustos pueden recibirse, decodificarse y procesarse por un receptor VSB robusto tal como el receptor VSB robusto (14) que se muestra en la Figura 3. Como se conoce y como se muestra en la Figura 4, el codificador interno de tasa 2/3 (32) del transmisor ATSC (26) incluye un precodificador (44) y un codificador de cuadrículas de cuatro estados (46). En combinación, el precodificador (44) y el codificador de cuadrícula de cuatro estados (46) puede considerarse como un codificador de ocho estados que produce tres bits de salida codificados con cuadrícula (Z0 Z1 Z2) para cada dos bits de entrada (X1 X2). Un mapeador (48) mapea los tres bits de salida codificados con cuadrícula con un símbolo que tiene uno de ocho niveles en la forma en que se indica en la Figura 5. Tal como se conoce bien a partir de la teoría de código convolucional, la operación del precodificador (44) y del codificador de cuadrículas de cuatro estados (46) puede observarse como una cuadrícula cuaternaria de ocho estados.

Por consiguiente, en el receptor VSB robusto (14), un decodificador interno con tasa de $2/3$ (50) puede operar en cualquier cuadrícula cuaternaria (4-ary) de ocho estados que vea al precodificador (44) y al codificador de cuadrícula de cuatro estados (46) del codificador interno con tasa de $2/3$ en combinación, tal como se muestra en la Figura 6 para producir una decisión de salida blanda (utilizando por ejemplo, el algoritmo SSA en la forma descrita en la publicación "Detección de Salida Blanda Optima para Canales con Interferencia de Intersímbolo", Li, Vucetic, y Sato, IEEE Transacciones sobre la Teoría de la Información, Mayo de 1995). Esta operación de toma de decisiones blandas es más complicada que el algoritmo Viterbi ampliamente utilizado, que produce una salida de decisión dura, pero la operación de toma de decisión blanda aprovecha más ampliamente de ganancia de la codificación provista por el codificador externo (20).

La salida del decodificador interno con tasa de $2/3$ (50) se desintercala por un desintercalador (52). El receptor VSB robusto (14) lee los PIDs de todos los paquetes a la salida del desintercalador (52). Con base en estos PIDs el receptor VSB robusto (14) descarta estos paquetes en el (54) que tiene los PIDs de los datos ATSC y también descarta las cabeceras de transporte adicionadas posteriormente al codificador

externo (20) y los bytes de paridad adicionados por el codificador Reed/Solomon (28). Así, el receptor VSB robusto (14), en el (54), pasa únicamente los paquetes de datos VSB robustos que contienen los datos VSB robustos codificados por el codificador externo (20). Los paquetes de datos VSB robustos se decodifican por un decodificador externo (56), se desintercalan por un desintercalador (58) que es el inverso del intercalador (18) y Reed/Solomon se decodifica por un decodificador Reed/Solomon (60) para reconstruir los datos auxiliares no codificados originales provistos al codificador Reed/Solomon (16) de la Figura 1.

La salida confiable del decodificador externo (56) (que se puede utilizar en salida blanda o dura) es intercalada por un intercalador (62) (que corresponde al intercalador (30) en un trayecto de retroalimentación (64) con el fin restaurar el ordenamiento de los datos decodificados externos al orden de los datos en el canal. Estos datos decodificados externos intercalados pueden por ejemplo utilizarse por un predictor de secciones (66) para crear retroalimentación confiable a un rastreador de fase y/o ecualizador. Sin embargo, la demora de la retroalimentación general introducida por el desintercalador (52) y el intercalador (62) en el receptor VSB robusto (14) es generalmente muy larga para proporcionar

retroalimentación útil al rastreador de fase y/o al ecualizador.

El arreglo que se muestra en las Figuras 7, 8 y 9 evita la demora en la retroalimentación introducida por el desintercalador (52) y el intercalador (62) del receptor VSB robusto (14). La Figura 7 muestra un transmisor VSB robusto (80) en el cual los bytes de datos auxiliares no codificados se codifican por un codificador Reed/Solomon (82) que adiciona bytes de paridad Reed/Solomon a los bytes de datos auxiliares no codificados. Los bytes de datos auxiliares no codificados y los bytes de paridad Reed/Solomon son intercalados por un intercalador (84). Entonces, los bytes de datos auxiliares no codificados intercalados y los bytes de paridad Reed/Solomon se codifican en término de bits por un codificador externo (86), utilizando ya sea un código convolucional o un código de producto turbo, en la forma arriba indicada. La salida en términos de bits del codificador externo (86) es un pequeño bloque intercalado por un intercalador de bloques pequeño (88) con el fin de reducir el impacto de los errores de las ráfagas del canal en el decodificación externo. A los datos provistos por el intercalador de bloques pequeño (88) puede hacerse referencia

como Rdatos (n.o.) que corresponde a los datos VSB robustos ordenados normalmente.

Una entrada del primer multiplexor (92) recibe paquetes formateados ATSC cada uno de los cuales comprende (i) una cabecera válida de transporte de tres bytes con un número PID para datos VSB robustos, (ii) 184 bytes que sostienen lugares de datos VSB robustos simulados, y (iii) veinte bytes que sostienen lugares para datos de paridad Reed/Solomon ATSC simulados. La otra entrada del primer multiplexor (92) recibe paquetes simulados formateados ATSC, cada uno de los cuales tiene 207 bytes de datos ATSC simulados. Estos paquetes simulados formateados ATSC sirven como tenedores de lugares ("placeholders") para los paquetes ATSC reales que se añaden corriente abajo. Las entradas del primer multiplexor (92) pueden seleccionarse sobre la base de paquete por paquete y esta selección esta basada en el mapa VSB robusto que se describirá más adelante.

La salida seleccionada del primer multiplexor (92) es intercalada por un intercalador (94) de acuerdo con la Norma ATSC para intercalación convolucional de bytes. Un reemplazador de datos (96) recibe tanto la salida del intercalador (94) como la salida del intercalador de bloques

pequeños (88). El reemplazador de datos (96) reemplaza cada byte con lugar para tener datos VSB robustos simulados desde el intercalador (94) con los siguientes bytes de datos VSB robustos normalmente ordenados desde el intercalador de bloques pequeños (88).

La salida del reemplazador de datos (96) contiene datos VSB robustos normalmente ordenados con cabeceras de transporte entremezcladas, bytes de paridad Reed/Solomon ATSC simulados y bytes de paquetes de datos ATSC simulados. Un desintercalador (98), que opera de acuerdo con la Norma ATSC para la desintercalación de bytes, desintercala la salida del reemplazador de datos (96) para así "repaquetizar" de forma efectiva los datos como paquetes de cabeceras de transporte, o datos VSB robustos reordenados (Rdata(r.o.)), o bytes de paridad Reed/Solomon ATSC simulados y datos ATSC simulados. El reordenamiento de los datos VSB robustos reordenados normalmente resulta de la desintercalación del desintercalador (98) y a los datos reordenados puede hacerse referencia como datos VSB robustos reordenados.

Los bytes de paridad Reed/Solomon ATSC simulados (20 por paquete) de los paquetes VSB robustos y de los paquetes de datos ATSC simulados (207 bytes por paquete) se descargan en

(100). Los paquetes VSB robustos restantes, cada uno de los cuales incluye una cabecera de transporte y datos VSB robustos reordenados, son multiplexados por un segundo multiplexor (102) con paquetes de datos ATSC reales cada uno de los cuales contiene 187 bytes de una cabecera de transporte y datos ATSC. Cualquiera de las entradas al segundo multiplexor (102) puede seleccionarse sobre la base de paquete por paquete y se provee a un transmisor ATSC (104). La selección del segundo multiplexor (102) cuya entrada pasa al transmisor ATSC (104) está basada en un mapa VSB robusto que se describirá más adelante.

El transmisor ATSC (104) típicamente incluye un codificador Reed/Solomon (106), un intercalador (108) y un codificador interno de tasa 2/3 de doce vías (110) todo lo cual opera de conformidad con la norma ATSC. Del codificador Reed/Solomon (106) salen paquetes de cabeceras de transporte, datos VSB robustos reordenados y bytes de paridad Reed/Solomon ATSC multiplexados con paquetes de cabeceras de transporte, datos ATSC y bytes de paridad Reed/Solomon ATSC. Los bytes de paridad Reed/Solomon ATSC para los datos VSB robustos se calculan con base en los datos VSB robustos reordenados. Además, el intercalador (108) cambia el ordenamiento de los datos VSB robustos de manera que dichos

datos en la salida del intercalador (108) vuelvan a ser datos VSB robustos normalmente ordenados. También el intercalador (108) dispersa las cabeceras de transporte, los bytes de paridad Reed/Solomon ATSC y los datos ATSC. Estos datos son codificados a una tasa de $2/3$ por el codificador interno de tasa $2/3$ de doce vías (110) y se transmiten. Los datos VSB robustos transmitidos están en el orden normal, v.g., el orden provisto a la salida del intercalador de bloques pequeños (88). Este orden normal permite que el receptor VSB robusto evite la demora causada por el desintercalador (52) y por el intercalador (62) del receptor VSB robusto (14).

Tal como se indica en la Figura 8, un receptor de la norma ATSC (120) incluye un decodificador interno $2/3$ de doce vías que decodifica los datos transmitidos para proporcionar un flujo de datos de salida que comprenda datos robustos normalmente ordenados con cabeceras intercaladas de transporte, datos ATSC, y bytes de paridad Reed/Solomon ATSC ubicados de acuerdo con la intercalación convolucional de bytes ATSC provista por el intercalador (108). Un desintercalador ATSC (124) restituye las cabeceras de transporte, los datos ATSC y los bytes de paridad Reed/Solomon ATSC hacia sus posiciones "paquetizadas" de transporte. También el desintercalador ATSC (124) convierte

los datos VSB robustos ordenados normalmente en datos VSB robustos reordenados. Esta forma reordenada permite que un decodificador Reed/Solomon ATSC (126) del receptor ATSC estándar (120) lleve a cabo pruebas correctas de la paridad de los paquetes de datos VSB robustos. El receptor ATSC estándar (120) puede entonces leer las cabeceras de transporte de los paquetes de datos VSB robustos y fácilmente descartar los paquetes de datos VSB robustos en (128) con base en sus PIDs.

Tal como se indica en la Figura 9, un receptor VSB robusto (130) incluye un decodificador interno de tasa 2/3 de doce vías de salida blanda (132). (Un decodificador de 2/3 de salida dura originaría una pérdida considerable de la ganancia de codificación). La salida del decodificador interno de tasa 2/3 de doce vías de salida blanda (132) incluye datos VSB robustos ordenados de forma normal con datos ATSC reordenados, cabeceras de transporte y símbolos de paridad Reed/Solomon ATSC dispersados dentro de los datos VSB robustos en las ubicaciones indicadas por una línea de control de descarte (134) de la que se hablará más adelante. Un bloque de descarte (136), bajo el control de la línea de control de descarte (134), descarta los datos ATSC

reordenados, las cabeceras de transporte y los símbolos de paridad Reed/Solomon ATSC.

Un desintercalador de bloques pequeños (138) desintercala los datos VSB robustos. El desintercalador de bloques pequeños (138) tiene un tiempo de demora relativamente bajo. El desintercalador dispersa errores posibles de ráfaga en los datos VSB robustos a la salida del decodificador interno de tasa 2/3 con doce vías de salida blanda (132). Los datos VSB robustos ordenados de forma normal se decodifican en términos de bits por un decodificador externo (140) que también agrupa los datos VSB robustos en bytes. La información amplificada le indica al decodificador externo (140) qué tasa de codificación utilizar en los datos provistos al decodificador externo (140) en una entrada de Datos R_{MAP} . No se necesita ni el desintercalador (52) ni el intercalador (62) en el receptor VSB robusto (130) permitiendo menos demora en la retroalimentación general hacia el rastreador de fase y/o el ecualizador. Los datos decodificados externos pueden ser utilizados, por ejemplo, por un predictor mejorado de secciones (142) para generar retroalimentación al rastreador de fase y/o al ecualizador. Si se desea, la retroalimentación puede atravesar por una compuerta o se puede ajustar el algoritmo del gradiente del

ecualizador del tamaño del paso proporcionalmente a la confiabilidad de los datos decodificados.

La carga útil del paquete de datos VSB robusto decodificada por el decodificador externo (140) es desintercalada por un desintercalador (144) (que corresponde al inverso del intercalador (84)) y recibe una decodificación Reed/Solomon por un decodificador Reed/Solomon (146) (que corresponde al codificador Reed/Solomon (82)) para reconstruir los datos auxiliares no codificados originales proporcionados al codificador Reed/Solomon (82) de la Figura 7.

Tal como se indica en la norma ATSC, un marco comprende una diversidad de segmentos cada uno de los cuales contiene un número predeterminados de bytes. El primer segmento de una trama es un segmento sincronizado de la trama y los segmentos restantes en la trama son segmentos de datos. Aunque los datos VSB robustos pueden transmitirse en segmentos o en segmentos parciales, es conveniente transmitir dichos datos en pares de segmentos. El mapa VSB robusto discutido arriba indica cuáles pares de segmentos contienen datos VSB robustos para que el bloque de descarte (136) pueda descartar correctamente los datos ATSC reordenados antes de que éstos

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puedan llegar al decodificador externo (140). Las cabeceras de transporte y los datos de paridad Reed/Solomon ATSC para todos los todos los segmentos (VSB robustos y ATSC) también pueden descartarse por el bloque de descarte (136).

En la Figura 10 aparece un circuito conceptualmente simple para generar la señal de control adecuada en la línea de control de descarte (134) para controlar esta función de descarte, junto con la porción relevante del receptor VSB robusto (130). El receptor VSB robusto (130) utiliza la información del mapa recibida (el método para transmisión y recepción de esta información de mapa está descrito a continuación) para dar una orden a un generador de segmento simulado (150) de cuándo construir los segmentos de bytes simulados (207). El generador de segmentos simulados (150) también utiliza la señal sincronizada de la trama. Para cada segmento simulado ATSC, el generador de segmentos simulados (150) fija todos los bytes en FF. Para cada uno de los segmentos simulados de los datos VSB robustos, el generador de segmentos simulados (150) fija la cabecera de transporte y los bytes de paridad Reed/Solomon en FF. El generador de segmentos simulados (150) fija el resto de los bytes de cada segmento simulado de datos VSB robustos en 00.

Estos segmentos simulados son alimentados por el generador de segmentos simulados (150) a un intercalador de bytes convolucional (152) cuya salida es posteriormente utilizada para controlar el bloque de descarte (136) que posteriormente responde a los códigos FF y 00 para descartar correctamente los datos ATSC reordenados, las cabeceras de transporte y los datos de paridad Reed/Solomon ATSC que están intercalados dentro del flujo de datos recibidos. El bloque de descarte (136) entonces, pasa únicamente por los datos VSB robustos.

La Figura 11 muestra un transmisor VSB robusto con código de salida múltiple (160). El transmisor VSB robusto (160) opera de forma similar al transmisor VSB robusto (80) de la Figura 7. El transmisor VSB robusto (160) tiene el primer codificador Reed/Solomon (162) que codifica los primeros datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a los primeros datos auxiliares no codificados, un segundo codificador Reed/Solomon (164) que codifica los segundos datos auxiliares no codificados añadiendo bytes de paridad Reed/Solomon a los segundos datos auxiliares no codificados, y un tercer codificador Reed/Solomon (166) que codifica los terceros bytes de datos auxiliares no codificados añadiendo bytes de paridad

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Reed/Solomon a dichos terceros datos auxiliares no codificados. Los datos auxiliares no codificados, codificados de primeros como Reed/Solomon, son intercalados por un primer intercalador (168); los segundos datos auxiliares no codificados, codificados como Reed/Solomon, son intercalados por un segundo intercalador (170) y, los terceros datos auxiliares no codificados, codificados como Reed/Solomon, son intercalados por un tercer intercalador (172). Entonces, los primeros datos auxiliares no codificados, codificados como Reed/Solomon intercalados, se codifican en términos de bits por un primer codificador externo (174); los segundos datos auxiliares no codificados, codificados como Reed/Solomon intercalados, se codifican en términos de bits por un segundo codificador externo (176), y los terceros datos auxiliares no codificados, codificados como Reed/Solomon intercalados, se codifican en términos de bits por un tercer decodificador externo (178). La salida en términos de bits del primer codificador externo (174) es intercalada por un primer intercalador de bloques pequeños (180); la salida en términos de bits del segundo codificador externo (176) es intercalada por un segundo intercalador de bloques pequeños (182) y la salida en términos de bits del tercer decodificador externo

(178) es intercalada por un tercer intercalador de bloques pequeños (184).

El primer codificador externo (174) es un codificador con tasa de $1/4$, el segundo codificador externo (176) es un codificador con tasa de $1/2$ y el tercer decodificador externo (178) es un decodificador con tasa de $3/4$, aún cuando se puede utilizar cualquier otra combinación de estos u otros codificadores externos que utilicen diferentes tasas de códigos. Las salidas de datos del primero, segundo y tercer intercaladores de bloques pequeños (180, 182 y 184) es seleccionada por un multiplexor (186) bajo control de una entrada selecta que determina el orden en que los diferentes datos codificados externos se insertan a la trama para ser transmitidos. Los datos a la salida de multiplexor (186) pueden mencionarse como Rdata(n.o.), los cuales tal como ya se dijo, corresponden a datos VSB robustos normalmente ordenados.

Las tres entradas superiores de un multiplexor (190) reciben paquetes de formato ATSC, cada uno de los cuales tiene una cabecera de transporte de tres bytes con un número de PID para datos VSB robustos (184), bytes con sitio para sostener datos VSB robustos simulados y veinte bytes

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simulados con sitio para sostener datos de paridad Reed/Solomon ATSC. Los datos VSB robustos en la entrada de más arriba del multiplexor (190) corresponden a datos codificados con tasa de $1/4$ del primer codificador externo (174); los datos VSB robustos en la siguiente entrada del multiplexor (190) corresponden a datos codificados con tasa de $1/2$ del segundo codificador externo (176) y los datos VSB robustos en la siguiente entrada del multiplexor (190) corresponden a datos codificados a una tasa de $1/3$ del tercer codificador externo (178). Los datos suministrados por la entrada más baja del multiplexor (190) comprenden paquetes simulados del formato ATSC, cada uno de los cuales tiene 207 bytes de datos ATSC simulados. Estos paquetes de datos ATSC simulados sirven como sostenedores para los paquetes de datos ATSC reales que deben adicionarse corriente abajo del multiplexor (190). Las entradas al multiplexor (190) se pueden seleccionar sobre una base de paquete por paquete de acuerdo con la entrada sobre la línea de selección. Esta selección está basada en el mapa de datos VSB robusto que se describe más adelante.

La salida del multiplexor (190) es intercalada por un intercalador (192) para lograr una intercalación convolucional ATSC correcta. Un reemplazador de datos (194)

recibe tanto la salida del intercalador (192) como la salida del multiplexor (186). El reemplazador de datos (194) reemplaza cada byte con lugar para tener datos VSB robustos simulados desde el multiplexor (190) con los siguientes bytes de datos VSB robustos correspondientes ordenados normalmente que provienen del multiplexor (186).

La salida del reemplazador de datos (194) contiene datos VSB robustos normalmente ordenados (codificados a tasas de 1/4, 1/2 y/o 3/4 según sea apropiado) con cabeceras de transporte intercaladas, bytes de paridad Reed/Solomon ATSC simulados, y bytes de paquetes de datos ATSC simulados. Un desintercalador de bytes convolucional (196) (en la forma descrita en la Norma ATSC) desintercala la salida del reemplazador de datos (194) para así "repaquetizar" eficazmente los datos como paquetes de cabeceras de transporte, datos VSB robustos reordenados (codificados a tasas de 1/4, 1/2 o 3/4), bytes de paridad Reed/Solomon ATSC simulados y paquetes simulados de datos ATSC. El reordenamiento de los datos VSB robustos ordenados normalmente resulta de la desintercalación del desintercalador (196).

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Los bytes de paridad Reed/Solomon ATSC simulados (20 por paquete) y los paquetes de datos ATSC simulados (207 bytes por paquete) se descartan en el (198) en una forma similar a aquella provista por la línea de control de descarte (134) y el bloque de descarte (136) de la Figura 9. Los paquetes VSB robustos restantes, cada uno de los cuales incluye una cabecera de transporte y datos VSB robustos reordenados, son multiplexados por un multiplexor (200) con paquetes de datos ATSC reales, cada uno de los cuales contiene 187 bytes de cabecera de transporte y datos ATSC. Cualquier entrada al multiplexor (200) puede seleccionarse sobre una base de paquete por paquete y se suministra a un transmisor ATSC (202). La selección del multiplexor (200) cuya entrada pasará al transmisor ATSC (202) está basada en el mapa VSB robusto que se describirá más adelante.

El transmisor ATSC (202) típicamente incluye un codificador Reed/Solomon (204), un intercalador (206) y un codificador interno con tasa de 2/3 de doce vías (208) todo lo cual opera de conformidad con la norma ATSC. El codificador Reed/Solomon (204) saca los paquetes de cabeceras de transporte, los datos VSB robustos reordenados y los bytes de paridad Reed/Solomon ATSC multiflexados con paquetes de cabeceras de transporte, datos ATSC, y bytes de paridad

Reed/Solomon ATSC. Los bytes de paridad Reed/Solomon ATSC para los datos VSB robustos se calculan con base en los datos VSB robustos reordenados. Además, el intercalador (206) cambia el ordenamiento de los datos VSB robustos de manera que dichos datos a la salida del intercalador (206) nuevamente sean datos VSB robustos ordenados de forma normal. También el intercalador (206) dispersa los bytes de la cabecera de transporte, los bytes de paridad Reed/Solomon ATSC y los datos ATSC. Estos datos son codificados a $2/3$ a una tasa de $2/3$ por un codificador interno de tasa de $2/3$ con doce vías (208) y son transmitidos. Los datos VSB robustos transmitidos se encuentran en orden normal, v.g., el orden provisto a la salida del multiplexor (186). Este orden normal de datos permite al receptor VSB robusto evadir la demora causada por el desintercalador (52) y por el intercalador (62).

Tal como se discutió arriba, una trama ATSC comprende un segmento sincronizado de trama y una diversidad de segmentos y para conveniencia, los datos VSB robustos se empacan en grupos de cuatro segmentos. Más específicamente, la Figura 12 muestra un ejemplo de cuatro segmentos de datos que se puede utilizar en una trama para transmitir datos VSB robustos que están codificados a una tasa de $1/2$, la Figura 13 muestra un

ejemplo de cuatro segmentos de datos que pueden utilizarse en una trama para transmitir datos VSB robustos que están codificados a una tasa de $1/4$ y la Figura 14 muestra un ejemplo de cuatro segmentos de datos que pueden utilizarse en una trama para transmitir datos VSB robustos que están codificados a una tasa de $3/4$. Estos ejemplos representan la trama antes del intercalador (108) y asumen que cada grupo de cuatro segmentos de datos VSB robustos contiene un número integral de bloques codificados Reed/Solomon robustos cada uno de los cuales tiene 184 bytes de largo, de los cuales veinte bytes son bytes de paridad.

Para el caso de un código externo con tasa de $1/2$, la Figura 12 muestra que el codificador externo saca dos bits por cada bit de entrada. Un paquete de datos VSB robusto se empaca como un bloque Reed/Solomon RVSB hacia un par de segmentos de datos (un bit por símbolo) de manera que, para un código de salida con tasa de $1/2$, cuatro segmentos contengan dos bloques codificados Reed/Solomon robustos. Como se indica en la Figura 13, para el caso de códigos externos con tasa de $1/4$, el codificador externo saca cuatro bits por cada bit de entrada. Los datos VSB robustos se empacan como un bloque Reed/Solomon RVSB por cada cuatro segmentos de datos ($1/2$ bit por símbolo) de manera que, para un código

externo con tasa de $1/4$, cuatro segmentos contengan un bloque codificado Reed/Solomon robusto. Tal como se indica en la Figura 14, para el caso del código externo de tasa de $3/4$ el codificador externo saca cuatro bits por cada tres bits de entrada. En este caso, las fronteras de los bytes y símbolos transmitidos no siempre concuerdan. Sin embargo, tres bloques completos Reed/Solomon RVSB conformarán un paquete exacto de cuatro segmentos de datos (1.5 bits por símbolo) de manera que, para un código externo con tasa de $3/4$, cuatro segmentos contengan tres bloques codificados Reed/Solomon robustos.

De acuerdo con lo anterior, las Figuras 12, 13 y 14 pueden representarse por la siguiente tabla:

S	X	Y
$1/2$	1	2
$1/4$	1	4
$3/4$	3	4

donde X representa el número de bloques codificados Reed/Solomon robustos completos y Y representa el número de segmentos de trama requeridos para contener el número X correspondiente de bloques codificados Reed/Solomon robustos.

Sin embargo, debe entenderse que pueden utilizarse otras tasas de codificación en relación con el presente invento y,

por consiguiente, la tabla anterior variará dependiendo de las tasas particulares de codificación que se utilicen.

Los intercaladores (18), (84), (168), (170) y (172) se indican con más detalle en la Figura 15 y los desintercaladores (58) y (144) también se muestran con más detalle en la Figura 16, asumiendo que el bloque codificado Reed/Solomon robusto se elige para que tenga 184 bytes de largo. Los intercaladores (18), (84), (168), (170) y (172) son intercaladores convolucionales $B = 46$, $M = 4$, $N = 184$ que intercalan los datos VSB robustos en términos de bytes. Este esquema de intercalación es el mismo esquema de intercalación ATSC descrito en la Norma A/53 de Televisión Digital ATSC y en la Guía para Utilizar la Norma A/54 de Televisión Digital ATSC, salvo que el parámetro B para el intercalador robusto es (46) en lugar de (52) y el parámetro N es (184) en lugar de (208). Este intercalador se requiere para que el receptor VSB robusto pueda manejar las largas ráfagas de ruido en el canal aún cuando no se pase por el desintercalador (D_s) ATSC, como se indica en la Figura 9.

Tal como se ilustra en la Figura 16, los desintercaladores (58) y (144) son desintercaladores convolucionales $B = 46$, $M = 4$, $N = 184$ que desintercalan los

datos VSB robustos en términos de bytes. Este esquema de desintercalación también es igual al esquema de desintercalación ATSC descrito en la Norma A/53 de Televisión Digital ATSC y en la Guía para la Utilización de la Norma A/54 de Televisión Digital ATSC, salvo que el parámetro B para el desintercalador robusto es (46) en lugar (52) y el parámetro N es (184) en lugar de (208).

Teniendo en cuenta que el bloque Reed/Solomon VSB robusto comprende 184 bytes y que un número integral de bloques Reed/Solomon VSB robustos se encuentra en una trama de datos, el número de bytes de datos VSB robustos más el número de bytes de paridad Reed/Solomon VSB robustos en una trama de datos es siempre divisible por 46. Entonces, el segmento sincronizado de trama puede utilizarse como un sincronizador para los desintercaladores (58) y (144) (D_r) en el receptor, independientemente del valor de G (que se describe más adelante). En la sincronización de la trama los conmutadores del desintercalador están forzados a las posiciones más altas. Los desintercaladores (58) y (144) son desintercaladores en términos de bytes.

Mapeo de Datos

Tal como se indicó arriba, cada trama de datos puede contener una mezcla de segmentos de datos VSB robustos y de segmentos de datos ATSC (no codificados robustamente). Además, los datos VSB robustos pueden contener datos codificados con una mezcla de tasas de codificación. El receptor VSB robusto (14) o (130) debe tener un mapa VSB robusto que indica cuáles segmentos son codificados VSB robustos y cuáles códigos externos se utilizan para la codificación VSB robusta de manera que el receptor VSB robusto (14) o (130) puedan correctamente procesar los datos VSB robustos y descartar los datos ATSC. Los transmisores VSB robustos (10), (80) y (160) también utilizan el mapa VSB robusto para controlar su correspondiente multiplexión y descartar funciones. Este mapa VSB robusto se transmite por un transmisor VSB robusto (10), (80) o (160) al receptor VSB robusto (14) o (130) junto con todos los demás datos en la forma descrita a continuación.

La presencia, número y ubicación de los datos VSB robustos en una trama de datos codificada con un código externo particular se indica por uno o más números S_c que aparecen como datos de dos niveles en el segmento

sincronizado de trama de la trama de datos. Como ya se sabe, el segmento sincronizado de trama es el primer segmento en una trama. Entonces, para los códigos externos descritos arriba (con tasas de $1/4$, $1/2$ y $3/4$), el segmento sincronizado de trama preferiblemente debe contener $[S_{1/4}, S_{1/2}, \text{ y } S_{3/4}]$. Cada S_c (tal como $S_{1/4}$, $S_{1/2}$, y $S_{3/4}$) se codifica como diez y ocho símbolos (bits) de dos niveles de datos. Para todos los tres códigos, un total de $3 \times 18 = 54$ símbolos se requieren como una definición del mapa VSB robusto. Estos símbolos se insertan al área reservada cerca de la terminación de cada segmento sincronizado de trama (justo antes de los doce bits de precodificación). Para cada grupo de diez y ocho bits ($b_{18} \dots b_1$), los últimos seis bits ($b_6 \dots b_1$) representan el número G de grupos de ocho segmentos (8 segmentos = 2, 4 o 6 paquetes de datos VSB robustos dependiendo del código de salida) mapeados como datos VSB robustos en la trama actual. Los doce bits precedentes son para compensación de filtros combinada (ver la Guía para la Utilización de la Norma A/54 de Televisión Digital ATSC). De acuerdo con lo anterior, tal como se indica en la Figura 18, los bits $b_6 \dots b_1$, representan el número G , los bits $b_{18} \dots b_{13}$ son el complemento de los bits $b_6 \dots b_1$ y los bits $b_{12} \dots b_7$ pueden alternarse +1 y -1 (o en cualquier otro patrón).

Asumamos que $S = S_{1/4} + S_{1/2} + S_{3/4}$. Como $312/8 = 39$, 0-39 se pueden mapear grupos de ocho segmentos como datos VSB robustos o como 8 datos VSB (datos ATSC). Por consiguiente, cada S_c puede tener un valor de 0...39, siempre que la suma S de los mismos sea ≤ 39 .

Los segmentos de datos VSB robustos preferiblemente se distribuyen en la forma más uniforme posible a lo largo de la trama de datos. Por ejemplo, si $S = 1$, entonces los siguientes ocho segmentos se mapean como segmentos de datos VSB robustos y todos los otros segmentos se mapean como segmentos de datos ATSC: (1), (40), (79), (118), (157), (196), (235) y (274). Si $S = 2$, entonces los siguientes diez y seis segmentos se mapean como segmentos de datos VSB robustos y todos los demás segmentos se mapean como segmentos de datos ATSC: (1), (20), (39), (58), (77), (96), (115), (134), (153), (172), (191), (210), (229), (248), (267) y (286). Estos ejemplos continúan hasta cuando $S = 39$, en donde toda la trama de datos se mapea como segmentos de datos VSB robustos. Para algunos valores de S , el espacio entre pares de segmentos de datos VSB robustos no es perfectamente uniforme. Sin embargo, para cualquier valor de S , el espacio

se determina de forma anticipada y por consiguiente, es conocido para todos los receptores.

Si una trama contiene datos VSB robustos proporcionados por tres codificadores externos que operan a tasas de $1/4$, $1/2$ y $3/4$, entonces los datos de estos tres codificadores externos se pueden dividir en una trama de manera que en cuanto se refiere a los segmentos RVBS, los primeros segmentos $8 \times S_{1/4}$ contengan los datos codificados externos con tasa de $1/4$, los siguientes segmentos $8 \times S_{1/2}$ contengan datos codificados externos con tasa de $1/2$ y los últimos segmentos $8 \times S_{3/4}$ contengan datos codificados externos con tasa de $3/4$. Sin embargo, son posibles otras organizaciones de segmentos de datos VSB robustos para estos tres codificadores externos o para cualquier número de otro tipo de codificadores externos.

Considerando que este mapa VSB robusto está contenido en el segmento sincronizado de trama, tal como se discutió arriba, el mapa VSB robusto no disfruta del mismo nivel de ganancia de codificación que los datos VSB robustos. No obstante, el mapa VSB robusto puede todavía adquirirse en forma confiable por un receptor VSB robusto mediante la correlación del mapa VSB robusto sobre algún número de

tramas. Por consiguiente, el mapa VSB robusto no debe cambiar muy a menudo (por ejemplo, no más a menudo de cada ~60 tramas).

El método de mapeo arriba indicado le permite a un receptor adquirir confiable y simplemente el mapa VSB robusto por correlación. Una vez que un receptor ha adquirido el mapa, es deseable que instantáneamente rastree los cambios en el mismo de forma confiable. Para rastrear dichos cambios en el mapa de forma instantánea y confiable, la definición del mapa VSB robusto para cada código externo, excluyendo los bits combinados de compensación, se duplica en el primer bloque codificado Reed/Solomon VSB robusto de la trama. Además, existen datos que indican (i) cuándo en el futuro el mapa cambiará y (ii) la definición futura del nuevo mapa. El primer paquete de datos VSB robustos de una trama para un codificador externo, por consiguiente, tiene la estructura indicada en la Figura 17, en donde la definición de datos del mapa VSB robusto está dada por lo siguiente: ocho bits que designan en mapa actual (únicamente seis de estos bits se utilizan); ocho bits que designan el número de tramas hasta que cambia el mapa (1-125; si es 0, entonces no se esperan cambios); y, ocho bits que designan el siguiente mapa (nuevamente, solo seis de estos bits se utilizan). La porción

restante del primer paquete de datos VSB robustos corresponde a datos. El primer segmento RVSB en una trama para un codificador externo respectivo tiene el arreglo que se ilustra en la Figura 17.

De esta forma, un receptor puede rastrear cambios en el mapa utilizando datos VSB robustos confiables. Aún cuando un error de ráfaga destruya un número de tramas, el receptor puede mantener su propio conteo descendiente de las tramas utilizando el número de tramas que se hayan leído a partir de una trama recibida previamente. Si el receptor en cualquier momento encuentra que una definición para un código externo previamente adquirido por la correlación sincronizada de la trama no concuerda con la definición para dicho código externo en el primer segmento de datos VSB robustos, el receptor debe reiniciar su proceso de adquisición del mapa.

Predicción Mejorada de Secciones RVSB y Retroalimentación del Ecualizador

Los receptores VSB ATSC 8 hacen uso importante de la ecualización adaptiva y del rastreo de fase en la forma explicada en la Norma A/53 de Televisión Digital ATSC publicada por el Comité de Sistemas Avanzados de Televisión, en la Guía para la Utilización de la Norma A/54 de Televisión

Digital ATSC, también publicada por el Comité de Sistemas de Televisión Avanzada. El RVSB tal como se describió arriba tiene características que permiten mejoras en la ecualización adaptiva y en el rastreo de la fase.

El mejoramiento resulta de la retroalimentación de estimados confiables demorados del nivel de símbolos de entrada al ecualizador adaptivo y/o rastreador de fase con base en una estimación de secuencias a partir de un Algoritmo Viterbi mejorado. (Ver "El Algoritmo Viterbi", G. D. Forney, Jr., Proc. IEEE, vol 61, pp. 268-278, marzo de 1973). Este tipo de retroalimentación evita la necesidad de "recodificación", que tiene un problema de inicialización de estado.

La Patente Norteamericana No. 5.923.711 titulada "Predictor de Secciones para un Receptor de Señal" revela un receptor VSB 8 ATSC que utiliza un predictor de secciones con el fin de proporcionar retroalimentación más confiable al rastreador de fase o al ecualizador adaptivo. Esta retroalimentación puede ser aún más confiable con el sistema de predicción de secciones mejorado (300) que se muestra en la Figura 19. El sistema de predicción de secciones mejorado (300) tiene un decodificador interno (302) y un decodificador

externo (304) que operan de forma similar a los decodificadores internos y a los decodificadores externos arriba descritos.

La salida de predicción de secciones del decodificador interno (302) trabaja en una forma similar a aquella descrita en la Patente Norteamericana 5.923.711 arriba mencionada. Tal como se explicó anteriormente, el decodificador interno (302) se basa en cuadrículas cuaternarias (4-ary) de 8 estados que incluyen un precodificador. Con base en la mejor métrica de trayectoria al tiempo actual t , el predictor de secciones del decodificador interno (302) decide el estado más probable en el tiempo t . Entonces, con base en el siguiente par posible de estados, se seleccionan cuatro niveles de entrada predicha posible (entre ocho) para el siguiente símbolo en el tiempo $t + 1$. Por ejemplo, como se indica en las cuadrículas del decodificador interno en la Figura 20, si el estado más probable en el tiempo t es el estado uno, el siguiente estado será $\varepsilon[1 \ 5 \ 2 \ 6]$. Por consiguiente, el siguiente nivel de entrada en el tiempo $t + 1$ puede ser -7 , $+1$, -3 o $+5$. Estos niveles de entrada siguientes corresponden a pares de bits decodificados (00), (10), (01) y (11), respectivamente.

De forma similar, el decodificador externo (304) también encuentra la mejor métrica de trayectoria para el tiempo actual t para las respectivas cuadrículas. Una porción de esta cuadrícula se muestra en la Figura 21 para un decodificador externo ejemplar y se puede aplicar generalmente a todos los tres códigos de salida. Tal como se indica en la Figura 21, se seleccionan dos posibles pares de bits de entrada del decodificador externo para el tiempo $t + 1$ con base en el siguiente par posible de estados. A manera de ejemplo, los dos posibles pares de bits de entrada al decodificador externo pueden ser (10) o (01). El par de bits escogido por el decodificador externo (304) se envía a un mejorador de predicción (306) que selecciona niveles de amplitud +5 o -3 del el grupo de cuatro niveles previamente seleccionado por el predictor de secciones del decodificador interno (302) como la predicción de secciones mejorada para el tiempo $t + 1$. Considerando que la predicción de secciones del decodificador interno (302) tiene una demora cercana a cero, pero como el decodificador externo (304) solo puede operar sobre el mismo símbolo hasta después de que el decodificador interno (302) haya provisto una salida blanda decodificada, un módulo de demora (308) proporciona un tiempo de mora levemente mayor que el tiempo de demora del rastreo

del decodificador interno (302). La predicción de secciones proporcionada por el mejorador de predicción (306) se puede proporcionar como retroalimentación a un ecualizador de rastreo de fase (310).

Con algún tiempo de demora adicional, el decodificador externo (304) puede tomar una decisión dura final y seleccionar un único par de bits de entrada más posible para el tiempo $t + 1$. Por ejemplo, si se encuentra que 11 es el par de bits de entrada más probable para el decodificador externo (304) según lo determinado por su Algoritmo Viterbi, esta información es enviada por el decodificador externo (304) al mejorador de predicción (306) que entonces elige +5 de un conjunto de cuatro niveles y pares de bits correspondientes ya seleccionados por el predictor de secciones del decodificador interno (302). El código externo puede ser un código convolucional u otro tipo de código de corrección de error. El mejorador de predicción (306) es inhabilitado durante los períodos de tiempo cuando los datos ATSC están siendo recibidos.

Una retroalimentación del sistema mejorado de predicción de secciones (320) del estimador de secuencias posibles máximas (MLSE) utiliza un algoritmo Viterbi tal como se

muestra en la Figura 22 junto con otras partes relevantes de un receptor RVSB. La retroalimentación del sistema mejorado de predicción de secciones MLSE (320) tiene un decodificador interno (322) y un decodificador externo (324) que opera de forma similar al decodificador interno (302) y al decodificador externo (304) arriba descritos. Sin embargo, en lugar de utilizar la salida de predicción de secciones del decodificador interno (302), se configura un módulo MLSE mejorado (326) para ejecutar el Algoritmo Viterbi usual sobre la señal recibida mediante la operación de cuadrículas de código con tasa de $2/3$ de ocho estados (las mismas cuadrículas utilizadas por el decodificador interno (322), incluyendo el precodificador).

El módulo MLSE mejorado (326) selecciona su siguiente entrada, bien sea (i) la señal recibida de nivel ocho ruidoso demorada por un módulo de demora (328) si la siguiente entrada es un símbolo no RVSB, o (ii) la salida de decisión de pares de bits del decodificador externo (324) (duro y blando) si la siguiente entrada es un símbolo RVSB. El módulo MLSE mejorado (326) realiza esta selección de acuerdo con la información de símbolo por símbolo en el mapa RVSB.

El módulo MLSE mejorado (326) saca uno de ocho símbolos posibles como su predicción de secciones, y esta predicción de secciones (decisión de símbolo) es provista por el módulo MLSE mejorado (326) como retroalimentación a un ecualizador o a un rastreador de fase (330).

El módulo MLSE mejorado (326) debería seguir una trayectoria más correcta a través de la cuadrícula de ocho estados que la que sigue el codificador interno (322) porque el módulo MLSE mejorado (326) obtiene entradas más confiables del decodificador externo (324) cuando un símbolo RVSB está disponible.

La salida del módulo MLSE mejorado (326) puede ser una decisión de sección dura o de nivel blando. También, cualquier indicación de confiabilidad del símbolo del decodificador interno (322) o del decodificador externo (324) se puede utilizar para cambiar el tamaño del paso del algoritmo LMS del ecualizador. (Ver la Guía para la Utilización de la Norma A/54 para Televisión Digital ATSC).

Una secuencia opcional de instrucción codificado predeterminado puede incluirse en una porción especificada del primer segmento RVSB de un campo de datos. Esta secuencia es conocida por adelantado tanto por el transmisor como por

el receptor. Durante el tiempo en que la secuencia de instrucción decodificada sale del decodificador externo (324), la entrada al módulo MLSE mejorado (326) se conmuta a una versión almacenado de la secuencia de instrucción decodificada.

Algunas modificaciones del presente invento han sido discutidas arriba. Otras modificaciones se les ocurrirán a aquellos que practiquen la técnica del presente invento. Por ejemplo, aunque el receptor estándar ATSC (12) y el receptor VSB robusto (14) se muestra arriba como receptores separados, las funciones del receptor estándar ATSC (12) y del receptor VSB robusto (14) pueden combinarse en dos trayectorias de datos de un mismo receptor capaz de decodificar ambos tipos de datos (datos ATSC y datos VSB robustos).

De conformidad con lo anterior, la descripción del presente invento debe interpretarse únicamente de forma ilustrativa solamente y con el propósito de enseñar a aquellos que conocen la técnica la mejor manera de implementar el invento. Los detalles pueden variar sustancialmente sin apartarse del espíritu del invento y se reserva el uso exclusivo de todas las modificaciones que estén dentro del alcance de las reivindicaciones anexas.

RETROALIMENTACIÓN DE LA PREDICCIÓN MEJORADA DE SECCIONES

Expediente 7174D

REIVINDICACIONES

1. Un método para proporcionar predicción mejorada de secciones, el cual se CARACTERIZA por los siguientes pasos:

recibir una entrada que contiene los primeros y los segundos datos, en donde los primeros y los segundos datos tienen la misma constelación de nivel n y diferentes tasas de bits;

decodificar únicamente los segundos datos con con decodificador;

producir una salida en respuesta a la entrada y al decodificador, en donde la salida se confina a por lo menos uno pero menos de $n/2$ de los niveles de constelación n , y en donde $n > 2$; y

proporcionar la salida como la predicción mejorada de secciones.

2. El método de la reivindicación 1 en donde el decodificador es un primer decodificador, y en donde el paso de recepción incluye el paso de decodificar la entrada con un

segundo decodificador para recuperar los primeros y los segundos datos, en donde el segundo decodificador tiene n estados, y el paso de producción incluye el paso de elegir $n/4$ estados de $n/2$ estados de los n estados del segundo decodificador y en donde el paso de suministro comprende el paso de proporcionar los estados $n/4$ como la predicción mejorada de secciones.

3. El método de la reivindicación 2 que comprende además el paso de demorar el paso de elección con base en un tiempo de procesamiento del segundo decodificador.

4. El método de la reivindicación 1 en donde el decodificador es un primer decodificador y en donde el paso receptor comprende el paso de decodificar la entrada con segundo decodificador para recuperar los primeros y los segundos datos y en donde el segundo decodificador tiene estados n y el paso de producción incluye el paso de elegir únicamente un estado entre los estados $n/2$ de los estados n del segundo decodificador y en donde el paso de suministro comprende el paso de proporcionar un estado como una predicción mejorada de secciones.

5. El método de la reivindicación 4 que comprende además el paso de demorar el paso de elección con base en un tiempo de procesamiento del segundo decodificador.

6. El método de las reivindicaciones 1, 2, 3, 4 o 5 en el que n es ocho.

7. El método de la reivindicación 1 en donde el paso de producción comprende los siguientes pasos:

decodificar la entrada cuando los segundos datos no están disponibles para así producir la salida; y,

decodificar los segundos datos cuando estos están disponibles para producir la salida.

8. El método de la reivindicación 7 que comprende además el paso de demorar la decodificación de la entrada con base al menos en parte en un tiempo de procesamiento del decodificador.

9. El método de la reivindicación 7 en donde el paso de suministro comprende el suministrar únicamente un estado como la predicción mejorada de secciones.

10. El método de la reivindicación 7 que comprende además el paso de seleccionar entre decodificar la entrada y los segundos datos en respuesta a un mapa recibido.

11. El método de la reivindicación 1 en donde el decodificador es un primer decodificador, en el que el paso de recepción comprende el paso de decodificar la entrada con un segundo decodificador para recuperar los primeros y los segundos datos y en donde el paso de decodificar únicamente los segundos datos incluye el paso de decodificar los segundos datos con el primer decodificador para producir dichos segundos datos decodificados y en donde el paso de producción comprende los siguientes pasos:

producir la salida mediante la decodificación de la entrada con un tercer decodificador cuando los segundos datos decodificados no estén disponibles; y

producir la salida mediante la decodificación de los segundos datos decodificados con un tercer decodificador cuando los segundos datos decodificados están disponibles.

12. El método de la reivindicación 11 que comprende además el paso de demorar el paso de decodificar la entrada con el tercer decodificador.

13. El método de la reivindicación 11 en donde el tercer decodificador implementa un algoritmo Viterbi.

14. El método de la reivindicación 11 en donde el paso de suministro comprende el paso de proporcionar únicamente un estado del tercer decodificador como la predicción mejorada de secciones.

15. El método de la reivindicación 11 que comprende además el paso de seleccionar entre decodificar la entrada y los segundos datos decodificados en respuesta a un mapa recibido.

16. El método de las reivindicaciones 7 u 11 en donde los primeros datos comprenden símbolos no-RVSB de ocho niveles y en donde los segundos datos incluyen símbolos de RVSB de ocho niveles.

17. El método de las reivindicaciones 1, 7 u 11 en donde el paso de suministro incluye el paso de suministrar la predicción mejorada de secciones con base en una señal de instrucción conocida cuando una señal de instrucción transmitida está contenida en una señal recibida.

18. El método de la reivindicación 1 comprende además el paso de suministrar la predicción mejorada de secciones como retroalimentación a un ecualizador.

19. El método de la reivindicación 1 que comprende además el paso de suministrar la predicción mejorada de secciones como retroalimentación a un rastreador de fase.

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(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 October 2001 (25.10.2001)

PCT

(10) International Publication Number
WO 01/78495 A2

- (51) International Patent Classification: Not classified
- (21) International Application Number: PCT/US01/09734
- (22) International Filing Date: 27 March 2001 (27.03.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
- | | | |
|------------|-------------------------------|----|
| 60/198,014 | 18 April 2000 (18.04.2000) | US |
| 60/255,476 | 13 December 2000 (13.12.2000) | US |
| 60/255,464 | 13 December 2000 (13.12.2000) | US |
| 09/804,237 | 13 March 2001 (13.03.2001) | US |
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- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
- Published:**
— without international search report and to be republished upon receipt of that report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

WO 01/78495 A2

(54) Title: ENHANCED SLICE PREDICTION FEEDBACK

(57) Abstract: Enhanced slice prediction is based upon ATSC 8 VSB data when robust 8 VSB data are not available and is based upon robust 8 VSB data when robust 8 VSB data are available.

3 LS

ENHANCED SLICE PREDICTION FEEDBACK**Related Applications**

This application claims the benefit of
U.S. Provisional Application No. 60/198,014, filed
5 April 18, 2000, U.S. Provisional Application No.
60/255,476, filed December 13, 2000, and U.S.
Provisional Application No. 60/255,464, filed
December 13, 2000.

Technical Field of the Invention

10 The present invention relates to the
transmission and/or reception of digital data.

Background of the Invention

The standard in the United States for the
transmission of digital television signals is known
15 as 8 VSB data (ATSC Digital Television Standard
A/53). This 8 VSB data has a constellation
consisting of eight possible symbol levels. In a
VSB system, the eight possible symbol levels are all
in the same phase. In a QAM system, however, the
20 symbols are transmitted in phase quadrature
relationship.

The standard referred to above specifies the formatting and modulation of digital video and audio data. The transmitted data is in the form of symbols with each symbol representing two bits of data that are trellis encoded into three bits of trellis encoded data. Each three bits of trellis encoded data are mapped into a symbol having a corresponding one of eight levels. Reed/Solomon encoding and interleaving are also provided to increase the robustness of the transmitted information.

Auxiliary data (data other than digital video or audio data) are also permitted to be transmitted in a digital television channel. These data are formatted and modulated according to the standard in the same manner as video and audio data. Receivers made in accordance with the 8 VSB standard are able to read packet identifications (PIDs) which allow the receivers to differentiate between audio, video, and auxiliary data.

However, while the robustness of the transmitted digital television signals is sufficient for digital television reception, this robustness

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may not be sufficient for the transmission of auxiliary data, particularly where the auxiliary data are critical. Accordingly, one of the applications of the present invention is the transmission of auxiliary data in a VSB format with outer encoding for added robustness. The auxiliary data transmitted in accordance with the application of the present invention are referred to herein as robust VSB data (RVSB).

Summary of the Invention

In one aspect of the present invention, a method for providing enhanced slice prediction comprises the following: receiving an input containing first and second data, wherein the first and second data have different bit rates and are defined by the same n level constellation; decoding only the second data with a decoder; producing an output in response to the input and the decoder, wherein the output is confined to at least one but fewer than $n/2$ of the n constellation levels, and wherein $n > 2$; and, providing the output as the enhanced slice prediction.

In another aspect of the present invention, an apparatus for providing enhanced slice prediction comprises an inner decoder, an outer decoder, and an enhanced slice predictor. The inner decoder inner decodes a received signal to provide an inner decoded output. The inner decoder produces $n/2$ possible decoding states based upon the received signal, and the received signal contains data having n levels, wherein $n > 2$. The outer decoder outer decodes the inner decoded output. The enhanced slice predictor chooses at least one but fewer than the $n/2$ of the $n/2$ possible decoding states based upon an output of the outer decoder and provides the chosen state or states as the enhanced slice prediction.

In yet another aspect of the present invention, an apparatus for providing enhanced slice prediction comprises an inner decoder, an outer decoder, and an enhanced slice predictor. The inner decoder inner decodes a received signal containing first and second data to provide inner decoded first and second data. The outer decoder outer decodes only the second data. The enhanced slice predictor

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provides a prediction output based upon the first data when the second data is not available and based upon the outer decoded second data when the second data is available.

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Brief Description of the Drawing

These and other features and advantages will become more apparent from a detailed consideration of the invention when taken in conjunction with the drawing in which:

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Figure 1 shows a robust VSB transmitter for transmitting robust VSB data and ATSC data in accordance with the present invention;

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Figure 2 shows a standard ATSC receiver for receiving the ATSC data transmitted by the robust VSB transmitter of Figure 1;

Figure 3 shows a robust VSB receiver for receiving the robust VSB data transmitted by the robust VSB transmitter of Figure 1;

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Figure 4 shows the 2/3 rate encoder of Figure 1 in additional detail;

Figure 5 shows the mapping function performed by the mapper of Figure 4;

Figure 6 shows the operation of the 2/3 rate decoders of Figures 2 and 3;

Figure 7 shows another robust VSB transmitter for transmitting robust VSB data and ATSC data in accordance with the present invention;

Figure 8 shows a standard ATSC receiver for receiving the ATSC data transmitted by the robust VSB transmitter of Figure 7;

Figure 9 shows a robust VSB receiver for receiving the robust VSB data transmitted by the robust VSB transmitter of Figure 7;

Figure 10 shows a circuit for generating the appropriate control signal on the discard control line of Figure 9;

Figure 11 shows yet another robust VSB transmitter for transmitting robust VSB data and ATSC data in accordance with the present invention;

Figure 12 shows an example of four data segments containing 1/2 rate outer coded data that may be transmitted by a robust VSB transmitter according to the present invention;

Figure 13 shows an example of four data segments containing 1/4 rate outer coded data that

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may be transmitted by a robust VSB transmitter according to the present invention;

Figure 14 shows an example of four data segments containing 3/4 rate outer coded data that may be transmitted by a robust VSB transmitter according to the present invention;

Figure 15 shows the interleavers (I_r) of Figures 1, 9, and 11 in more detail;

Figure 16 shows the deinterleavers (D_r) of Figures 3 and 9 in more detail;

Figure 17 shows a map definition structure of a first robust VSB data packet of a frame;

Figure 18 shows a portion of the frame sync segment of a frame that carries a map indicating where in the frame robust VSB data can be found;

Figure 19 illustrates an enhanced slice predictor according to one embodiment of the present invention;

Figure 20 shows the trellis for the inner decoder of Figure 19;

Figure 21 shows possible state transitions for the outer decoder of Figure 19; and,

Figure 22 illustrates an enhanced slice predictor according to another embodiment of the present invention.

Detailed Description

5 RVSB and ATSC Data Transmission and Reception

Figure 1 shows a robust VSB transmitter 10 that transmits both ATSC data and robust VSB data in accordance with one embodiment of the present invention. Figure 2 shows a standard ATSC receiver 10
10 12 that receives the ATSC data transmitted by the robust VSB transmitter 10, and Figure 3 shows a robust VSB receiver 14 that receives the robust VSB data transmitted by the robust VSB transmitter 10.

The robust VSB transmitter 10 includes a
15 Reed/Solomon encoder 16 that encodes uncoded auxiliary data bytes by adding Reed/Solomon parity bytes to the uncoded auxiliary data bytes. The uncoded auxiliary data bytes and the Reed/Solomon parity bytes are interleaved by an interleaver 18.
20 Then, the interleaved uncoded auxiliary data bytes and the Reed/Solomon parity bytes are bitwise encoded by an outer coder 20 using either a

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convolutional code or other error correcting code.

The outer coder 20 improves the robustness of the uncoded auxiliary data bytes and the Reed/Solomon parity bytes, converting them to robust data bytes (hereinafter referred to as robust VSB data bytes) and Reed/Solomon parity bytes.

The outer coder 20, for example, may be a 1/2 rate coder which produces two output bits for every input bit, a 1/4 rate coder which produces four output bits for every input bit, or a 3/4 rate coder which produces four output bits for every three input bits. Other coders could instead be used.

At the output of the outer coder 20, a three byte transport (tx) header is added to each group of 184 coded robust VSB data and Reed/Solomon bytes to form robust VSB data packets. A multiplexer 24 multiplexes these robust VSB data packets with ATSC data packets (typically, video and audio) each comprising a three byte transport header and 184 bytes of ATSC data. Either input to the multiplexer 24 may be selected on a packet by packet basis and each selected input is supplied to an ATSC

transmitter 26. The selection by the multiplexer 24 of which input to pass to the ATSC transmitter 26 is based on a robust VSB map to be described hereinafter.

5 The ATSC transmitter 26, as is typical, includes a Reed/Solomon encoder 28, an interleaver 30, and a 2/3 rate inner encoder 32 all operating in accordance with the ATSC standard.

10 A standard ATSC receiver, such as the standard ATSC receiver 12 shown in Figure 2, receives and processes the ATSC data and discards the robust VSB data. Accordingly, the standard ATSC receiver 12 includes a 2/3 rate inner decoder 34, a deinterleaver 36, and a Reed/Solomon decoder 38, all
15 operating in accordance with the ATSC standard. The standard ATSC receiver 12, however, is programmed to decode both the ATSC data and the robust VSB data transport headers (which include the packet identifications or PID's and which have not been
20 coded by the outer coder 20). The standard ATSC receiver 12 reads the PID's of all packets and, at 40, discards those packets having the PID's of robust VSB data. The standard ATSC receiver 12 also

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includes a slice predictor 42 (such as the slice predictor disclosed in U.S. Patent No. 5,923,711) which is responsive to the inner decoded data and which provides an output back to a phase tracker and/or equalizer, as is known in the art.

The robust VSB data packets can be received, decoded, and processed by a robust VSB receiver such as the robust VSB receiver 14 shown in Figure 3. As is known, and as shown in Figure 4, the 2/3 rate inner encoder 32 of the ATSC transmitter 26 includes a precoder 44 and a four state trellis encoder 46. In combination, the precoder 44 and the four state trellis encoder 46 may be viewed as an eight state coder that produces three trellis encoded output bits (Z_0 Z_1 Z_2) for every two input bits (X_1 X_2). A mapper 48 maps the three trellis encoded output bits to a symbol having one of eight levels as shown in Figure 5. As is well known from convolutional code theory, the operation of the precoder 44 and the four state trellis encoder 46 may be viewed as an eight state 4-ary trellis.

Therefore, in the robust VSB receiver 14, a 2/3 rate inner decoder 50 may operate on an eight state 4-ary trellis which views the precoder 44 and the four state trellis encoder 46 of the 2/3 rate inner encoder 32 in combination as shown in Figure 6 to produce a soft output decision (using, for example, the SSA algorithm as described in "Optimum Soft Output Detection for Channels with Intersymbol Interference," Li, Vucetic, and Sato, IEEE Transactions on Information Theory, May, 1995). This soft decision making operation is more complicated than the widely used Viterbi algorithm, which produces a hard decision output, but the soft decision making operation more fully takes advantage of the coding gain provided by the outer coder 20.

The output of the 2/3 rate inner decoder 50 is deinterleaved by a deinterleaver 52. The robust VSB receiver 14 reads the PID's of all packets at the output of the deinterleaver 52. Based upon these PID's, the robust VSB receiver 14 discards those packets at 54 which have the PID's of ATSC data and also discards the transport headers added following the outer coder 20 and the parity

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bytes added by the Reed/Solomon encoder 28. Thus, the robust VSB receiver 14, at 54, passes only the robust VSB data packets containing the robust VSB data coded by the outer coder 20. The robust VSB data packets are decoded by an outer decoder 56, deinterleaved by a deinterleaver 58 (which is the inverse of the interleaver 18), and Reed/Solomon decoded by a Reed/Solomon decoder 60 in order to reconstruct the original uncoded auxiliary data supplied to the Reed/Solomon encoder 16 of Figure 1.

The reliable output of the outer decoder 56 (either soft or hard output may be used) is interleaved by an interleaver 62 (corresponding to the interleaver 30) in a feedback path 64 in order to restore the ordering of the outer decoded data to the order of the data in the channel. This interleaved outer decoded data can be used, for example, by a slice predictor 66 to create reliable feedback to a phase tracker and/or equalizer. However, the overall feedback delay introduced by the deinterleaver 52 and the interleaver 62 in the robust VSB receiver 14 is generally too long to

provide useful feedback to the phase tracker and/or equalizer.

The arrangement shown in Figures 7, 8, and 9 avoids the feedback delay introduced by the deinterleaver 52 and the interleaver 62 of the robust VSB receiver 14. Figure 7 shows a robust VSB transmitter 80 in which uncoded auxiliary data bytes are encoded by a Reed/Solomon encoder 82 which adds Reed/Solomon parity bytes to the uncoded auxiliary data bytes. The uncoded auxiliary data bytes and the Reed/Solomon parity bytes are interleaved by an interleaver 84. Then, the interleaved uncoded auxiliary data bytes and Reed/Solomon parity bytes are bitwise encoded by an outer coder 86 using either a convolutional code or a turbo product code, as discussed above. The bitwise output of the outer coder 86 is small block interleaved by a small block interleaver 88 in order to reduce the impact of channel burst errors on the outer decoding. The data provided by the small block interleaver 88 may be referred to as Rdata(n.o.) which stands for normally ordered robust VSB data.

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One input of a first multiplexer 92 receives ATSC formatted packets each comprising (i) a valid three byte transport header with a PID number for robust VSB data, (ii) 184 placeholder bytes of dummy robust VSB data, and (iii) twenty placeholder bytes for dummy ATSC Reed/Solomon parity data. The other input of the first multiplexer 92 receives ATSC formatted dummy packets each comprising 207 bytes of dummy ATSC data. These ATSC formatted dummy packets serve as placeholders for the real ATSC packets to be added downstream. The inputs of the first multiplexer 92 may be selected on a packet by packet basis, and this selection is based on the robust VSB map to be described later.

The selected output of the first multiplexer 92 is interleaved by an interleaver 94 according to the ATSC Standard for the convolutional byte interleave. A data replacer 96 receives both the output of the interleaver 94 and the output of the small block interleaver 88. The data replacer 96 replaces each dummy robust VSB data placeholder byte from the interleaver 94 with the next normally

ordered robust VSB data byte from the small block interleaver 88.

The output of the data replacer 96 contains normally ordered robust VSB data with interspersed transport headers, dummy ATSC Reed/Solomon parity bytes, and dummy ATSC data packet bytes. A deinterleaver 98, which operates according to the ATSC Standard for byte deinterleaving, deinterleaves the output of the data replacer 96 to thus effectively "repacketize" the data as packets of transport headers, reordered robust VSB data (Rdata(r.o.)), dummy ATSC Reed/Solomon parity bytes, and dummy ATSC data. The reordering of the normally reordered robust VSB data results from the deinterleaving of the deinterleaver 98 and the reordered data may be referred to as reordered robust VSB data.

The dummy ATSC Reed/Solomon parity bytes (20 per packet) of the robust VSB packets and the dummy ATSC data packets (207 bytes per packet) are discarded at 100. The remaining robust VSB packets, each including a transport header and reordered robust VSB data, are multiplexed by a second

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multiplexer 102 with real ATSC data packets each containing 187 bytes of a transport header and ATSC data. Either input to the second multiplexer 102 may be selected on a packet by packet basis and is
5 supplied to an ATSC transmitter 104. The selection by the second multiplexer 102 of which input to pass to the ATSC transmitter 104 is based on the robust VSB map to be described hereinafter.

The ATSC transmitter 104 typically
10 includes a Reed/Solomon encoder 106, an interleaver 108, and a twelve way 2/3 rate inner encoder 110 all operating in accordance with the ATSC standard. The Reed/Solomon encoder 106 outputs packets of transport headers, reordered robust VSB data, and
15 ATSC Reed/Solomon parity bytes multiplexed with packets of transport headers, ATSC data, and ATSC Reed/Solomon parity bytes. The ATSC Reed/Solomon parity bytes for the robust VSB data are calculated based on the reordered robust VSB data. Moreover,
20 the interleaver 108 changes the ordering of the robust VSB data so that the robust VSB data at the output of the interleaver 108 is again normally ordered robust VSB data. Also, the interleaver 108

disperses the transport headers, the ATSC Reed/Solomon parity bytes, and the ATSC data. This data is 2/3 rate coded by the twelve way 2/3 rate inner encoder 110 and is transmitted. The transmitted robust VSB data is in normal order, i.e., the order provided at the output of the small block interleaver 88. This normal order permits the robust VSB receiver to avoid the delay caused by the deinterleaver 52 and the interleaver 62 of the robust VSB receiver 14.

As shown in Figure 8, a standard ATSC receiver 120 includes a twelve way 2/3 inner decoder 122 which decodes the transmitted data to provide an output data stream comprising normally ordered robust data with interspersed transport headers, ATSC data, and ATSC Reed/Solomon parity bytes located according to the ATSC convolutional byte interleave provided by the interleaver 108. An ATSC deinterleaver 124 restores the transport headers, ATSC data, and ATSC Reed/Solomon parity bytes to their transport "packetized" positions. Also, the ATSC deinterleaver 124 converts the normally ordered robust VSB data into reordered robust VSB data.

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This reordered form permits an ATSC Reed/Solomon decoder 126 of the standard ATSC receiver 120 to correctly test parity for the robust VSB data packets. The standard ATSC receiver 120 can then read the robust VSB data packet transport headers and gracefully discard the robust VSB data packets at 128 based on their PIDs.

As shown in Figure 9, a robust VSB receiver 130 includes a soft output twelve way 2/3 rate inner decoder 132. (A hard output 2/3 decoder would result in a considerable loss of coding gain). The output of the soft output twelve way 2/3 rate inner decoder 132 comprises normally ordered robust VSB data, with reordered ATSC data, transport headers, and ATSC Reed/Solomon parity symbols dispersed within the robust VSB data at locations indicated by a discard control line 134 discussed below. A discard block 136, under control of the discard control line 134, discards the reordered ATSC data, transport headers, and ATSC Reed/Solomon parity symbols.

A small block deinterleaver 138 deinterleaves the robust VSB data. The small block

deinterleaver 138 has a relatively low delay time. This deinterleaving disperses possible burst errors in the robust VSB data at the output of the soft output twelve way 2/3 rate inner decoder 132. The normally ordered robust VSB data is bitwise decoded by an outer decoder 140 which also packs the robust VSB data into bytes. The amp information telling the outer decoder 140 what decoding rate to use on what data is provided to the outer decoder 140 at an R_{max} Data input. Neither the deinterleaver 52 nor the interleaver 62 is needed in the robust VSB receiver 130 allowing for lower overall feedback delay to the phase tracker and/or equalizer. The outer decoded data can be used, for example, by an enhanced slice predictor 142 to generate feedback to the phase tracker and/or equalizer. If desired, the feedback may be gated, or the step size of the equalizer gradient algorithm adjusted proportionally to the reliability of the decoded data.

The robust VSB data packet payload decoded by the outer decoder 140 is deinterleaved by a deinterleaver 144 (which is the inverse of the interleaver 84) and is Reed/Solomon decoded by a

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Reed/Solomon decoder 146 (corresponding to the Reed/Solomon encoder 82) in order to reconstruct the original uncoded auxiliary data supplied to the Reed/Solomon encoder 82 of Figure 7.

5 As provided in the ATSC standard, a frame comprises a plurality of segments each containing a predetermined number of bytes. The first segment of a frame is a frame sync segment, and the remaining segments in the frame are data segments. Although
10 robust VSB data can be transmitted in segments or in partial segments, it is convenient to transmit robust VSB data in segment pairs. The robust VSB map discussed above indicates which segment pairs contain robust VSB data so that the discard block
15 136 can correctly discard the reordered ATSC data before the reordered ATSC data can get to the outer decoder 140. The transport headers and the ATSC Reed/Solomon parity data for all segments (robust VSB and ATSC) must also be discarded by the discard
20 block 136.

A conceptually simple circuit to generate the appropriate control signal on the discard control line 134 to control this discarding function

is shown in Figure 10, together with the relevant portion of the robust VSB receiver 130. The robust VSB receiver 130 uses received map information (the method for transmission and reception of this map information is described below) to instruct a dummy segment generator 150 when to construct dummy 207 byte segments. The dummy segment generator 150 also uses the frame sync signal. For each ATSC dummy segment, the dummy segment generator 150 sets all bytes to FF. For each robust VSB data dummy segment, the dummy segment generator 150 sets the transport header and ATSC Reed/Solomon parity bytes to FF. The dummy segment generator 150 sets the rest of the bytes of each robust VSB data dummy segment to 00.

These dummy segments are fed by the dummy segment generator 150 to an ATSC convolutional byte interleaver 152 whose output is then used to control the discard block 136 which then responds to the FF and 00 codes to correctly discard the reordered ATSC data, the transport headers, and the ATSC Reed/Solomon parity data which are interleaved

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within the received data stream. The discard block 136, thus, passes only the robust VSB data.

Figure 11 shows a multiple outer code robust VSB transmitter 160. The robust VSB transmitter 160 operates similarly to the robust VSB transmitter 80 of Figure 7. The robust VSB transmitter 160 has a first Reed/Solomon encoder 162 which encodes first uncoded auxiliary data by adding Reed/Solomon parity bytes to the first uncoded auxiliary data, a second Reed/Solomon encoder 164 which encodes second uncoded auxiliary data by adding Reed/Solomon parity bytes to the second uncoded auxiliary data, and a third Reed/Solomon encoder 166 which encodes third uncoded auxiliary data bytes by adding Reed/Solomon parity bytes to the third uncoded auxiliary data. The Reed/Solomon encoded first uncoded auxiliary data are interleaved by a first interleaver 168, the Reed/Solomon encoded second uncoded auxiliary data are interleaved by a second interleaver 170, and the Reed/Solomon encoded third uncoded auxiliary data are interleaved by a third interleaver 172. Then, the interleaved Reed/Solomon encoded first uncoded auxiliary data

are bitwise encoded by a first outer coder 174, the interleaved Reed/Solomon encoded second uncoded auxiliary data are bitwise encoded by a second outer coder 176, and the interleaved Reed/Solomon encoded third uncoded auxiliary data are bitwise encoded by a third outer coder 178. The bitwise output of the first outer coder 174 is interleaved by a first small block interleaver 180, the bitwise output of the second outer coder 176 is interleaved by a second small block interleaver 182, and the bitwise output of the third outer coder 178 is interleaved by a third small block interleaver 184.

The first outer coder 174 is a $1/4$ rate coder, the second outer coder 176 is a $1/2$ rate coder, and the third outer coder 178 is a $3/4$ rate coder, although any other combination of these or other outer coders using different coding rates could be used. The data outputs of the first, second, and third small block interleavers 180, 182, and 184 are selected by a multiplexer 186 under control of a select input which determines the order in which the differently outer coded data are inserted into the frame to be transmitted. The data

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at the output of the multiplexer 186 may be referred to as Rdata(n.o.) which, as before, stands for normally ordered robust VSB data.

5 The top three inputs of a multiplexer 190 receive ATSC format packets each having of a valid three byte transport header with a PID number for robust VSB data, 184 placeholder bytes of dummy robust VSB data, and twenty dummy placeholder bytes for ATSC Reed/Solomon parity data. The robust VSB 10 data at the topmost input of the multiplexer 190 correspond to 1/4 rate coded data from the first outer coder 174, the robust VSB data at the next input of the multiplexer 190 correspond to 1/2 rate coded data from the second outer coder 176, and the 15 robust VSB data at the next input of the multiplexer 190 correspond to 3/4 rate coded data from the third outer coder 178. The data supplied to the bottommost input of the multiplexer 190 comprises ATSC format dummy packets each having 207 bytes of 20 dummy ATSC data. These dummy ATSC data packets serve as placeholders for the real ATSC data packets to be added downstream of the multiplexer 190. The inputs to the multiplexer 190 may be selected on a

packet by packet basis in accordance with the input on a select line. This selection is based on the robust VSB data map to be described below.

The output of the multiplexer 190 is interleaved by an interleaver 192 in order to achieve a correct ATSC convolutional interleave. A data replacer 194 receives both the output of the interleaver 192 and the output of the multiplexer 186. The data replacer 194 replaces each dummy robust VSB data placeholder byte from the multiplexer 190 with the next corresponding normally ordered robust VSB data byte from the multiplexer 186.

The output of the data replacer 194 contains normally ordered robust VSB data (which is 1/4 rate coded, 1/2 rate coded, and/or 3/4 rate coded, as appropriate) with interspersed transport headers, dummy ATSC Reed/Solomon parity bytes, and dummy ATSC data packet bytes. A convolutional byte deinterleaver 196 (as described in the ATSC Standard) deinterleaves the output of the data replacer 194 to thus effectively "repacketize" the data as packets of transport headers, reordered

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robust VSB data (1/4, 1/2, and/or 3/4 rate coded), dummy ATSC Reed/Solomon parity bytes, and dummy packets of ATSC data. The reordering of the normally ordered robust VSB data results from the deinterleaving of the deinterleaver 196.

The dummy ATSC Reed/Solomon parity bytes (20 per packet) and the dummy ATSC data packets (207 bytes per packet) are discarded at 198 in a manner similar to that provided by the discard control line 134 and the discard block 136 of Figure 9. The remaining robust VSB packets, each including a transport header and reordered robust VSB data, are multiplexed by a multiplexer 200 with real ATSC data packets each containing 187 bytes of a transport header and ATSC data. Either input to the multiplexer 200 may be selected on a packet by packet basis and is supplied to an ATSC transmitter 202. The selection by the multiplexer 200 of which input to pass to the ATSC transmitter 202 is based on the robust VSB map to be described hereinafter.

The ATSC transmitter 202 typically includes a Reed/Solomon encoder 204, an interleaver 206, and a twelve way 2/3 rate inner encoder 208 all

operating in accordance with the ATSC standard. The Reed/Solomon encoder 204 outputs packets of transport headers, reordered robust VSB data, and ATSC Reed/Solomon parity bytes multiplexed with packets of transport headers, ATSC data, and ATSC Reed/Solomon parity bytes. The ATSC Reed/Solomon parity bytes for the robust VSB data are calculated based on the reordered robust VSB data. Moreover, the interleaver 206 changes the ordering of the robust VSB data so that the robust VSB data at the output of the interleaver 206 are again normally ordered robust VSB data. Also, the interleaver 206 disperses the transport header bytes, the ATSC Reed/Solomon parity bytes, and the ATSC data. These data are 2/3 rate coded by the twelve way 2/3 rate inner encoder 208 and are transmitted. The transmitted robust VSB data are in normal order, i.e., the order provided at the output of the multiplexer 186. This normal data order permits the robust VSB receiver to avoid the delay caused by the deinterleaver 52 and the interleaver 62.

As discussed above, an ATSC frame comprises a frame sync segment and a plurality of

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data segments and, for convenience, robust VSB data are packed into groups of four segments. More specifically, Figure 12 shows an example of four data segments that may be used in a frame to transmit robust VSB data that is 1/2 rate coded, Figure 13 shows an example of four data segments that may be used in a frame to transmit robust VSB data that is 1/4 rate coded, and Figure 14 shows an example of four data segments that may be used in a frame to transmit robust VSB data that is 3/4 rate coded. These examples represent the frame prior to the interleaver 108 and assume that each group of four robust VSB data segments contains an integral number of robust Reed/Solomon encoded blocks each of which is 184 bytes long, of which twenty bytes are parity bytes.

For the case of a 1/2 rate outer code, Figure 12 shows that the outer coder outputs two bits for each input bit. A robust VSB data packet is packed as one RVSB Reed-Solomon block to a pair of data segments (one bit per symbol) so that, for a 1/2 rate outer code, four segments contain two robust Reed/Solomon encoded blocks. As shown in

Figure 13, for the case of a $1/4$ rate outer code, the outer coder outputs four bits for each input bit. Robust VSB data is packed as one RVSB Reed-Solomon block for every four data segments ($1/2$ bit per symbol) so that, for a $1/4$ rate outer code, four segments contain one robust Reed/Solomon encoded block. As shown in Figure 14, for the case of a $3/4$ rate outer code, the outer coder outputs four bits for each three input bits. In this case, transmitted symbol and byte boundaries do not always match. However, three complete RVSB Reed-Solomon blocks will pack exactly into four data segments (1.5 bits per symbol) so that, for a $3/4$ rate outer code, four segments contain three robust Reed/Solomon encoded blocks.

Accordingly, Figures 12, 13, and 14 can be represented by the following table:

S	X	Y
$1/2$	1	2
$1/4$	1	4
$3/4$	3	4

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where X represents the number of complete robust Reed/Solomon encoded blocks and Y represents the number of frame segments required to contain the corresponding number X of robust Reed/Solomon encoded blocks.

However, it should be understood that other coding rates can be used in conjunction with the present invention and, therefore, the above table will change depending upon the particular coding rates that are used.

The interleavers 18, 84, 168, 170, and 172 are shown in more detail in Figure 15, and the deinterleavers 58 and 144 are shown in more detail in Figure 16, assuming that a robust Reed/Solomon encoded block is chosen to be 184 bytes long. The interleavers 18, 84, 168, 170, and 172 are $B = 46$, $M = 4$, $N = 184$ convolutional interleavers that byte wise interleave the robust VSB data. This interleaving scheme is the same as the ATSC interleaver scheme described in the ATSC Digital Television Standard A/53 and the Guide to the Use of the ATSC digital Television Standard A/54, except that the B parameter for the robust interleaver is

46 instead of 52 and the parameter N is 184 instead of 208. This interleaver is needed so that a robust VSB receiver can cope with long bursts of noise on the channel even though the ATSC deinterleaver (D_a) is bypassed as shown in Figure 9.

As shown in Figure 16, the deinterleavers 58 and 144 are $B = 46$, $M = 4$, $N = 184$ convolutional deinterleavers that byte wise deinterleave the robust VSB data. This deinterleaving scheme is also the same as the ATSC deinterleaver scheme described in the ATSC Digital Television Standard A/53 and the Guide to the Use of the ATSC digital Television Standard A/54, except that the B parameter for the robust deinterleaver is 46 instead of 52 and the parameter N is 184 instead of 208.

Because a robust VSB Reed/Solomon block comprises 184 bytes, and because an integral number of robust VSB Reed/Solomon blocks are in a data frame, the number of robust VSB data bytes plus robust VSB Reed/Solomon parity bytes in a data frame is always evenly divisible by 46. Therefore, the frame sync segment can be used as a synchronizer for the deinterleavers 58 and 144 (D_r) in the receiver,

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regardless of the value of G (to be described below). At frame sync, the deinterleaver commutators are forced to the top positions. The deinterleavers 58 and 144 are byte wise deinterleavers.

Data Mapping

As discussed above, each data frame may contain a mix of robust VSB data segments and ATSC (non-robustly coded) data segments. Moreover, the robust VSB data may contain data coded with a mix of coding rates. The robust VSB receiver 14 or 130 must have a robust VSB map that indicates which segments are robust VSB coded and which outer code is used for the robust VSB coding so that the robust VSB receiver 14 or 130 can correctly process the robust VSB data and discard the ATSC data. The robust VSB transmitters 10, 80, and 160 also use the robust VSB map to control their corresponding multiplexing and discard functions. This robust VSB map is transmitted by the robust VSB transmitter 10, 80, or 160 to the robust VSB receiver 14 or 130

along with all the other data in a manner described below.

The presence, amount, and location of the robust VSB data in a data frame encoded with a particular outer code are indicated by one or more numbers S_c that appear as two level data in the frame sync segment of the data frame. As is known, the frame sync segment is the first segment in a frame. So, for the outer codes described above (1/4 rate, 1/2 rate, and 3/4 rate), the frame sync segment should preferably contain $[S_{1/4} S_{1/2} S_{3/4}]$. Each S_c (such as $S_{1/4}$ or $S_{1/2}$ or $S_{3/4}$) is encoded as eighteen symbols (bits) of two level data. For all three codes, a total of $3 \times 18 = 54$ symbols are needed as a definition of the robust VSB map. These symbols are inserted into the reserved area near the end of each frame sync segment (just before the twelve precoding bits). For each group of eighteen bits ($b_{18} \dots b_1$), the last six bits ($b_6 \dots b_1$) represent the number G of groups of eight segments (8 segments = 2, 4 or 6 robust VSB data packets depending on the outer code) mapped as robust VSB data in the current frame. The twelve preceding

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bits are for comb filter compensation (see the Guide to the Use of the ATSC digital Television Standard A/54). Accordingly, as shown in Figure 18, bits b_6 . . . b_1 represent the number G , bits b_{18} . . . b_{13} are the complement of bits b_6 . . . b_1 , and bits b_{12} . . . b_7 can be alternating +1 and -1 (or any other pattern).

Let it be assumed that $S = S_{1/4} + S_{1/2} + S_{3/4}$. Because $312/8 = 39$, 0-39 groups of eight segments can be mapped as robust VSB data or 8 VSB data (ATSC data). Therefore, each S_c may have a value of 0 . . . 39, as long as their sum S is ≤ 39 .

The robust VSB data segments are preferably distributed as uniformly as possible over the data frame. For example, if $S = 1$, then the following eight segments are mapped as robust VSB data segments and all other segments are mapped as ATSC data segments: 1, 40, 79, 118, 157, 196, 235, and 274. If $S = 2$, then the following sixteen segments are mapped as robust VSB data segments and all other segments are mapped as ATSC data segments: 1, 20, 39, 58, 77, 96, 115, 134, 153, 172, 191, 210, 229, 248, 267, and 286. These examples continue

until $S = 39$, where the whole data frame is mapped as robust VSB data segments. For some values of S , the spacing between robust VSB data segment pairs is not perfectly uniform. However, for any value of S , the spacing is fixed in advance and, therefore, known to all receivers.

If a frame contains robust VSB data provided by three outer coders operating at $1/4$ rate, $1/2$ rate, and $3/4$ rate, then the data from these three outer coders may be divided in a frame such that, as to RVSB segments, the first $S \times S_{1/4}$ segments contain the $1/4$ rate outer coded data, the next $S \times S_{1/2}$ segments contain the $1/2$ rate outer coded data, and the last $S \times S_{3/4}$ segments contain the $3/4$ rate outer coded data. However, other robust VSB data segment organizations are possible for these three outer coders or for any number of other types of outer coders.

Because this robust VSB map is contained in the frame sync segment, as discussed above, the robust VSB map does not enjoy the same level of coding gain as the robust VSB data. However, the robust VSB map may still be reliably acquired by a

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robust VSB receiver by correlating the robust VSB map over some number of frames. Therefore, the robust VSB map should not change too often (for example, not more often than every -60 frames).

5 The above mapping method allows a receiver to reliably and simply acquire the robust VSB map by correlation. Once a receiver has acquired the map, it is desirable for the receiver to instantly and reliably track changes in the map. In order to
10 instantly and reliably track changes in the map, the definition in the robust VSB map for each outer code, excluding the comb compensation bits, is duplicated in the first robust VSB Reed/Solomon encoded block of the frame. In addition, there is
15 data indicating (i) when in the future the map will change and (ii) the future new map definition. The first robust VSB data packet of a frame for an outer coder, therefore, has the structure shown in Figure 17, where the robust VSB map definition data is
20 given by the following: eight bits designating the current map (only six of these bits are used); eight bits designating the number of frames until the map changes (1-125; if 0, then no change

coming); and, eight bits designating the next map
(again, only six of these bits are used). The
remaining portion of the first robust VSB data
packet is data. The first RVSB segment in a frame
5 for a respective outer coder has the arrangement
shown Figure 17.

In this way, a receiver can track map
changes using reliable robust VSB data. Even if a
burst error destroys a number of the frames, the
10 receiver can keep its own frame countdown using the
number of frames read from a previously received
frame. If the receiver finds at any time that the
definition for an outer code previously acquired by
the frame sync correlation does not match the
15 definition for that outer code in the first robust
VSB data segment, the receiver should restart its
map acquisition process.

RVSB Enhanced Slice Prediction and Equalizer Feedback

20 ATSC 8 VSB receivers make important use of
adaptive equalization and phase tracking as
explained in the ATSC Digital Television Standard

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A/53 published by the Advanced Television Systems Committee, in the Guide to the Use of the ATSC Digital Television Standard A/54, also published by the Advanced Television Systems Committee. RVSB as
5 described above has features that allow for improvements in adaptive equalization and phase tracking.

One such improvement results from feeding back delayed reliable estimates of the input symbol
10 level to the adaptive equalizer and/or phase tracker based on a sequence estimation from an enhanced Viterbi Algorithm. (See "The Viterbi Algorithm," G. D. Forney, Jr., Proc. IEEE, vol 61, pp. 268-278, March, 1973). This type of feedback avoids the need
15 for "re-encoding," which has a state initialization problem.

U.S. Patent No. 5,923,711, entitled "Slice Predictor for a Signal Receiver," discloses an ATSC
8 VSB receiver which utilizes a slice predictor in
20 order to provide more reliable feedback to the phase tracker or adaptive equalizer. This feedback can be made even more reliable by a enhanced slice predictor system 300 shown in Figure 19. The

enhanced slice predictor system 300 has an inner decoder 302 and an outer decoder 304 which operate similarly to the inner decoders and outer decoders described above.

5 The slice prediction output from the inner decoder 302 works in a manner similar to that described in the aforementioned U.S. Patent No. 5,923,711. As explained above, the inner decoder 302 is based on an 8 state 4-ary trellis that
10 includes a precoder. Based on the best path metric at the current time t , the slice predictor of the inner decoder 302 decides a most likely state at time t . Then, based on the next possible pair of states, four possible predicted input levels (out of
15 eight) for the next symbol at time $t + 1$ are selected. For example, as shown by the inner decoder trellis in Figure 20, if the most likely state at time t is state one, the next state is $\in [1 \ 5 \ 2 \ 6]$. Therefore, the next input level at time $t +$
20 1 may be $-7, +1, -3$, or $+5$. These next input levels correspond to decoded bit pairs 00, 10, 01, and 11, respectively.

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Similarly, the outer decoder 304 also finds the best path metric for the current time t for the respective trellis. A portion of this trellis is shown in Figure 21 for an exemplary outer decoder and may be applied generally to all three outer codes. As shown in Figure 21, two possible outer decoder input bit pairs are selected for the time $t + 1$ based on the next possible pair of states. By way of example, the two possible outer decoder input bit pairs may be 11 or 01. The bit pair chosen by the outer decoder 304 is sent to a prediction enhancer 306 which selects amplitude levels +5 or -3 from the set of four levels previously selected by the slice predictor of the inner decoder 302 as the enhanced slice prediction for time $t + 1$. Because the slice prediction of the inner decoder 302 is near zero delay, but because the outer decoder 304 cannot operate on the same symbol until after the inner decoder 302 has provided a decoded soft output, a delay module 308 provides a delay time slightly greater than the traceback delay time of the inner decoder 302. The slice prediction provided by the prediction enhancer

306 may be supplied as feedback to an equalizer of phase tracker 310.

With some additional delay time, the outer decoder 304 can make a final hard decision and select a single most likely input bit pair for time $t + 1$. For example, if 11 is found to be the most likely input bit pair to the outer decoder 304 as determined by its Viterbi Algorithm, this information is sent by the outer decoder 304 to the prediction enhancer 306 which then chooses +5 from the set of four levels and corresponding bit pairs already selected by the slice predictor of the inner decoder 302. The outer code can be a convolutional code or other type of error correction code. The predictor enhancer 306 is disabled during the periods of time when ATSC data is being received.

A feedback enhanced maximum likelihood sequence estimator (MLSE) slice predictor system 320 uses the Viterbi Algorithm and is shown in Figure 22 along with other relevant parts of an RVSB receiver. The feedback enhanced MLSE slice predictor system 320 has an inner decoder 322 and an outer decoder 324 which operate similarly to the inner decoder 302

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and the outer decoder 304 described above. However, instead of using the slice prediction output of the inner decoder 302, an enhanced MLSE module 326 is configured to execute the usual Viterbi Algorithm on the received signal by operating the eight state 2/3 rate code trellis (the same trellis used by the inner decoder 322, including the precoder).

The enhanced MLSE module 326 selects as its next input either (i) the noisy eight level received signal as delayed by a delay module 328 if the next input is a non-RVSB symbol or (ii) the bit pair decision output of the outer decoder 324 (hard or soft) if the next input is a RVSB symbol. The enhanced MLSE module 326 makes this selection according to the symbol by symbol information in the RVSB map.

The enhanced MLSE module 326 outputs one of eight possible symbols as its slice prediction, and this slice prediction (symbol decision) is provided by the enhanced MLSE module 326 as feedback to an equalizer or phase tracker 330.

The enhanced MLSE module 326 should follow a more correct path through the eight state trellis

than does the inner decoder 322 because the enhanced MLSE module 326 gets more reliable input from the outer decoder 324 when an RVSB symbol is available.

The output of the enhanced MLSE module 326 may be a hard slice decision or a soft level. Also, any symbol reliability indication from the inner decoder 322 or the outer decoder 324 may be used to change the step size of the equalizer LMS algorithm. (See the Guide to the Use of the ATSC Digital Television Standard A/54.)

An optional predetermined coded training sequence may be included in a specified portion of the first RVSB segment of a data field. This sequence is known in advance by both the transmitter and receiver. During the time the decoded training sequence is output from the outer decoder 324, the input to the enhanced MLSE module 326 is switched to a stored version of the decoded training sequence.

Certain modifications of the present invention have been discussed above. Other modifications will occur to those practicing in the art of the present invention. For example, although the standard ATSC receiver 12 and the robust VSB

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receiver 14 are shown above as separate receivers,
the functions of the standard ATSC receiver 12 and
the robust VSB receiver 14 can be combined in two
data paths of a single receiver capable of decoding
both types of data (ATSC data and robust VSB data).

Accordingly, the description of the
present invention is to be construed as illustrative
only and is for the purpose of teaching those
skilled in the art the best mode of carrying out the
invention. The details may be varied substantially
without departing from the spirit of the invention,
and the exclusive use of all modifications which are
within the scope of the appended claims is reserved.

CLAIMS:

2 1. A method of providing enhanced slice
3 prediction, the method being CHARACTERIZED by the
4 following steps:
5 receiving an input containing first and
6 second data, wherein the first and second data have
7 the same n level constellation and different bit
8 rates;
9 decoding only the second data with a
10 decoder;
11 producing an output in response to the
12 input and the decoder, wherein the output is
13 confined to at least one but fewer than $n/2$ of the n
14 constellation levels, and wherein $n > 2$; and,
15 providing the output as the enhanced slice
16 prediction.

1 2. The method of claim 1 wherein the
2 decoder is a first decoder, wherein the receiving
3 step comprises the step of decoding the input with a
4 second decoder to recover the first and second data,
5 wherein the second decoder has n states, wherein the

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6 producing step comprises the step of choosing $n/4$
7 states out of $n/2$ states of the n states of the
8 second decoder, and wherein the providing step
9 comprises the step of providing the $n/4$ states as
10 the enhanced slice prediction.

1 3. The method of claim 2 further
2 comprising the step of delaying the choosing step
3 based upon a processing time of the second decoder.

1 4. The method of claim 1 wherein the
2 decoder is a first decoder, wherein the receiving
3 step comprises the step of decoding the input with a
4 second decoder to recover the first and second data,
5 wherein the second decoder has n states, wherein the
6 producing step comprises the step of choosing only
7 one state out of $n/2$ states of the n states of the
8 second decoder, and wherein the providing step
9 comprises the step of providing the one state as the
10 enhanced slice prediction.

1 5. The method of claim 4 further
2 comprising the step of delaying the choosing step
3 based upon a processing time of the second decoder.

1 6. The method of claims 1, 2, 3, 4, or 5
2 wherein n is eight.

1 7. The method of claim 1 wherein the
2 producing step comprises the following steps:
3 decoding the input when the second data is
4 not available so as to produce the output; and,
5 decoding the second data when the second
6 data is available so as to produce the output.

1 8. The method of claim 7 further
2 comprising the step of delaying the decoding of the
3 input based at least in part upon a processing time
4 of the decoder.

1 9. The method of claim 7 wherein the
2 providing step comprises providing only one state as
3 the enhanced slice prediction.

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1 10. The method of claim 7 further
2 comprising the step of selecting between decoding
3 the input and the second data in response to a
4 received map.

1 11. The method of claim 1 wherein the
2 decoder is a first decoder, wherein the receiving
3 step comprises the step of decoding the input with a
4 second decoder to recover the first and second data,
5 wherein the step of decoding only the second data
6 comprises the step of decoding the second data with
7 the first decoder to produce decoded second data,
8 and wherein the producing step comprises the
9 following steps:
10 producing the output by decoding the input
11 with a third decoder when the decoded second data is
12 not available; and,
13 producing the output by decoding the
14 second decoded data with the third decoder when the
15 decoded second data is available.

1 12. The method of claim 11 further
2 comprising the step of delaying the step of decoding
3 the input with the third decoder.

1 13. The method of claim 11 wherein the
2 third decoder implements a Viterbi algorithm.

1 14. The method of claim 11 wherein the
2 providing step comprises the step of providing only
3 one state of the third decoder as the enhanced slice
4 prediction.

1 15. The method of claim 11 further
2 comprising the step of selecting between decoding
3 the input and the decoded second data in response to
4 a received map.

1 16. The method of claims 7 or 11 wherein
2 the first data comprises eight level non-RVSB
3 symbols, and wherein the second data comprises eight
4 level RVSB symbols.

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1 18. The method of claim 1, 7, or 11
2 wherein the providing step comprises the step of
3 providing the enhanced slice prediction based upon a
4 known training signal when a transmitted training
5 signal is contained in a received signal.

1 18. The method of claim 1 further
2 comprising the step of providing the enhanced slice
3 prediction as feedback to an equalizer.

1 19. The method of claim 1 further
2 comprising the step of providing the enhanced slice
3 prediction as feedback to a phase tracker.

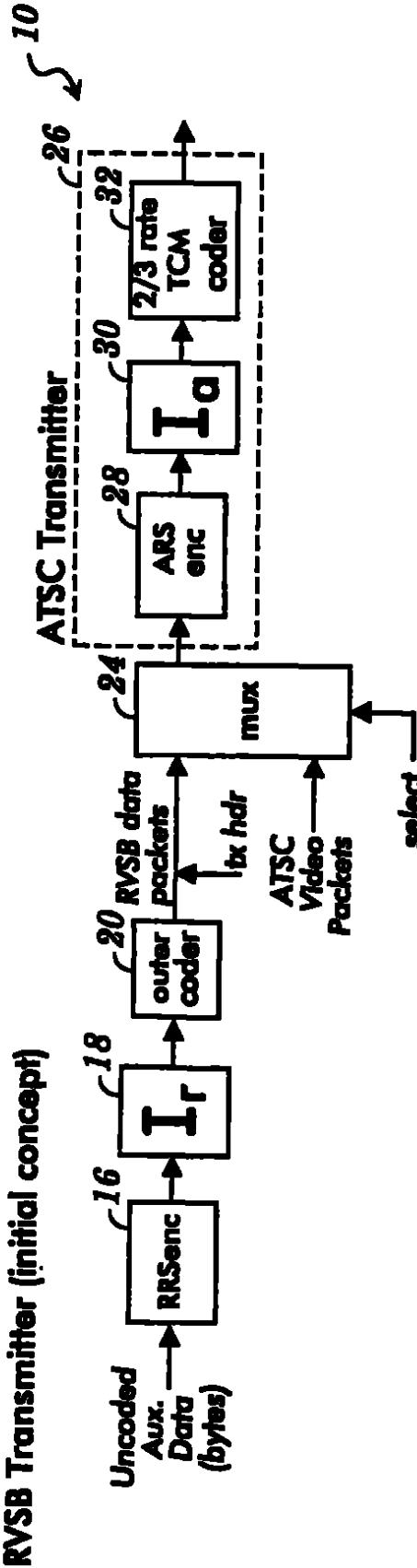


Figure 1

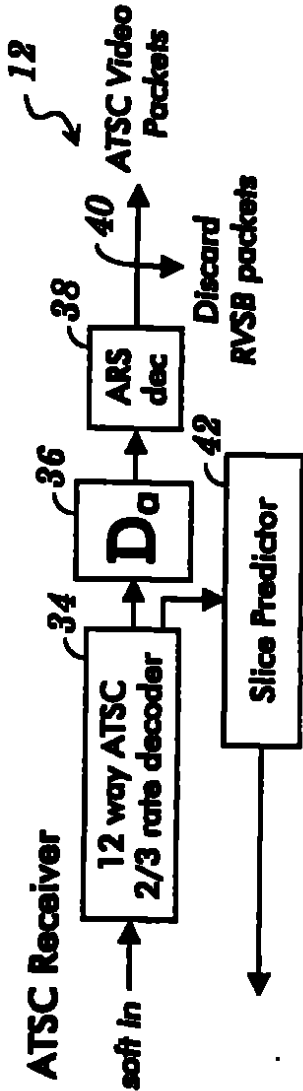
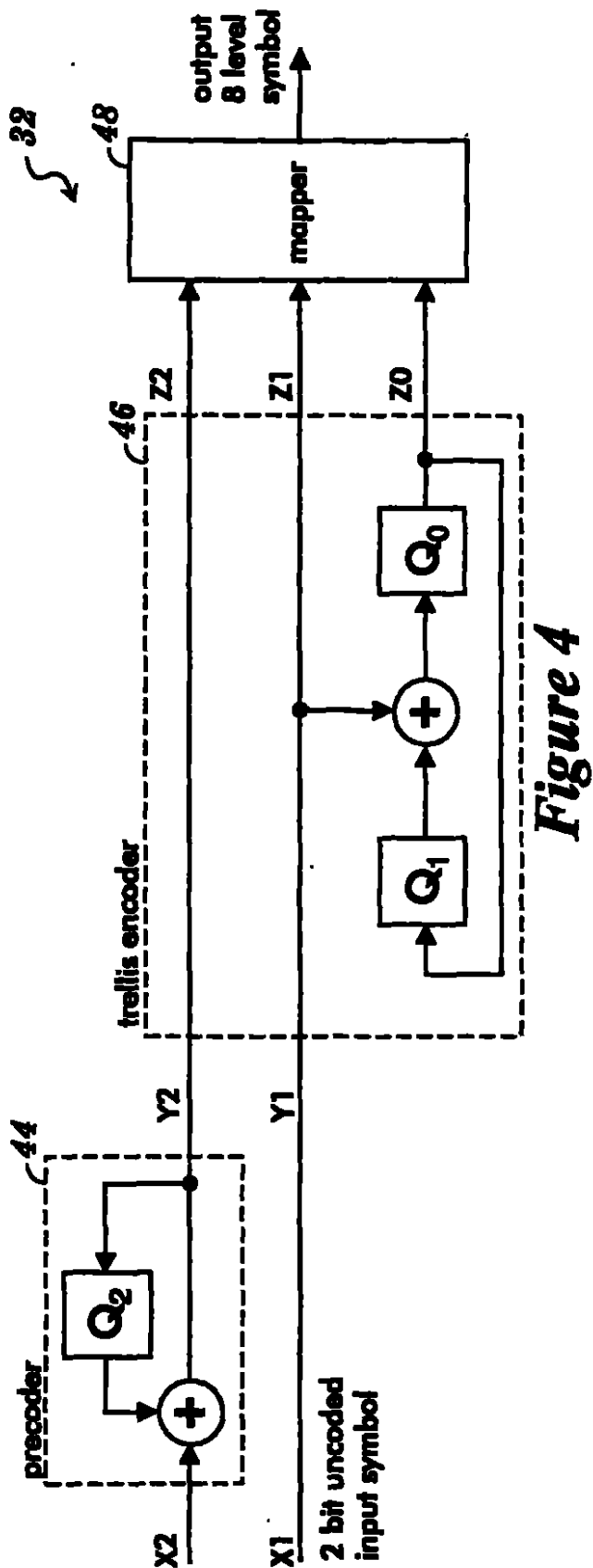
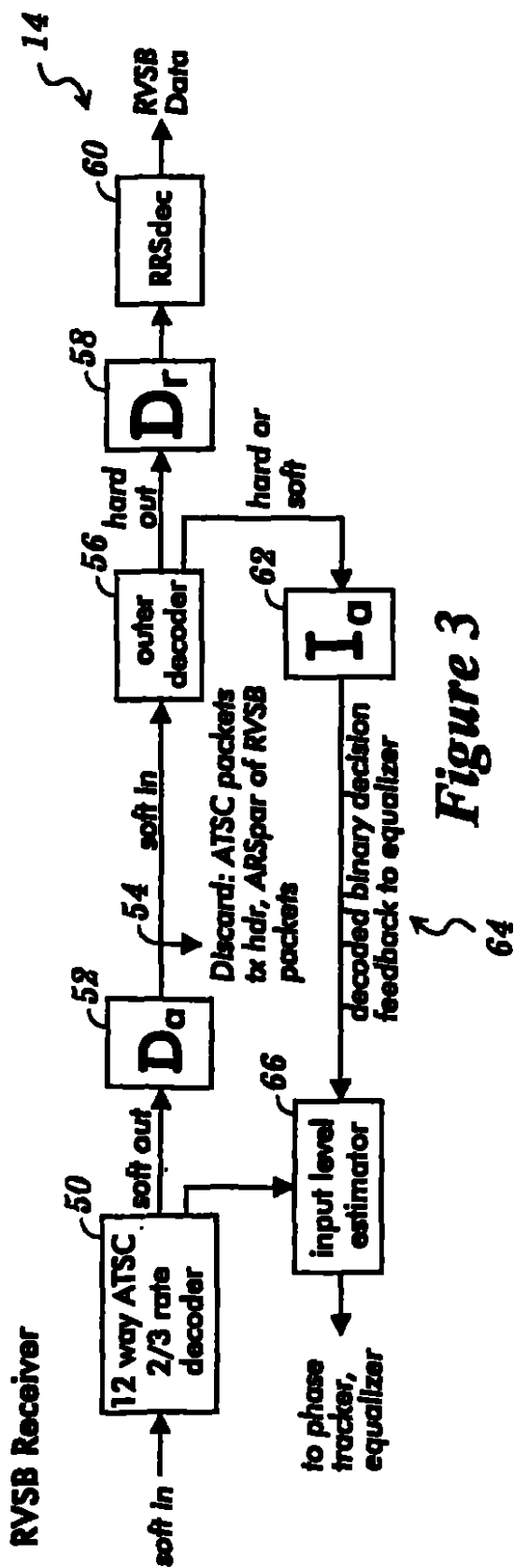


Figure 2

mapper function				level
Z2	Z1	Z0		
0	0	0	-7	
0	0	1	-5	
0	1	0	-3	
0	1	1	-1	
1	0	0	+1	
1	0	1	+3	
1	1	0	+5	
1	1	1	+7	

Figure 5



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branch label :
 $X_2 X_1$ / mapped output level

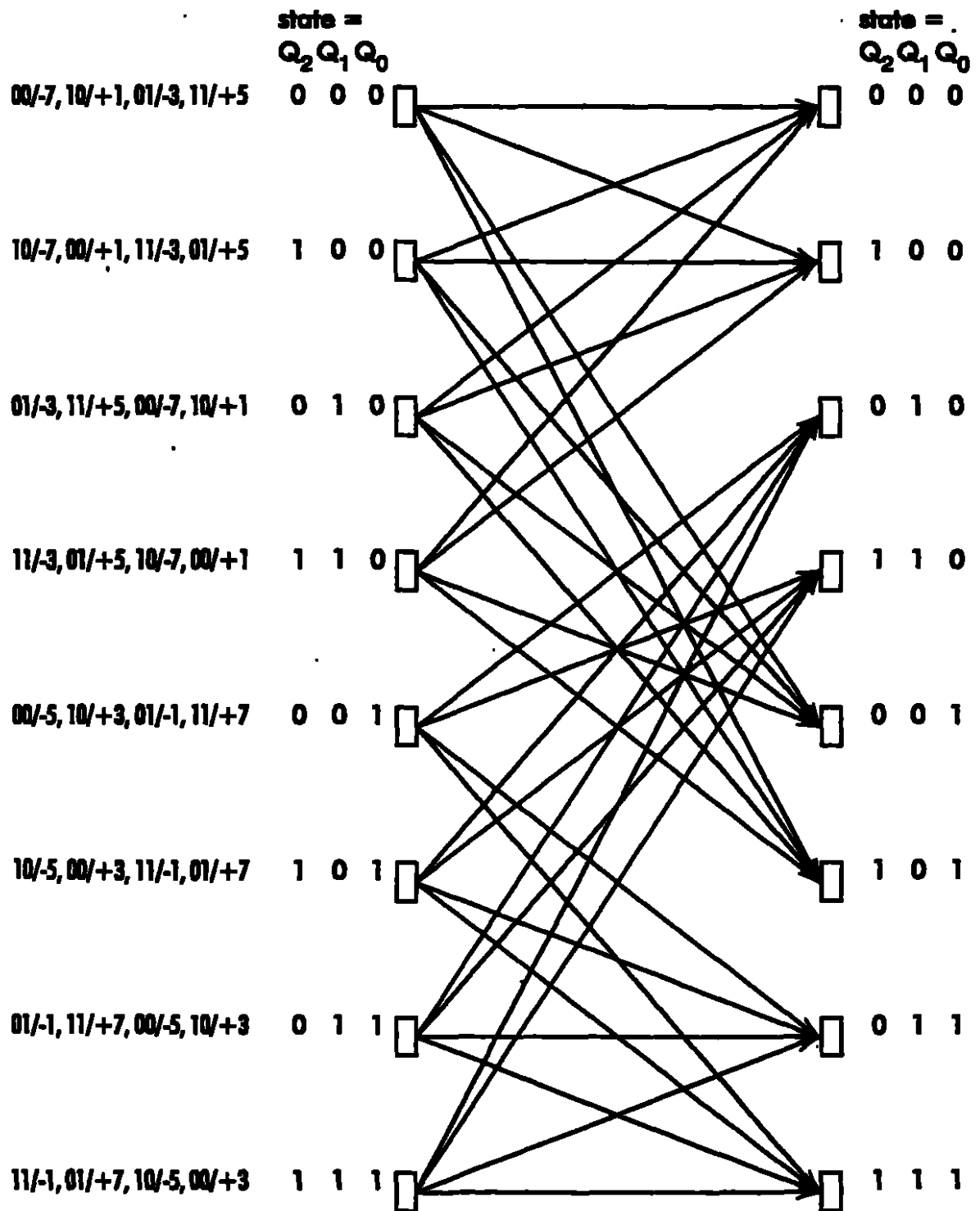


Figure 6

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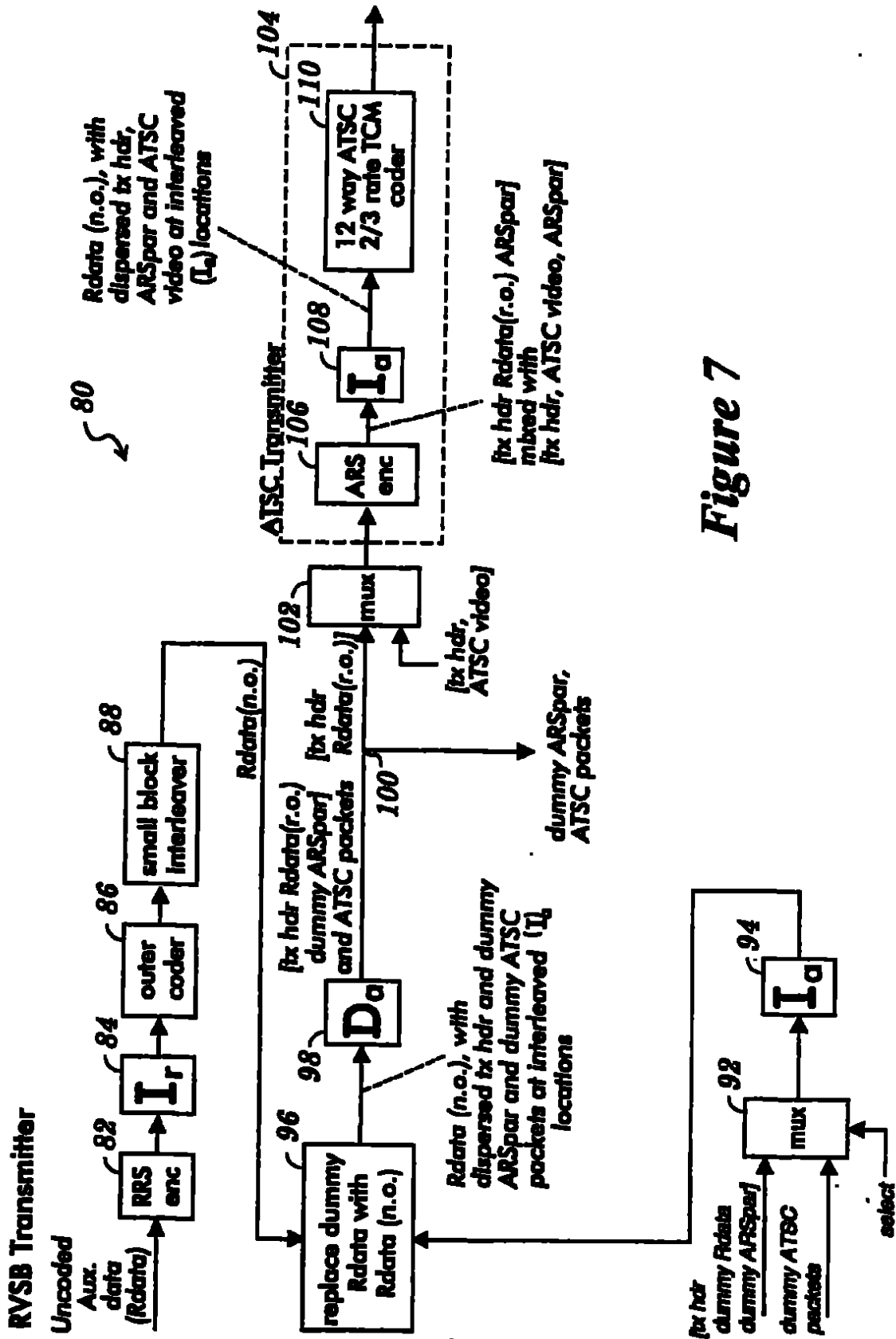


Figure 7

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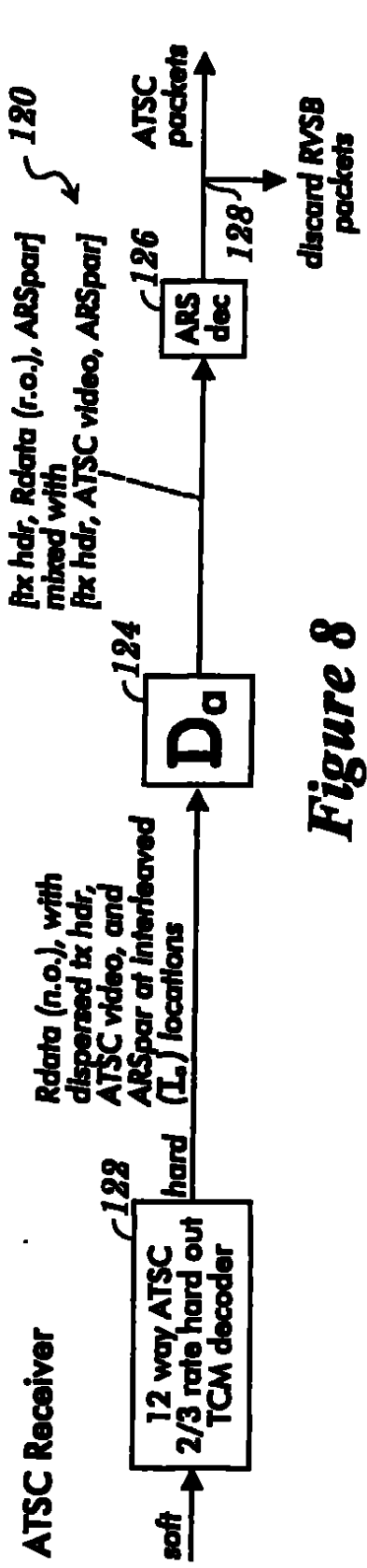


Figure 8

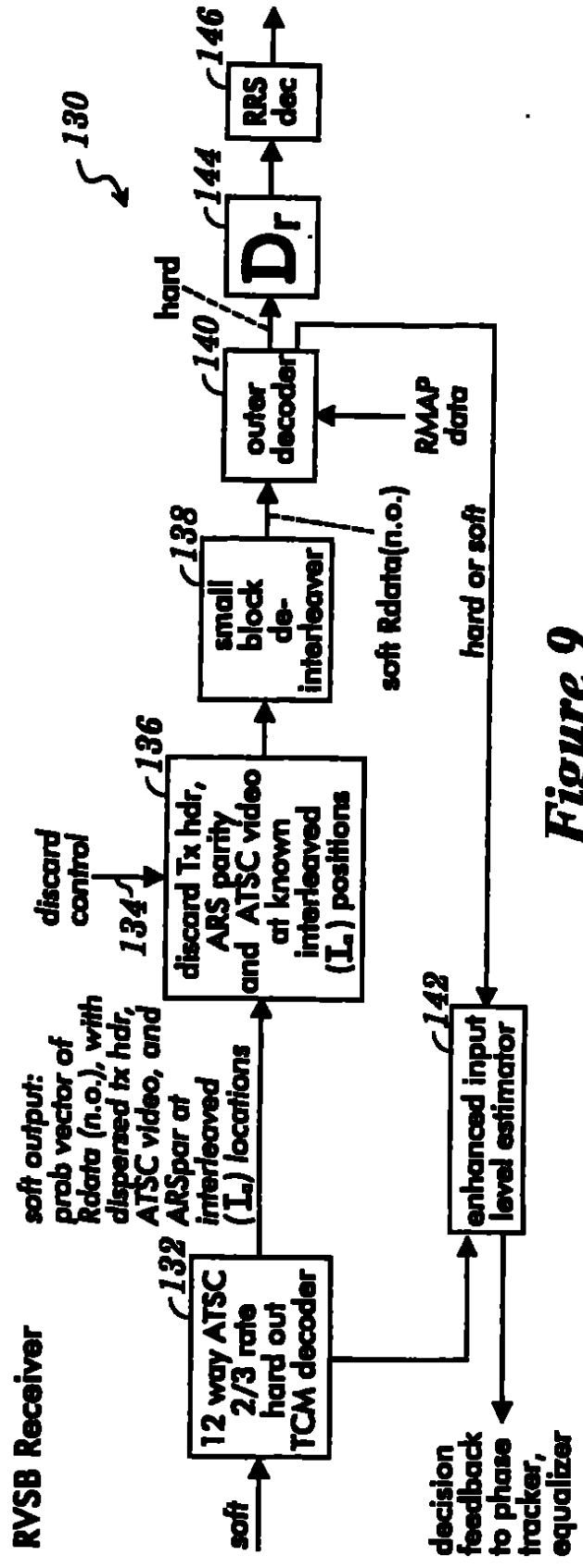


Figure 9

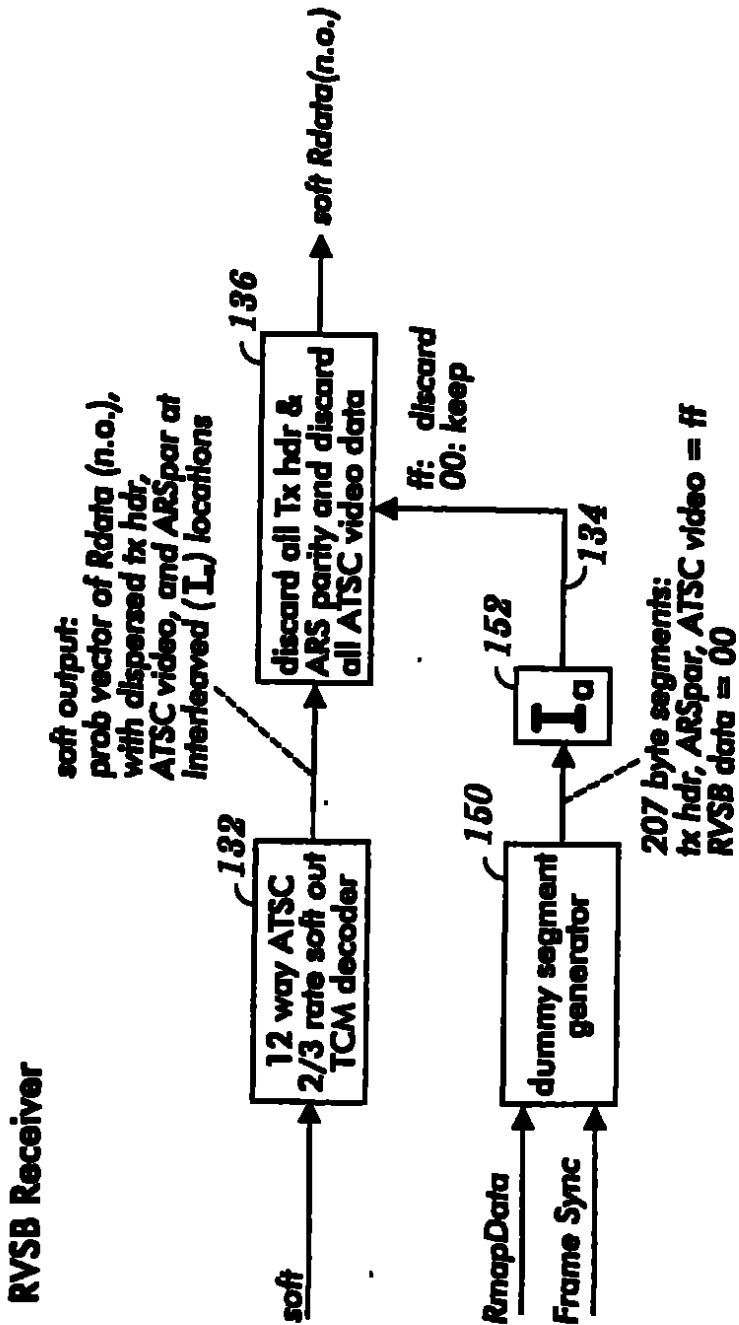


Figure 10

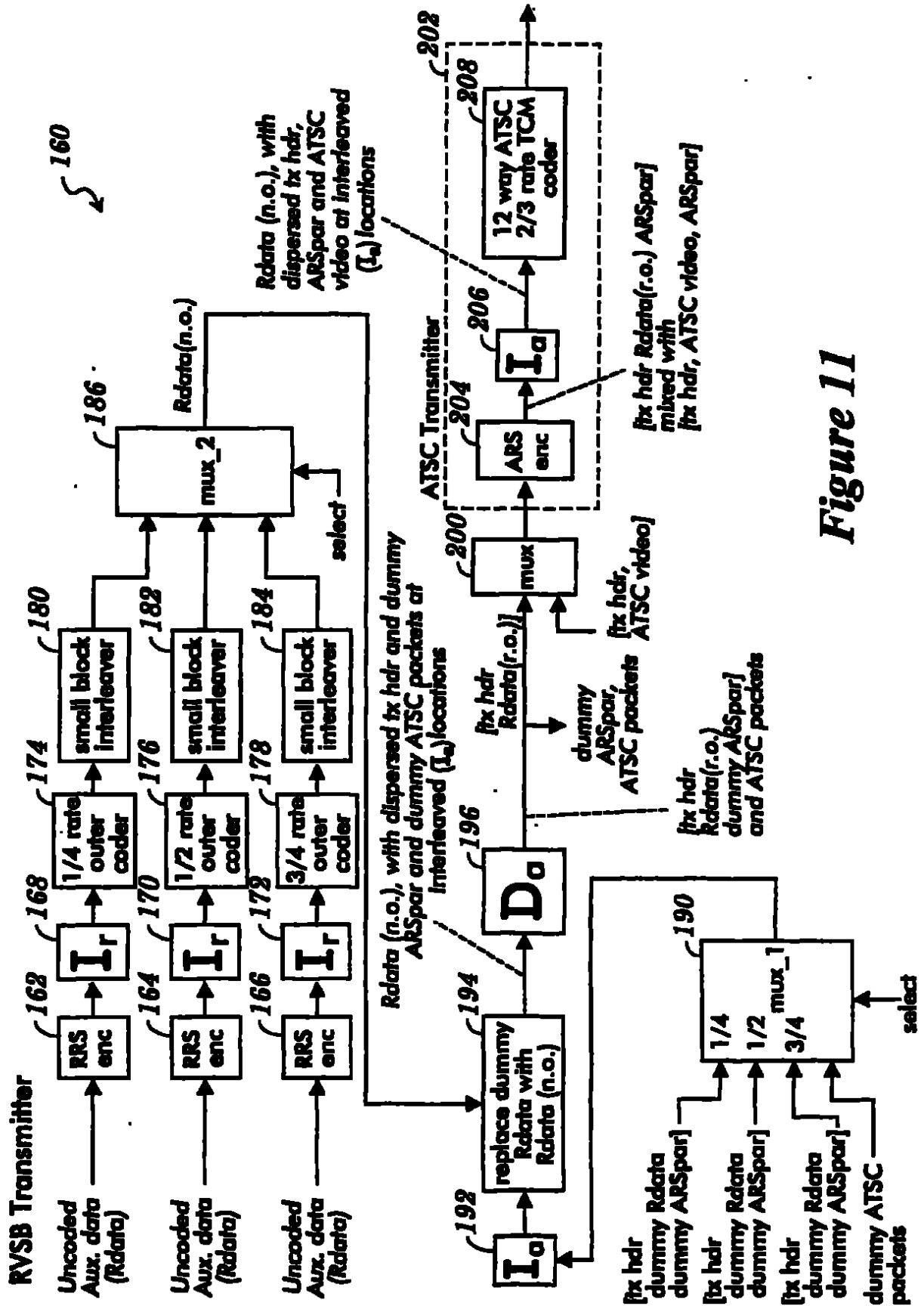


Figure 11

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for 1/2 rate outer code

ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 92 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (576 symbols) 72 bytes payload	RRS parity (160 symbols) 20 bytes	ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 92 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (576 symbols) 72 bytes payload	RRS parity (160 symbols) 20 bytes	ARS parity (80 symbols)
2 bits/symbol	1 bit/symbol		2 bits/symbol

Figure 12

for 1/4 rate outer code

ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 46 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 46 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 46 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (416 symbols) 26 bytes payload	RRS parity (320 symbols) 20 bytes	ARS parity (80 symbols)
2 bits/symbol	0.5 bit/symbol		2 bits/symbol

Figure 13

for 3/4 rate outer code

ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 138 bytes payload		ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 26 bytes payload	20 bytes RRS parity 92 bytes payload	ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 72 bytes payload	20 bytes RRS parity 46 bytes payload	ARS parity (80 symbols)
ATSC tx hdr (12 symbols)	RVSB data (736 symbols) 118 bytes payload	20 bytes RRS parity	ARS parity (80 symbols)
2 bits/symbol	1.5 bit/symbol		2 bits/symbol

Figure 14

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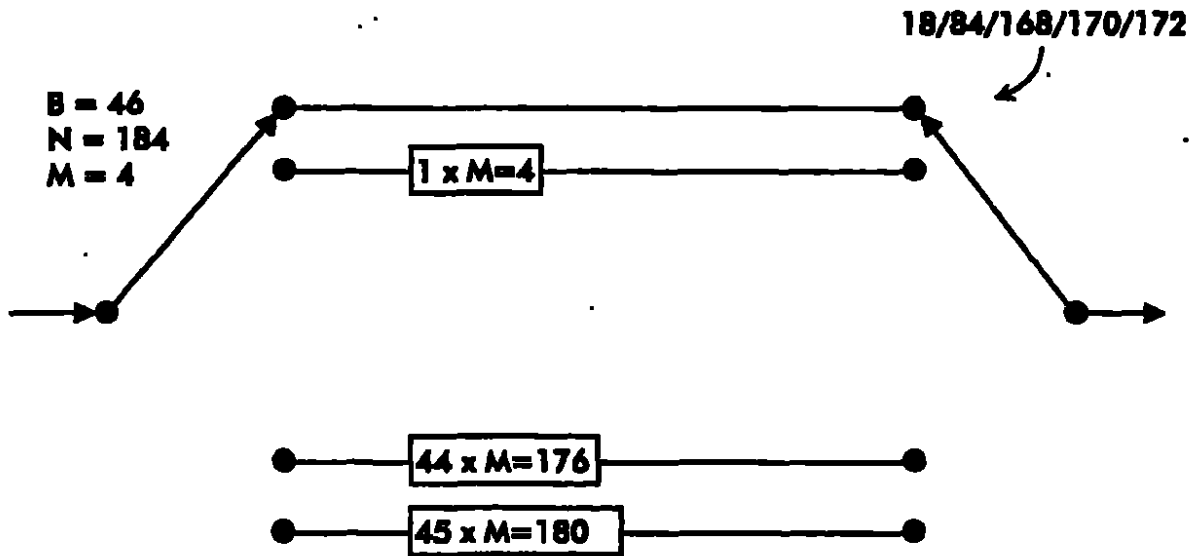


Figure 15

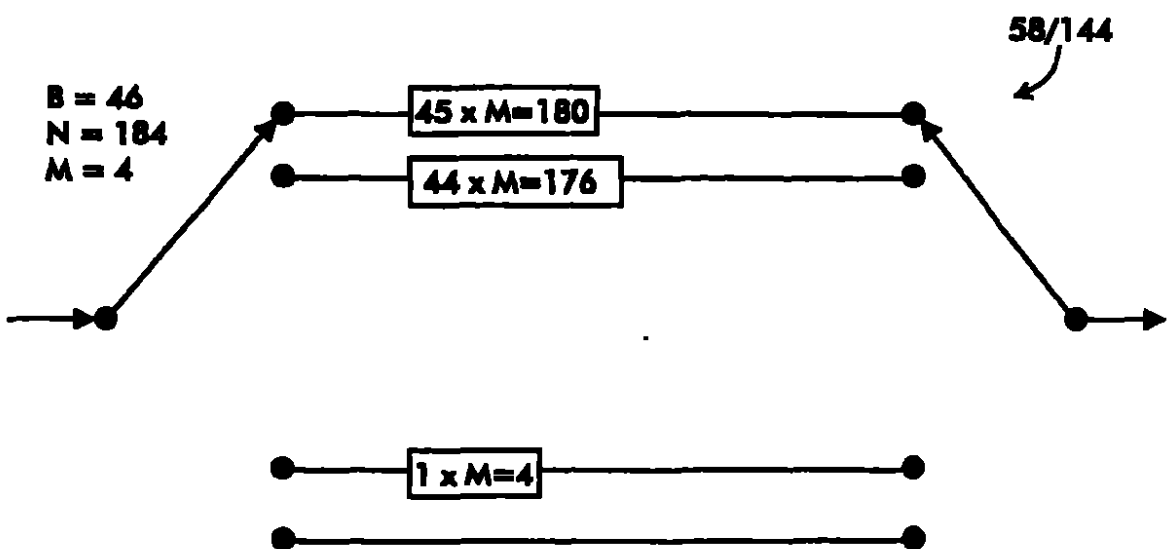


Figure 16

First RVSB RS block of field

RVSB map data (24 bits)	1288 bits
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Figure 17

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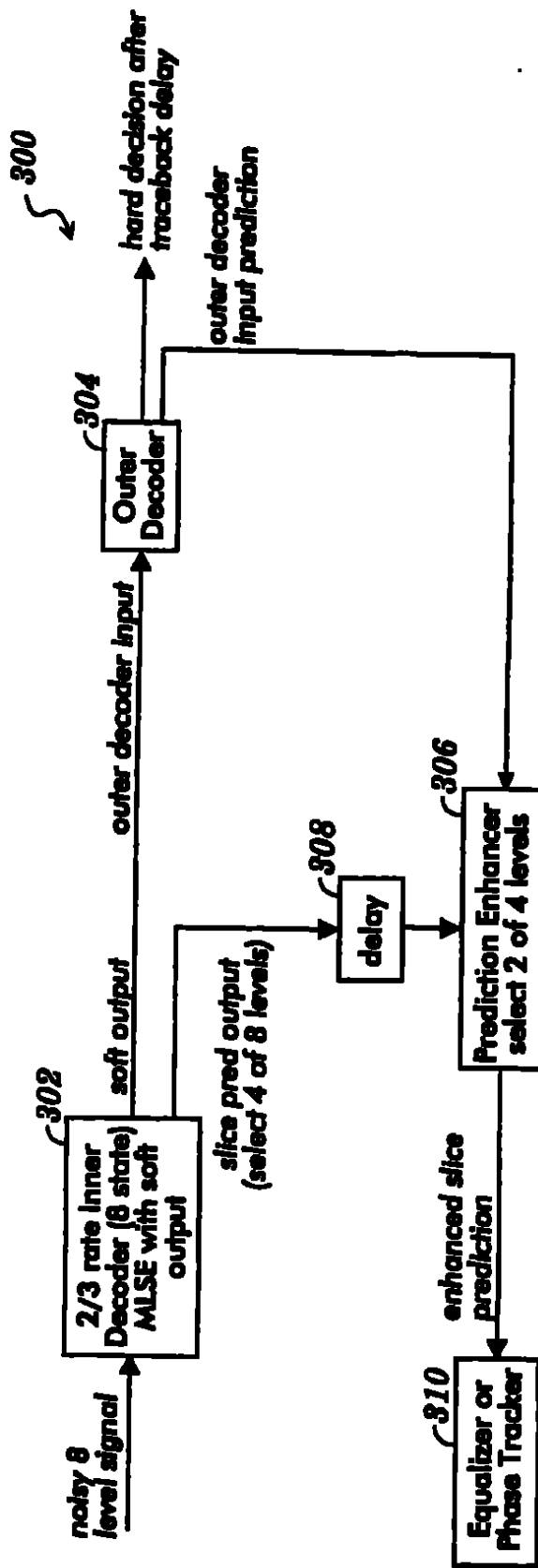
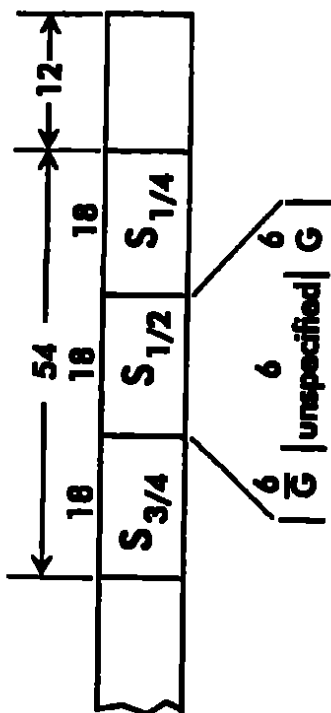




Figure 20

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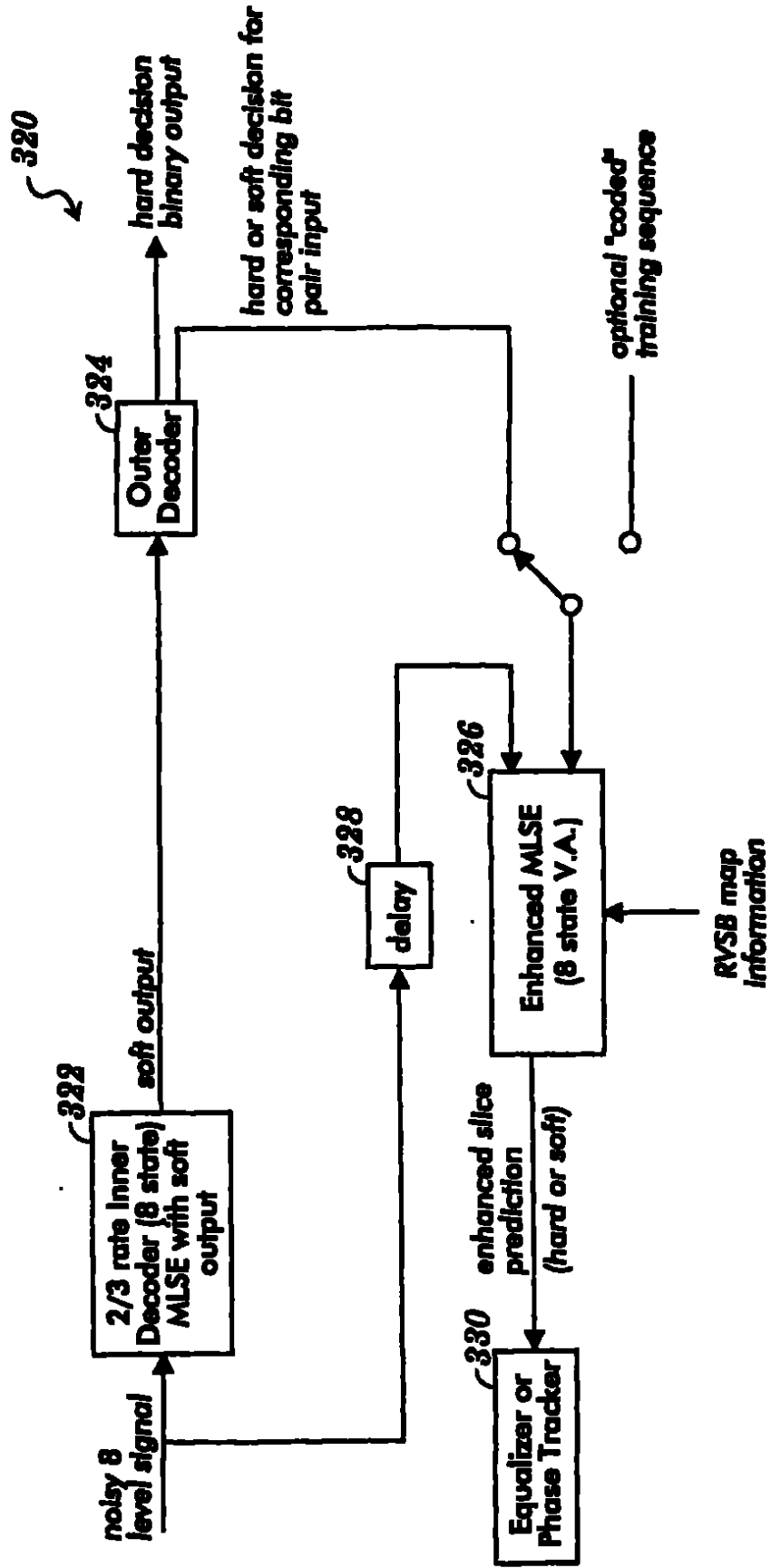


Figure 22

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US005923711A

United States Patent [19]
Willming

[11] **Patent Number:** **5,923,711**
[45] **Date of Patent:** **Jul. 13, 1999**

[54] **SLICE PREDICTOR FOR A SIGNAL RECEIVER**
[75] **Inventor:** David A. Willming, Palatine, Ill.
[73] **Assignee:** Zenith Electronics Corporation, Glenview, Ill.

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Primary Examiner—Chi H. Pham
Assistant Examiner—Khai Tran

[21] **Appl. No.:** 08/627,826
[22] **Filed:** Apr. 2, 1996
[51] **Int. Cl.^o** H04L 25/34; H04L 25/06
[52] **U.S. Cl.** 375/287; 375/317; 375/286
[58] **Field of Search** 375/286, 287, 375/261, 262, 264, 241, 317, 247, 302, 320, 341

[57] **ABSTRACT**

The disclosed data processor develops a data signal which has a plurality of multi-level symbols. The data processor, in response to each of the symbols, determines the lowest path metric characterizing the data signal, and selects one of a plurality of sets of slice values in response to the lowest path metric. A slicer responds to the selected set of slice values by slicing the multi-level symbols. There may be only two sets of slice values in the plurality of sets of slice values, wherein each of the only two sets has three slice levels. Alternatively, there may be only five sets of slice values in the plurality of sets of slice values, wherein each of the only five sets has five slice levels. As a still further alternative, there may be only two sets of slice values in the plurality of sets of slice values, wherein each of the only two sets has a minimum of six slice levels.

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38 Claims, 7 Drawing Sheets

A	B	C	D	E	F	G
Relative Amplitude	Symbol Levels	Z ₁ Z ₂ Z ₃	Symbol Subset	Slice Levels	Slice Levels a/c	Slice Levels b/d
-7	—	000	d	000	001	000
-5	—	001	c	001	010	010
-3	—	010	b	010	011	011
-1	—	011	a	011	100	100
+1	—	100	d	100	101	101
+3	—	101	c	101	110	110
+5	—	110	b	110	111	111
+7	—	111	a	111		

Q ₁ Q ₀	Y ₁ Y ₀	Z ₁ Z ₂ Z ₃	S	R	Q ₁ Q ₀
(n)	(n)	(n)	(n)	(n)	(n+1)
00	00	000	d	-7	00
00	01	010	b	-3	01
00	10	100	d	+1	00
00	11	110	b	+5	01
01	00	001	c	-5	10
01	01	011	a	-1	11
01	10	101	c	+3	10
01	11	111	a	+7	11
10	00	000	d	-7	01
10	01	010	b	-3	00
10	10	100	d	+1	01
10	11	110	b	+5	00
11	00	001	c	-5	11
11	01	011	a	-1	10
11	10	101	c	+3	11
11	11	111	a	+7	10

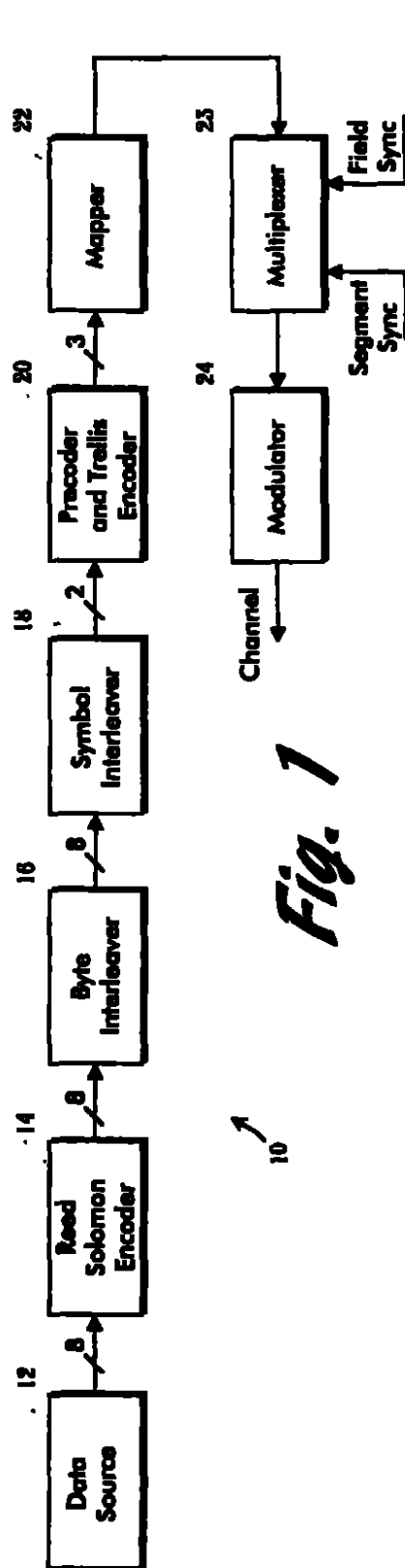


Fig. 1

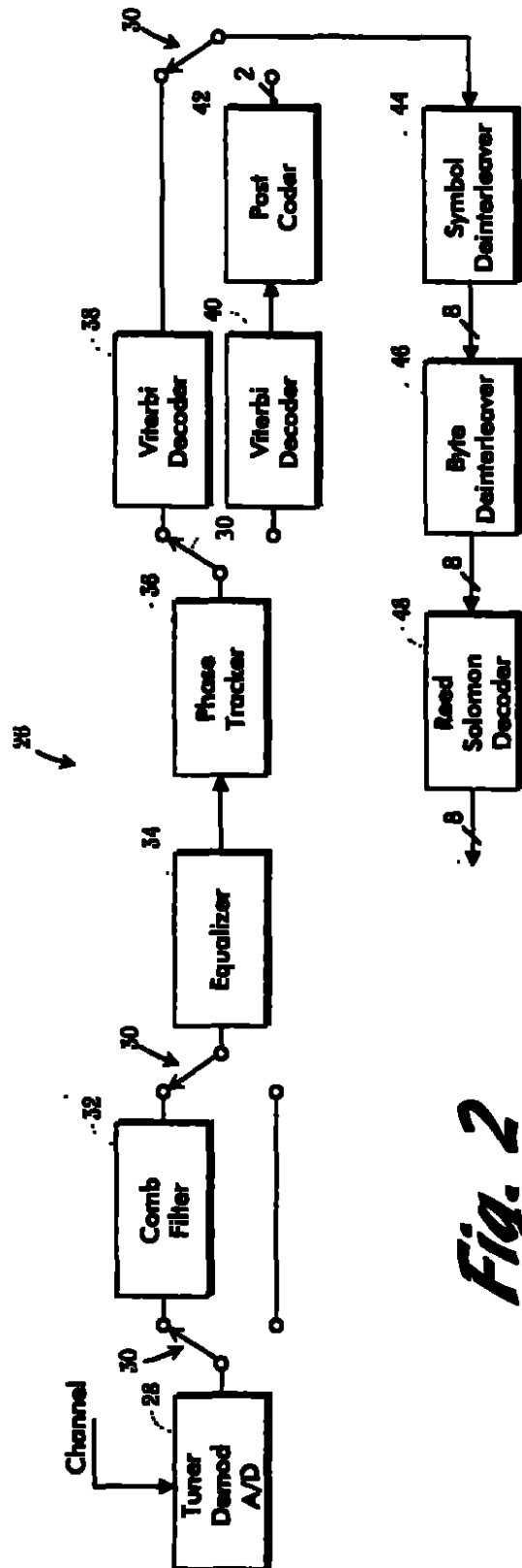


Fig. 2

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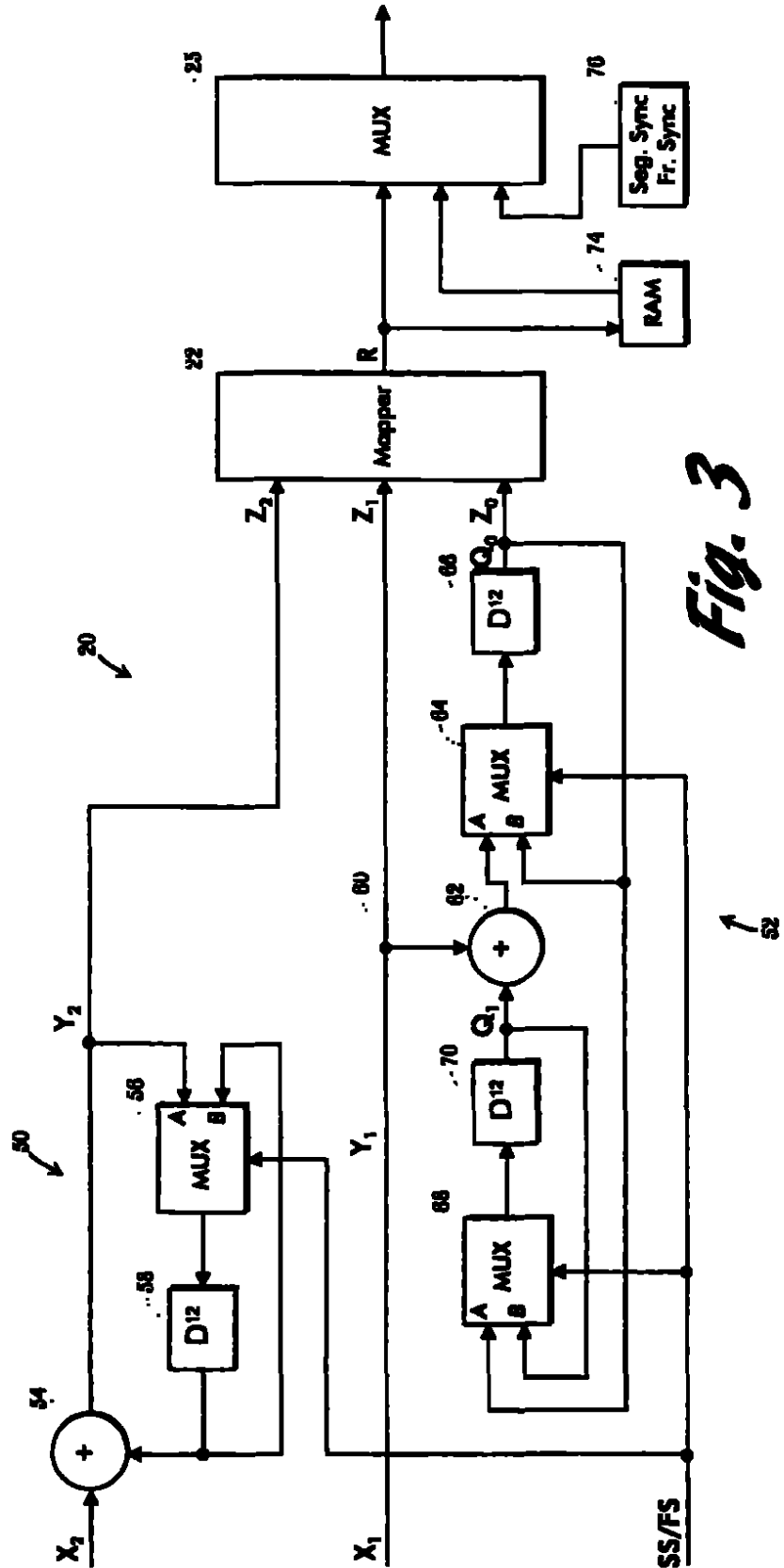


Fig. 3

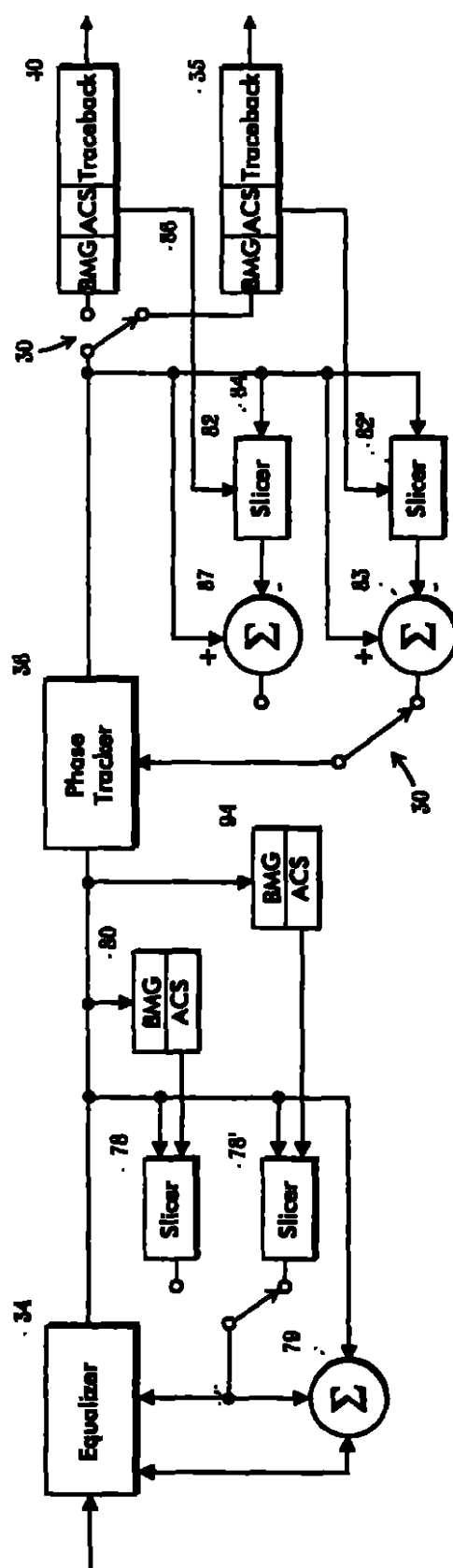


Fig. 4

Q_1Q_0 (n)	Y_1Y_0 (n)	$Z_1Z_0Z_0$ (n)	S (n)	R (n)	Q_1Q_0 (n+1)
00	00	000	d	-7	00
00	01	010	b	-3	01
00	10	100	d	+1	00
00	11	110	b	+5	01
01	00	001	c	-5	10
01	01	011	a	-1	11
01	10	101	c	+3	10
01	11	111	a	+7	11
10	00	000	d	-7	01
10	01	010	b	-3	00
10	10	100	d	+1	01
10	11	110	b	+5	00
11	00	001	c	-5	11
11	01	011	a	-1	10
11	10	101	c	+3	11
11	11	111	a	+7	10

Fig. 6

A Relative Amplitude	B Symbol Levels	C $Z_1Z_0Z_0$	D Symbol Subset	E Slice Levels	F Slice Levels a/c	G Slice Levels b/d
-7	—	000	d	000	001	000
-5	—	001	c	001	010	010
-3	—	010	b	010	011	100
-1	—	011	a	011	101	110
+1	—	100	d	100	111	
+3	—	101	c	101		
+5	—	110	b	110		
+7	—	111	a	111		

Fig. 5

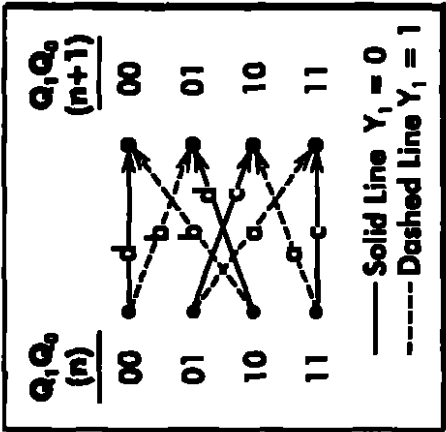


Fig. 7

A	B1	B2	C1	C2	D1	D2
+14○B	+14○B	+14●B	+14○B	+14○B	+14○B	+14○B
+12○C	+12○C	+12○C	+12○C	+12●C	+12○C	+12○C
+10○D	+10○D	+10○D	+10○D	+10○D	+10○D	+10●D
+8●A	+8○A	+8○A	+8○A	+8○A	+8○A	+8○A
+6○B	+6●B	+6●B	+6○B	+6○B	+6○B	+6○B
+4○C	+4○C	+4○C	+4●C	+4●C	+4○C	+4○C
+2○D	+2○D	+2○D	+2○D	+2○D	+2●D	+2●D
0●A	0○A	0○A	0○A	0○A	0○A	0○A
-2○B	-2●B	-2●B	-2○B	-2○B	-2○B	-2○B
-4○C	-4○C	-4○C	-4●C	-4●C	-4○C	-4○C
-6○D	-6○D	-6○D	-6○D	-6○D	-6●D	-6●D
-8●A	-8○A	-8○A	-8○A	-8○A	-8○A	-8○A
-10○B	-10●B	-10○B	-10○B	-10○B	-10○B	-10○B
-12○C	-12○C	-12○C	-12●C	-12○C	-12○C	-12○C
-14○D	-14○D	-14○D	-14○D	-14○D	-14 D	-14○D

Fig. 8

A&C1&C2	B1&B2&D1&D2
+14○B	+14●B
+12○C	+12○C
+10○D	+10●D
+8●A	+8○A
+6○B	+6●B
+4●C	+4○C
+2○D	+2●D
0⊕A	0⊕A
-2○B	-2●B
-4●C	-4○C
-6○D	-6●D
-8●A	-8○A
-10○B	-10●B
-12●C	-12○C
-14○D	-14●D

Fig. 10

A&C2	A&C1	B2&D2	B1&D2	B1&D1
+14○B	+14○B	+14●B	+14○B	+14○B
+12○C	+12○C	+12○C	+12○C	+12○C
+10○D	+10○D	+10●D	+10○D	+10○D
+8●A	+8●A	+8○A	+8○A	+8○A
+6○B	+6○B	+6●B	+6●B	+6●B
+4●C	+4●C	+4○C	+4○C	+4○C
+2○D	+2○D	+2●D	+2●D	+2●D
0⊕A	0⊕A	0⊕A	0⊕A	0⊕A
-2○B	-2○B	-2●B	-2●B	-2●B
-4●C	-4●C	-4○C	-4○C	-4○C
-6○D	-6○D	-6●D	-6●D	-6●D
-8●A	-8●A	-8○A	-8○A	-8○A
-10○B	-10○B	-10●B	-10●B	-10●B
-12○C	-12○C	-12○C	-12○C	-12○C
-14○D	-14○D	-14○D	-14○D	-14○D

Fig. 9

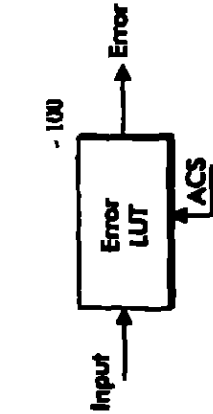


Fig. 13

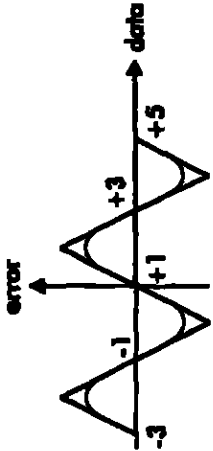


Fig. 12

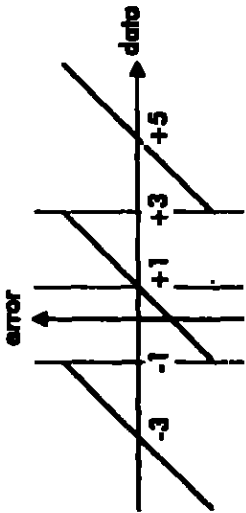


Fig. 11

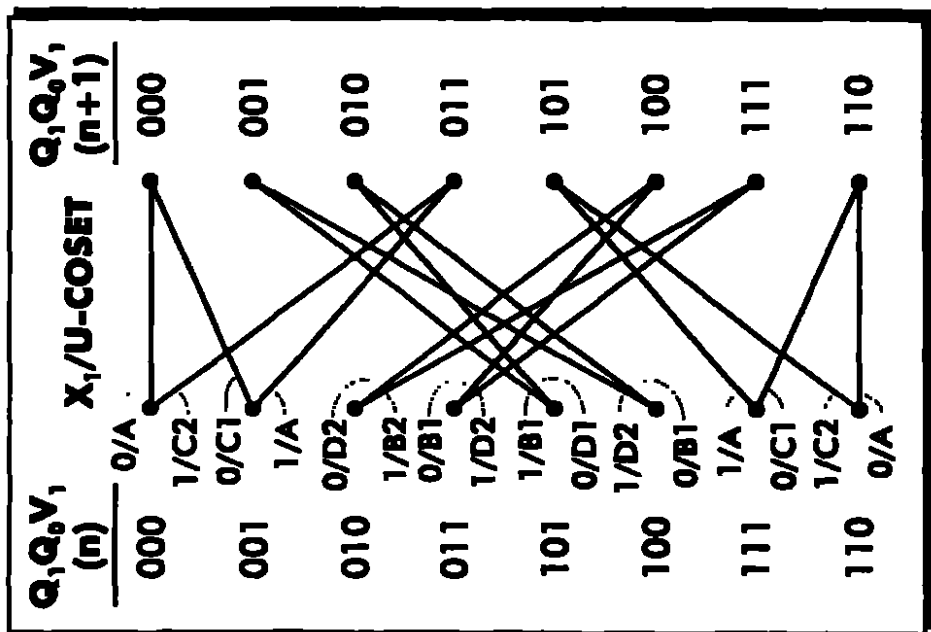


Fig. 14

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1 SLICE PREDICTOR FOR A SIGNAL RECEIVER

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a slicing arrangement for slicing multi-level signals which are transmitted and received in a data transmission and reception system.

BACKGROUND OF THE INVENTION

Multi-level modulation, such as the modulation produced by trellis encoders, is a well-known technique for improving the performance of a data transmission and reception system. For example, multi-level modulation results in an improvement in the signal-to-noise (S/N) performance of the data transmission and reception system at a given power level. Alternatively, multi-level modulation permits the transmitted power level required to achieve a given signal-to-noise performance to be reduced.

In essence, trellis-coded modulation (TCM) comprises the use of a multi-state convolution encoder to convert each k input data bits of an input sequence of data bits into $k+n$ output data bits, and is therefore referred to as a rate $k/(k+n)$ convolution encoder. The output bits are then mapped into a sequence of discrete multi-level symbols of a modulated carrier for data transmission. Each multi-level symbol typically has one of $2^{(k+n)}$ values. These values can be phase and/or amplitude values. By coding the input data bits in a state-dependent sequential manner, increased minimum Euclidean distances between the allowable transmitted sequences may be achieved leading to a reduced error probability where a maximum likelihood decoder (for example, a Viterbi decoder) is used in the receiver.

In an example of a data transmission and reception system which uses multi-level modulation, successive pairs of data bits X_1, X_2 are encoded for transmission as eight-level, one-dimensional symbols. More specifically, bit X_1 is convolutionally encoded using a four-state convolution encoder to generate bits Z_0, Z_1 , and bit X_2 is precoded to generate bit Z_2 . Bits Z_2, Z_1 , and Z_0 are mapped to respective eight-level symbols using a one-dimensional symbol constellation. As an example, $2^{(k+n)}$ amplitude values of $-7, -5, -3, -1, +1, +3, +5$, and $+7$ may be used for the one-dimensional symbol constellation. The eight-level symbols, after insertion of appropriate sync signals, are transmitted in the form of a suppressed carrier vestigial sideband (VSB) signal.

This signal is received by a receiver which, at the front end, may include a tuner, an IF demodulator, an analog-to-digital (A/D) converter, a channel equalizer, and a decoder. The decoder decodes the multi-level symbols in order to recover the successive pairs of data bits X_1, X_2 . The receiver may also include a phase tracker to reduce phase noise errors and amplitude-related errors. That is, many signal receivers, such as television receivers, which are used in data transmission and reception systems and which are designed for receiving suppressed carrier VSB signals, use a double conversion tuner at the receiver front end. The first local oscillator of such a tuner typically exhibits a relatively high level of phase noise in the demodulated data. In addition, the demodulated data may be degraded by amplitude-related errors resulting in the demodulated data being recovered with undesired offsets and/or at undesired levels of gain. These phase noise errors and amplitude-related errors may lead to an unacceptable error rate if uncorrected, especially in the case of tightly packed data constellations. In order to minimize the error rate due to phase noise errors and amplitude-related errors, the multi-level symbols may be

processed by a phase tracker. An example of such a phase tracker is disclosed in U.S. Pat. No. 5,406,587.

Circuits, such as equalizers and phase trackers, usually compute a sliced data signal from a continuous valued signal. The conventional slicer slices the eight-level symbols in accordance with a set of seven slice levels to produce one of eight quantized output values. While this approach to slicing is perfectly satisfactory in theory, performance of the conventional slicer is usually degraded under noisy conditions which cause the amplitude of a multi-level symbol level to cross a slice level solely due to noise acquired during transmission and reception.

For example, the amplitude of a symbol originally having a value of $+5$ (using the $-7, -5, -3, -1, +1, +3, +5, +7$ constellation described above) may be degraded by noise such that its value at the output of the phase tracker may be $+6.1$. Accordingly, a slicing system, which slices the received signal at $-6, -4, -2, 0, +2, +4$, and $+6$ will produce an incorrect quantized value of $+7$ rather than the proper quantized value of $+5$ for use by the phase tracker.

The present invention solves one or more of the above described problems.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a data processor comprises a receiving means, a selecting means, and a slicing means. The receiving means receives a plurality of multi-level symbols. The selecting means selects one of a plurality of sets of slice values, wherein each set of slice values has a minimum of three slice values. The slicing means slices the multi-level symbols in response to the selected set of slice values.

In accordance with another aspect of the present invention, a data processor comprises a receiving means, a selecting means, and a slicing means. The receiving means receives a plurality of multi-level symbols. The selecting means selects one of only two sets of slice values, wherein each of the only two sets of slice values has a plurality of slice values. The slicing means slices the multi-level symbols in response to the selected set of slice values.

In accordance with yet another aspect of the present invention, a data processor comprises a receiving means, a selecting means, and a slicing means. The receiving means receives a plurality of multi-level symbols. The selecting means selects one of only five sets of slice values, wherein each of the only five sets of slice values has a plurality of slice values. The slicing means slices the multi-level symbols in response to the selected set of slice values.

In accordance with a further aspect of the present invention, a data processor comprises a developing means, a determining means, a selecting means, and a slicing means. The developing means develops a data signal including a plurality of multi-level symbols. The determining means is responsive to each of the multi-level symbols in order to determine a lowest path metric characterizing the data signal. The selecting means selects one of a plurality of sets of slice values in response to the lowest path metric. The slicing means slices the multi-level symbols in response to the selected set of slice values.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention will become more apparent from a detailed consideration of the invention when taken in conjunction with the drawings in which:

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FIG. 1 is a block diagram of a transmitter which is useful in a multi-level symbol data transmission and reception system and which includes a precoder and trellis encoder;

FIG. 2 is a block diagram of a receiver which is useful in a multi-level symbol data transmission and reception system and which includes a channel equalizer and a phase tracker;

FIG. 3 is a block diagram illustrating the precoder and trellis encoder of FIG. 1;

FIG. 4 is a slicing arrangement which implements the present invention and which is useful with the channel equalizer and the phase tracker of FIG. 2;

FIG. 5 illustrates two sets of slice levels for the slicer shown in FIG. 4 in the case where a comb filter is not used in the receiver of a multi-level symbol data transmission and reception system;

FIG. 6 is a state table illustrating the operation of the trellis encoding process;

FIG. 7 is a trellis diagram for the trellis encoder of FIG. 3 and is based upon FIG. 6;

FIG. 8 illustrates seven unique co-sets which characterize the output of a comb filter when used in conjunction with a multi-level symbol data transmission and reception system;

FIG. 9 illustrates five sets of slice values for the slicer shown in FIG. 4 in the case where a comb filter is used in the receiver of a multi-level symbol data transmission and reception system;

FIG. 10 illustrates an alternative two sets of slice values for the slicer shown in FIG. 4 in the case where a comb filter is used in the receiver of a multi-level symbol data transmission and reception system;

FIGS. 11-13 illustrate a refinement of the present invention; and,

FIG. 14 is a trellis diagram similar to the trellis diagram illustrated in FIG. 7 but for the case where a trellis encoder and a comb filter are used in combination.

DETAILED DESCRIPTION

FIGS. 1 and 2 generally illustrate a multi-level symbol data transmission and reception system as applied to a multi-level VSB high definition television (HDTV) transmission and reception system of the type disclosed in U.S. Pat. No. 5,087,975 and in copending patent application Ser. No. 08/272,181, filed on Jul. 8, 1994, the disclosures of which are incorporated herein by reference. However, while the multi-level VSB HDTV application is contemplated in the preferred embodiment of the present invention, it will be understood that the present invention is more general in nature and, thus, may be applied to other types of transmission and reception systems, including lower resolution video systems as well as non-video based data systems.

Accordingly, as shown in FIG. 1, a transmitter 10 of a multi-level symbol data transmission and reception system includes a data source 12 which provides a succession of data bytes and a plurality of timing signals. The data bytes, for example, may include eight bits per byte and may comprise a compressed HDTV signal, a compressed television signal of NTSC resolution, or any other data signal.

The data bytes are preferably, although not necessarily, arranged in successive fields. Each field includes a field segment and 312 field sync and data segments, and each field sync and data segment comprises 828 eight-level symbols and four two-level data segment sync symbols occurring at a symbol rate of about 10.76 Msymbols/sec. The data bytes from the data source 12 are applied to a Reed

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Solomon encoder 14 for forward error correction coding, and then to a byte interleaver 16. The byte interleaver 16 reorders the data bytes throughout a frame to reduce the susceptibility of the multi-level symbol data transmission and reception system to burst noise.

The interleaved data bytes from the byte interleaver 16 are applied to a symbol interleaver 18 which provides, for example, two output bit streams X_1 and X_2 at the symbol rate. As disclosed, each bit pair X_1 , X_2 is converted to a corresponding multi-level symbol. In particular, due to the presence of a comb filter in the receiver (to be described in more detail hereinafter), it is desirable to interleave the bit pairs X_1 , X_2 of each data segment among twelve subsegments. Therefore, each subsegment comprises, for example, 69 symbols. This symbol interleaving is discussed in more detail in the aforementioned 181 application.

The stream of bit pairs X_1 , X_2 from the symbol interleaver 18 is coupled to a precoder and trellis encoder 20 for conversion to three output bits as described in further detail hereinafter. Because the precoder and trellis encoder 20 is characterized by a twelve-symbol delay, the precoder and trellis encoder 20 may be envisioned as comprising twelve parallel encoders each operating at 1/12 of the symbol clock rate such that each subsegment generated by the symbol interleaver 18 is processed by a respective one of twelve parallel encoders. The stream of three-bit output bits developed at the output of the precoder and trellis encoder 20 is applied to a symbol mapper 22 and therefrom to a multiplexer 23. The multiplexer 23 multiplexes the output of the mapper 22 with a field sync symbol and a segment sync symbol. The field sync symbol and the segment sync symbol provide field structure. The symbols mapped by the mapper 22, the field sync symbol, and the segment sync symbol, which are multiplexed by the multiplexer 23, are connected to a VSB modulator 24 for transmission as a plurality of multi-level symbols.

As shown in FIG. 2, a receiver 26 of the multi-level symbol data transmission and reception system receives the signal transmitted by the VSB modulator 24 and includes a tuner, demodulator, and A/D converter 28. The tuner, demodulator, and A/D converter 28 tunes a desired channel, converts the received and tuned signal to an intermediate frequency signal, demodulates the intermediate frequency signal to a baseband analog signal, and converts the baseband analog signal to a digital signal for further processing. This digital signal comprises the stream of multi-bit, multi-level symbols which are transmitted by the transmitter 10, and is applied by a multiple pole switch 30 to first and second signal processing paths.

The first signal processing path comprises a comb filter 32, a channel equalizer 34, a phase tracker 36, and a Viterbi decoder 38. The second signal processing path comprises the channel equalizer 34, the phase tracker 36, a Viterbi decoder 40, and a post coder 42. The output of the Viterbi decoder 38, or the output of the post coder 42, is connected to a symbol deinterleaver 44, a byte deinterleaver 46, and a Reed Solomon decoder 48. The output of the Reed Solomon decoder 48 is further processed by elements of the receiver 26 not shown. The comb filter 32 may comprise a feed forward filter including a linear summer and a twelve-symbol delay element.

The reason for these different first and second signal processing paths is because of the possibility of co-channel interference. That is, as explained in more detail in the previously mentioned '975 patent, the comb filter 32 is operable for reducing NTSC co-channel interference by

subtracting from each received symbol, the symbol received twelve-symbol intervals earlier. Because of the symbol interleaving provided in the transmitter, the comb filter 32 independently operates on each of the twelve subsegments of a data segment for providing successive combed outputs of the form $A_1-A_0, B_1-B_0, \dots, A_{12}-A_1, B_{12}-B_1, \dots, A_{24}-A_{13}, B_{24}-B_{13}, \dots$.

The comb filter 32 is desirable in those regions which may receive both HDTV digital signals and standard NTSC signals. For some period of time, at least some of the same broadcast channels in adjacent or nearby television service areas are likely to be allocated for both NTSC transmissions and HDTV transmissions. This overlapping allocation may result in co-channel interference where HDTV and NTSC transmissions in nearby or adjacent television service areas occur on the same channel. The comb filter 32 is thus intended to reduce NTSC co-channel interference from a received HDTV signal. Accordingly, if the receiver 26 is used in such a service area, the multiple pole switch 30 is operated to process the output from the tuner, demodulator, and A/D converter 28 along the first path which includes the comb filter 32 and the Viterbi decoder 35. If the receiver 26 is not used in such a service area, the output of the tuner, demodulator, and A/D converter 28 may be processed along the second path which bypasses the comb filter 32 and the Viterbi decoder 35 and instead processes the signals using the Viterbi decoder 40 and the post coder 42. The processing along the second path is simpler because the comb filter 32 doubles the complexity of processing the received data signals.

As shown in FIG. 3, the precoder and trellis encoder 20 includes a precoder 50 and a trellis encoder 52. The precoder 50 is a modulo-2, feedback precoder which receives the multi-level symbols (each symbol being identified as bits X_1 and X_2) from the symbol interleaver 18, and develops intermediate bits Y_1, Y_2 . More specifically, the precoder 50 includes a modulo-2 summer 54 having a first input connected to receive the bit X_2 . The output of the modulo-2 summer 54 provides the intermediate bit Y_2 and is connected to a first (A) input of a multiplexer 56 having an output connected to a twelve-symbol delay element 58. The output of the twelve-symbol delay element 58 is connected to a second input of the modulo-2 summer 54 and is also connected to a second (B) input of the multiplexer 56. The intermediate bit Y_2 generated by the precoder 50 is applied as an output bit Z_2 to a first input of the symbol mapper 22. The intermediate bit Y_1 is an uncoded form of the bit X_1 and is supplied to the trellis encoder 52.

The trellis encoder 52 comprises a rate $1/2$, 4-state systematic feedback convolution encoder which converts the intermediate bit Y_1 to the output bits Z_1 and Z_0 . Accordingly, the trellis encoder 52 includes a signal path 60 for applying the intermediate bit Y_1 as the output bit Z_1 directly to a second input of the symbol mapper 22. Also, the trellis encoder 52 includes a modulo-2 summer 62 which receives the intermediate bit Y_1 from the signal path 60 at a first input thereof. The modulo-2 summer 62 has an output connected to a first (A) input of a multiplexer 64, the output of which is connected to a twelve-symbol delay element 66. The output of the twelve-symbol delay element 66 is connected to the symbol mapper 22, to a second (B) input of the multiplexer 64, and to a first (A) input of a multiplexer 68. The twelve-symbol delay element 66 produces a state bit Q_0 , which is used to define a state of the trellis encoder 52 at a particular time and which is provided as the output bit Z_0 . The output of the multiplexer 68 is connected to a twelve-symbol delay element 70 and produces a state bit Q_1 , which

is also used to define the state of the trellis encoder 52 at the particular time. The output of the twelve-symbol delay element 70 is connected as a second input to the modulo-2 summer 62 and is fed back to a second (B) input of the multiplexer 68. Because of the twelve-symbol delay elements 58, 66, and 70, each subsegment of a data segment is independently processed by the precoder 50 and the trellis encoder 52. The multiplexers 56, 64, and 68 are provided to allow for sync insertion during which times their respective second (B) inputs are selected. At all other times, the first (A) inputs of the multiplexers 56, 64, and 68 are selected.

The output bits Z_2, Z_1 , and Z_0 are supplied to the symbol mapper 22. The symbol mapper 22 maps these three output bits to a corresponding one of eight signal levels to form a multi-level symbol. These eight signal levels are shown in Columns A and B of FIG. 5. Column C of FIG. 5 shows the various combinations of the output bits Z_2, Z_1, Z_0 . For example, if $Z_2=0, Z_1=1$, and $Z_0=1$, the mapper 22 maps output bits Z_2, Z_1 , and Z_0 to a multi-level symbol of -1. As can be seen from FIG. 5, the eight-level symbols developed at the output of the symbol mapper 22 are symmetrical about the zero level. To facilitate signal acquisition by the receiver 26, it is preferable to offset each symbol by a given amount (for example, +1 unit) in order to provide a pilot component. The multi-level symbols, and the pilot component if used, are then applied through a first input of a multiplexer 23 to the VSB modulator 24. The VSB modulator 24 modulates the multi-level symbols (and the pilot component) on a selected carrier for transmission in a suppressed carrier VSB form as described in the previously mentioned '975 patent. The output of the symbol mapper 22 is also applied to the input of a RAM 74 whose output is supplied to a second input of the multiplexer 23. A third input of the multiplexer 23 is supplied from a source 76 of segment and frame sync signals.

Also, as shown in FIG. 5, the eight levels of the multi-level symbols are divided into four subsets a, b, c, and d. Each of these four subsets is identified by a particular state of the output bits Z_1, Z_0 . Thus, when the output bits Z_1, Z_0 are in state 00, their state corresponds to subset d; when the output bits Z_1, Z_0 are in state 01, their state corresponds to subset c; when the output bits Z_1, Z_0 are in state 10, their state corresponds to subset b; and, when the output bits Z_1, Z_0 are in state 11, their state corresponds to subset a.

FIG. 4 illustrates a modification of a portion of the receiver 26 shown in FIG. 2 according to the present invention. As illustrated in FIG. 4, the stream of received multi-level symbols (at a rate equal to 10.76 MHz) representing the output bits Z_2, Z_1, Z_0 is provided to the channel equalizer 34. The multi-level symbols are equalized by the channel equalizer 34, and are then processed by the phase tracker 36 to remove undesired phase noise. The phase tracker 36 may be of the type disclosed in the aforementioned '587 patent.

When processing by the comb filter 32 is not necessary, the output of the phase tracker 36 is connected through a pole of the multiple pole switch 30 to the Viterbi decoder 40 to derive an estimation of the original data bits X_1, X_2 . As discussed in the aforementioned 181 application, a Viterbi decoder, such as a Viterbi decoder manufactured by LSI Logic Corp., includes a branch metric generator (BMG) which is responsive to the received multi-level symbols for generating and for applying branch metrics to an add, compare, and select (ACS) unit. The ACS unit is bi-directionally coupled to a path metric storage memory (not shown) and also supplies a traceback memory.

The ACS unit of a Viterbi decoder is responsive to the branch metrics generated by the BMG for generating a

plurality of path metrics for each multi-level symbol. Each path metric corresponds to a selected state of a convolution encoder. The convolutional encoder used in the present invention (i.e., the trellis encoder 52) has four states as shown by the $Q_1Q_0(n)$ column of the state table shown in FIG. 6. Each of these four states is repeated four times because of the four possible states of the intermediate bits Y_1, Y_2 shown in the $Y_2Y_1(n)$ column of FIG. 6. The $Z_2Z_1Z_0(n)$ column is derived from the $Q_1Q_0(n)$ column and the $Y_2Y_1(n)$ column. That is, as shown in FIG. 3, the output bit Z_2 is always equal to the intermediate bit Y_2 , the output bit Z_1 is always equal to the intermediate bit Y_1 , and the output bit Z_0 is always equal to the state bit Q_0 . The subset(n) column shows in which of the four subsets {a, b, c, or d} a point lies. The $R(n)$ column is determined by mapping of the Z_2, Z_1, Z_0 bits to an output data level. The next state $Q_1Q_0(n+1)$ is defined by the combination of the current state $Q_1Q_0(n)$ and the current input bit $Y_1(n)$.

The information in the state table of FIG. 6 may also be represented by the trellis diagram of FIG. 7. As shown therein, the four path metrics maintained by the ACS unit correspond to the four encoder states. As shown in FIGS. 5, 6, and 7, when the encoder is in state 00 or state 10, the symbol output during the current symbol period lies in either subset b or subset d, and when the encoder is in state 01 or state 11, the symbol output during the current symbol period lies in either subset a or subset c. Furthermore, the path metric having the lowest value provides the best estimate of the current state of the encoder. That is, the lowest path metric generated by the ACS unit provides an estimate of the current state of the encoder, and allows a prediction of which subset the following symbol will lie in.

As discussed above, a sliced signal is determined for the channel equalizer 34 based upon its output as shown in FIG. 4, and a sliced signal is determined for the phase tracker 36 based upon its output as shown in FIG. 4. The slicing may be accomplished using a conventional slicer characterized by a single set of seven slice levels for slicing the eight-level symbols. The seven levels are shown in Column E of FIG. 5. Thus, a symbol having a level more positive than +6 would be fed back to the channel equalizer 34 or the phase tracker 36 as the quantized value +7, a symbol having a level between +4 and +6 would be fed back as the quantized value +5, a symbol having a level between +2 and +4 would be fed back as the quantized value +3, a symbol having a level between 0 and +2 would be fed back as the quantized value +1, a symbol having a level between 0 and -2 would be fed back as the quantized value -1, a symbol having a level between -2 and -4 would be fed back as the quantized value -3, a symbol having a level between -4 and -6 would be fed back as the quantized value -5, and a symbol having a level below -6 would be fed back as the quantized value -7.

While this approach is perfectly satisfactory in theory, its performance may be degraded under noisy conditions where the amplitude of the symbol level may cross a slice level solely due to noise acquired during transmission and reception. In the example discussed above, the amplitude of a symbol originally having a value of +5 may be degraded by noise such that its value at the output of the phase tracker 36, or at the output of the channel equalizer 34, is +6.1. Without noise, the +5 symbol is correctly sliced by the conventional slicer to its proper quantized value of +5. However, in the presence of noise, the +5 symbol is improperly sliced by the conventional slicer to an incorrect quantized value of +7.

Accordingly, unlike conventional slicers, the slicers of the present invention store plural sets of slice levels for the

purpose explained below. One of these slicers, a slicer 78 (FIG. 4), is used in conjunction with the channel equalizer 34. The slicer 78 provides an output (through the switch 30) to both the channel equalizer 34 and a negative input of a summer 79, and receives an input not only from the output of the channel equalizer 34, but also from an ACS unit of a partial Viterbi decoder 80. (For example, the channel equalizer 34 may be of the type having a feedback filter and a training algorithm so that the output of the slicer 78 is provided to the feedback filter and the output of the summer 79 is provided to the training algorithm.) The output of the equalizer 34 is also connected to the positive input of the summer 79. Only the ACS unit and the RMG of a Viterbi decoder are required for the partial Viterbi decoder 80. Similarly, instead of a conventional slicer, a slicer 82 is used in conjunction with the phase tracker 36. The slicer 82 has a symbol input 84, which is connected to an output of the phase tracker 36, a set selecting input 86, which is connected to an ACS unit of the Viterbi decoder 40, and an output, which is connected to a negative input of a summer 87. A positive input of the summer 87 is connected to the symbol input 84. The output of the summer 87 is connected through another pole of the multiple pole switch 30 to the phase tracker 36. If the phase tracker 36 is the phase tracker disclosed in the aforementioned '587 patent, the slicer 82 would be incorporated in the mapper 34 disclosed therein. The slicers 78 and 82 are active when the comb filter 32 is not active.

The slicer 82, which is used with the summer 87, with the phase tracker 36, and with the Viterbi decoder 40, stores two sets of three slicing levels. One set of three slicing levels is illustrated in Column F of FIG. 5 and is used by the slicer 82 when the lowest value path metric supplied by the ACS unit of the Viterbi decoder 40 corresponds to an encoder state of 01 or 11. The other set of three slicing levels is illustrated in Column G of FIG. 5 and is used by the slicer 82 when the lowest value path metric supplied by the ACS unit of the Viterbi decoder 40 corresponds to an encoder state of 00 or 10.

In other words, if the lowest value path metric of the ACS unit of the Viterbi decoder 40 corresponds to an encoder state of 01 or 11, it is assumed that the multi-level symbol at the output of the phase tracker 36 belongs to either the subset a or the subset c so that only the three slice levels 88, 90, and 92 in Column F of FIG. 5 need to be used to derive the corresponding quantized level. Thus, if the multi-level symbol at the output of the phase tracker 36 and applied to the slicer 82 is more positive than +5, this multi-level symbol will be quantized to a value of +7. If the multi-level symbol is between +5 and +1, this multi-level symbol will be quantized to a +3. If the multi-level symbol is between +1 and -3, this multi-level symbol will be quantized to value of -1. If the multi-level symbol is more negative than -3, this multi-level symbol will be quantized to a value of -5.

Similarly, if the lowest path metric corresponds to an encoder state of 00 or 10, it is assumed that the multi-level symbol belongs to either subset b or subset d, so that only the three slice levels in Column G of FIG. 5 are used to derive the quantized data level to be supplied by the slicer 82 to the summer 87 as discussed above in connection with Column F. Thus, if the multi-level symbol at the output of the phase tracker 36 and applied to the slicer 82 is more positive than +3, this multi-level symbol will be quantized to a value of +5. If the multi-level symbol is between -1 and +3, this multi-level symbol will be quantized to a +1. If the multi-level symbol is between -5 and -1, this multi-level symbol will be quantized to value of -3. If the multi-level

symbol is more negative than -5, this multi-level symbol will be quantized to a value of -7.

Whether using Column F or Column G, the distance between adjacent slice levels is twice that of the conventional slice levels of Column E, thereby significantly increasing the robustness of the slicing system. In the example discussed above of a nominal +5 level symbol which has been corrupted by noise to a +6.1 level symbol, the symbol will be quantized to a value of +7 instead of its correct value of +5 without the present invention. However, with the present invention, the proper result is produced because the lowest path metric produced by the ACS unit of the Viterbi decoder 40 directs use of the proper slice levels, i.e. the set of slice levels in Column G.

The summer 87 subtracts the quantized value produced by the slicer 82 from the multi-level symbol at the output of the phase tracker 36 in order to generate an error signal which is applied to appropriate elements of the phase tracker 36.

The slicer 78 associated with the equalizer 34 may operate in a manner which is similar to the slicer 82.

The transfer characteristic of the operation of the slicer 82 and the summer 87 is shown in FIG. 11 which illustrates three exemplary slice values of -3, +1, and +5. If the slice value, as dictated by the lowest path metric produced by the ACS unit of the Viterbi decoder 40, and the output of the phase tracker 36 are both +5, for example, a zero error value is generated. If the slice value is +5 and the output of the phase tracker 36 is +5.5, an error value of +0.5 is generated, and so on. If the phase tracker 36 is the phase tracker disclosed in the aforementioned '587 patent, the mapper 34 disclosed in this patent uses this error value to generate its difference.

However, if data (e.g., the output of the phase tracker 36) is close to midway between two slice values (such as at about +3), such data can be incorrectly sliced because there is an uncertainty as to whether the data should be sliced to a value of +1 or +5. Incorrect slicing can result in an error and an attempted correction in the wrong direction. In such circumstances, it may be better to generate a weighted error signal so that small corrections are attempted in the region where the slice decisions are likely to be incorrect rather than possibly correcting in the wrong direction. In order to correctly generate a weighted error signal in these circumstances, the slicer 82 and summer 87 may be combined into a single error look-up table to produce any desired response, such as the response illustrated in FIG. 12. As shown in FIG. 12, an error signal of zero is generated midway between slice values. Error signals at other data values are likewise modified in accordance with the characteristic of FIG. 12.

A preferred technique for implementing the characteristic of FIG. 12 is to use an error LUT 100, as shown in FIG. 13, in place of a slicer and its corresponding summer. The error LUT 100 stores multiple look-up tables in which the active look-up table is selected in response to the lowest path metric produced by the ACS unit of the Viterbi decoder 40. Thus, each value of the input data addresses a memory location in the selected look-up table, and the error stored at that memory location is read out as the corresponding error signal.

The above description of the slicer 82, which operates in conjunction with the Viterbi decoder 40, applies to the case where data processing is performed along the second signal processing path of the receiver 26, i.e. where the comb filter 32 is not used to process data. However, in the case where data processing is performed along the first signal process-

ing path of the receiver 26, i.e. where the comb filter 32 is used to process data, a slicer 82' having a set selecting input connected to the ACS unit of the Viterbi decoder 35 is used instead of the slicer 82. When the multiple pole switch 30 is operated so that data is processed along the first signal processing path, the slicer 82' is active. The output of the slicer 82' is connected to a summer 83, which operates in a manner similar to the summer 87. Similarly, the output of a slicer 78' is connected to a summer similar to the summer 87, and a partial Viterbi decoder 94, similar to the partial Viterbi decoder 80, is used in conjunction with the slicer 78'.

Although the comb filter 32 has the desired effect of reducing NTSC channel interference, the comb filter 32 also increases the complexity of the receiver's Viterbi decoders. That is, an optimum Viterbi decoder must take into account not only the state of the trellis encoder 52, but also the state of the delay element of the comb filter 32. Because there are four encoder states for the trellis encoder 52, and four possible states of the delay element of the comb filter 32, an optimum Viterbi decoder must process a sixteen-state trellis. The aforementioned 181 application illustrates a technique for reducing the complexity of a Viterbi decoder which is to be used in conjunction with a comb filter. Such a reduced complexity Viterbi decoder may be used for the Viterbi decoder 35 and the partial Viterbi decoder 94.

Each of the BMGs of the Viterbi decoder 38 and the partial Viterbi decoder 94 generate seven branch metrics. Each of the seven branch metrics represents the squared Euclidean distance between the symbol level at the output of the comb filter 32 and the nearest one of three values of each of seven co-sets A, B1, B2, C1, C2, D1, and D2. These co-sets, and the three values for each co-set (shown as black dots), are illustrated in FIG. 8 hereof.

These co-sets illustrated in FIG. 8 may be rearranged as shown in FIG. 9 according to the following explanation. When the trellis encoder 52 is in a particular state, its output can lie in only two of the four subsets as illustrated in FIG. 7. For example, when the trellis encoder 52 lies in state 00, the next symbol must reside in either the subset b or d. The current estimate of the state of the trellis encoder 52 of the Viterbi decoder 40 can be used to predict in which of these two subsets the next symbol can lie. Hence, the slicer 82 can quantize the signal to one of four amplitudes that make up subset b and/or subset d.

A similar procedure occurs when the comb filter 32 is active. It can be shown from FIG. 14 that, when the combination of the trellis encoder 52 and the comb filter 32 is in a particular state, the output of the comb filter 32 will lie in one of only two of the seven subsets illustrated in FIG. 8. (FIG. 14 is reproduced from the aforementioned 181 application and is a trellis diagram for the case where the comb filter 32 is active.) Thus, (i) when the combined state of the trellis encoder 52 and the comb filter 32 is state 0, the next symbol must lie in either subset A or subset C2, (ii) when the combined state of the trellis encoder 52 and the comb filter 32 is state 1, the next symbol must lie in either subset A or subset C1, (iii) when the combined state of the trellis encoder 52 and the comb filter 32 is state 2, the next symbol must lie in either subset B2 or subset D2, (iv) when the combined state of the trellis encoder 52 and the comb filter 32 is state 3, the next symbol must lie in either subset B1 or subset D2, (v) when the combined state of the trellis encoder 52 and the comb filter 32 is state 4, the next symbol must lie in either subset B1 or subset D1, (vi) when the combined state of the trellis encoder 52 and the comb filter 32 is state 5, the next symbol must lie in either subset B1 or subset D2, (vii) when the combined state of the trellis

encoder 52 and the comb filter 32 is state 6, the next symbol must lie in either subset A or subset C1, and (viii) when the combined state of the trellis encoder 52 and the comb filter 32 is state 7, the next symbol must lie in either subset A or subset C2.

It is noted that the output co-sets (A and C2) of transitions (i) and (viii) are the same, that the output co-sets of transitions (ii) and (vii) are the same, and that the output co-sets of transitions (iv) and (vi) are the same. Consequently, these seven co-sets may be rearranged into five groups of two co-sets each such that, for a particular state of the trellis encoder 20/comb filter 32 combination, the output of the comb filter 32 must lie within one of these five groups. The state of the trellis encoder 52 and the comb filter 32 as estimated by the Viterbi decoder 35 can be used to predict in which of these five groups the next symbol can lie.

These five groups are shown in FIG. 9. Each group has five slice levels. The five slice levels of the group A and C2 is shown in FIG. 9. Similarly, the group A and C1 has slice levels at +6, +2, -2, -6, and -10, the group B2 and D2 has slice levels at +12, +8, +4, 0, and -4, the group B1 and D2 has slice levels at +8, +4, 0, -4, and -8, and the group B1 and D1 has slice levels at +4, 0, -4, -8, and -12. Accordingly, the lowest path metric produced by the ACS unit of the Viterbi decoder 35 selects the slice levels of one of the five groups illustrated in FIG. 9. The selected set of slice levels is then used by the slicer 82' for slicing the output of the phase tracker 36 to produce a quantized value for supply to the summer 83 or by the slicer 78' for slicing the output of the equalizer 34.

The five sets of slice levels shown in FIG. 9 can be reorganized into two sets of slice values as shown in FIG. 10. These two sets of slice levels shown in FIG. 10 are somewhat less robust than the five sets illustrated in FIG. 9, but these two sets result in a less complicated selection process. The first set of slice values, A, C1, and C2, has six slice levels, and the second set of slice values, B1, B2, D1, and D2, has seven slice levels. The slicers 78' and 82' store the seven groups of slice levels shown in FIG. 8, the five groups of slice levels shown in FIG. 9, or the two groups of slice levels shown in FIG. 10, as appropriate.

With these stored slice levels, the slicer 82' then responds to the lowest path metric from the ACS unit of the Viterbi decoder 35 in the same manner as the slicer 82 responds to the ACS unit of the Viterbi decoder 40, and the slicer 78' responds to the lowest path metric from the ACS unit of the partial Viterbi decoder 94 in the same manner as the slicer 82 responds to the ACS unit of the Viterbi decoder 40. Similarly, the slicer 78 responds to the lowest path metric from the ACS unit of the partial Viterbi 80 in the same manner as the slicer 82 responds to the ACS unit of the Viterbi decoder 40.

Certain modifications of the present invention have been discussed above. Other modifications will occur to those practicing in the art of the present invention. The trellis encoder 52, for instance, may take various other forms than that shown in FIG. 3 without departing from the invention. For example, the number of encoder states may differ from that shown, feedforward architectures may be used rather than the disclosed feedback structure, and non-systematic coding may be employed in either a feedback or a feedforward arrangement.

Also, modulation and demodulation techniques other than VSB, such as those employing, for example, quadrature amplitude modulation (QAM) and demodulation, may be employed.

Additionally, the present invention has been described in connection with eight-level symbols, although it should be understood that the present invention may be used with symbols having any number of levels.

Accordingly, the description of the present invention is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention. The details may be varied substantially without departing from the spirit of the invention, and the exclusive use of all modifications which are within the scope of the appended claims is reserved.

What is claimed is:

1. A data processor comprising:
 - receiving means for receiving a plurality of multi-level symbols;
 - selecting means for selecting one of a plurality of sets of slice values based upon the multi-level symbols, wherein each set of slice values has a minimum of three slice values; and,
 - slicing means responsive to the selected set of slice values for slicing and decoding the multi-level symbols.
2. The data processor of claim 1 wherein each of the sets of slice values has a number of slice values, wherein the multi-level symbols are characterized by a number of values, and wherein the number of slice values of each of the sets of slice values is less than one-half of the number of values characterizing the multi-level symbols.
3. The data processor of claim 1 wherein adjacent slice values of each of the sets of slice values are spaced apart from each other, and wherein the slice values of one of the sets of slice values are offset from the slice values of another one of the sets of slice values.
4. The data processor of claim 1 wherein adjacent slice values of each of the sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the sets of slice values are offset by a substantially equal amount from the corresponding slice values of another one of the sets of slice values.
5. The data processor of claim 1 wherein the selecting means comprises means for selecting one of only two sets of slice values, and wherein each of the only two sets of slice values contains only three slice values.
6. The data processor of claim 5 wherein adjacent slice values of each of the only two sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only two sets of slice values are offset by a substantially equal amount from the corresponding slice values of the other of the only two sets of slice values.
7. The data processor of claim 6 wherein the plurality of multi-level symbols comprises a plurality of eight-level symbols, and wherein the selecting means comprises means responsive to each multi-level symbol for calculating four path metrics.
8. The data processor of claim 1 wherein the selecting means comprises means for selecting one of only two sets of slice values, and wherein each of the only two sets of slice values contains a minimum of six slice values.
9. The data processor of claim 8 wherein adjacent slice values of each of the only two sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only two sets of slice values are offset by a substantially equal amount from the corresponding slice values of the other of the only two sets of slice values.
10. The data processor of claim 9 wherein the plurality of multi-level symbols comprises a plurality of eight-level

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symbols, and wherein the selecting means comprises means responsive to each multi-level symbol for calculating seven path metrics.

11. The data processor of claim 1 wherein the selecting means comprises means for selecting one of only five sets of slice values, and wherein each of the only five sets of slice values contains a minimum of five slice values.

12. The data processor of claim 11 wherein adjacent slice values of each of the only five sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only five sets of slice values are offset by a substantially equal amount from the corresponding slice values of another one of the only five sets of slice values.

13. The data processor of claim 12 wherein the plurality of multi-level symbols comprises a plurality of eight-level symbols, and wherein the selecting means comprises means responsive to each multi-level symbol for calculating seven path metrics.

14. A data processor comprising:

a receiver, wherein the receiver is arranged to receive a plurality of multi-level symbols;

a selector, wherein the selector is arranged to select one of only two sets of slice values, wherein each of the only two sets of slice values has a plurality of slice values; and,

a slicer, wherein the slicer is responsive to the selected set of slice values and is arranged to slice and decode the multi-level symbols.

15. The data processor of claim 14 wherein each of the only two sets of slice values has a number of slice values, wherein the multi-level symbols are characterized by a number of values, and wherein the number of slice values of each of the only two sets of slice values is less than one-half of the number of values characterizing the multi-level symbols.

16. The data processor of claim 14 wherein adjacent slice values of each of the only two sets of slice values are spaced apart from each other, and wherein the slice values of one of the only two sets of slice values are offset from the slice values of the other of the only two sets of slice values.

17. The data processor of claim 14 wherein adjacent slice values of each of the only two sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only two sets of slice values are offset by a substantially equal amount from the corresponding slice values of the other of the only two sets of slice values.

18. The data processor of claim 14 wherein each of the only two sets of slice values contains only three slice values.

19. The data processor of claim 18 wherein adjacent slice values of each of the only two sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only two sets of slice values are offset by a substantially equal amount from the corresponding slice values of the other of the only two sets of slice values.

20. The data processor of claim 19 wherein the plurality of multi-level symbols comprises a plurality of eight-level symbols, and wherein the selector is responsive to each multi-level symbol in order to calculate four path metrics.

21. The data processor of claim 14 wherein each of the only two sets of slice values contain a minimum of six slice values.

22. The data processor of claim 21 wherein adjacent slice values of each of the only two sets of slice values are spaced apart from each other by a substantially equal amount, and

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wherein the slice values of one of the only two sets of slice values are offset by a substantially equal amount from the corresponding slice values of the other of the only two sets of slice values.

23. The data processor of claim 22 wherein the plurality of multi-level symbols comprises a plurality of eight-level symbols, and wherein the selector is responsive to each multi-level symbol in order to calculate seven path metrics.

24. A data processor comprising:

receiving means for receiving a plurality of multi-level symbols;

selecting means for selecting one of only five sets of slice values, wherein each of the only five sets of slice values has a plurality of slice values; and,

slicing means responsive to the selected set of slice values for slicing and decoding the multi-level symbols.

25. The data processor of claim 24 wherein each of the only five sets of slice values has a number of slice values, wherein the multi-level symbols are characterized by a number of values, and wherein the number of slice values of each of the only five sets of slice values is less than one-half of the number of values characterizing the multi-level symbols.

26. The data processor of claim 24 wherein adjacent slice values of each of the only five sets of slice values are spaced apart from each other, and wherein the slice values of one of the only five sets of slice values are offset from the slice values of another one of the only five sets of slice values.

27. The data processor of claim 24 wherein adjacent slice values of each of the only five sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only five sets of slice values are offset by a substantially equal amount from the corresponding slice values of another one of the only five sets of slice values.

28. The data processor of claim 24 wherein each of the only five sets of slice values contains only five slice values.

29. The data processor of claim 28 wherein adjacent slice values of each of the only five sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the only five sets of slice values are offset by a substantially equal amount from the corresponding slice values of another one of the only five sets of slice values.

30. The data processor of claim 29 wherein the plurality of multi-level symbols comprises a plurality of eight-level symbols, and wherein the selector is responsive to each multi-level symbol for calculating seven path metrics.

31. A data processor comprising:

developing means for developing a data signal including a plurality of multi-level symbols;

determining means responsive to each of the multi-level symbols for determining the lowest path metric characterizing the data signal;

selecting means for selecting one of a plurality of sets of slice values in response to the lowest path metric; and,

slicing means responsive to the selected set of slice values for slicing and decoding the multi-level symbols.

32. The data processor of claim 31 wherein each of the sets of slice values has a number of slice values, wherein the multi-level symbols are characterized by a number of values, and wherein the number of slice values of each of the sets of slice values is less than one-half of the number of values characterizing the multi-level symbols.

33. The data processor of claim 31 wherein adjacent slice values of each of the sets of slice values are spaced apart

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from each other, and wherein the slice values of one of the sets of slice values are offset from the slice values of another one of the sets of slice values.

34. The data processor of claim 31 wherein adjacent slice values of each of the sets of slice values are spaced apart from each other by a substantially equal amount, and wherein the slice values of one of the sets of slice values are offset by a substantially equal amount from the corresponding slice values of another one of the sets of slice values.

35. The data processor of claim 31 wherein the data signal comprises a plurality of eight-level symbols encoded by a four-state encoder, and wherein the determining means comprises means responsive to each symbol for calculating four path metrics each corresponding to a respective state of the encoder.

36. The data processor of claim 35 wherein the four-state encoder is a convolutional encoder.

37. The data processor of claim 36 wherein the selecting means comprises means for selecting one of two sets of slice values, each of the sets of slice values containing three slice values.

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38. A data processor comprising:

a receiver arranged to receive a plurality of multi-level symbols;

a selector arranged to select one of a plurality of sets of slice values, wherein each set of slice values has a minimum of three slice values; and

a slicer having a symbol input, a selector input, and an output, wherein the slicer stores the plurality of sets of slice values, wherein the symbol input is coupled to receive the multi-level symbols from the receiver, wherein the selector input is coupled to the selector, and wherein the slicer is arranged to slice and decode the multi-level symbols dependent upon the set of slice values selected by the selector and to provide the sliced multi-level symbols at the output.

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US005748226A

United States Patent [19]
Limberg

[11] **Patent Number:** 5,748,226
[45] **Date of Patent:** May 5, 1998

[54] **DIGITAL TELEVISION RECEIVER WITH ADAPTIVE FILTER CIRCUITRY FOR SUPPRESSING NTSC CO-CHANNEL INTERFERENCE**

5,648,822 7/1997 Halydier 348/21

Primary Examiner—Victor R. Kostak

[75] **Inventor:** Allen LeRoy Limberg, Vienna, Va.

[57] **ABSTRACT**

[73] **Assignee:** Samsung Electronics Co., Ltd., Suwon, Rep. of Korea

Co-channel interference accompanying multiple-level symbols in a digital receiver, such as a digital television receiver, is suppressed by using a first comb filter to reduce the energy of the co-channel interference before data slicing. The first comb filter incidentally carries out a symbol re-coding procedure of first type that introduces error into the symbol decoding results generated by the data slicing. A second comb filter carries out a symbol re-coding procedure of second type after the data slicing to compensate for the symbol re-coding procedure of first type and generate corrected symbol decoding results. The symbol re-coding procedure of first type re-codes an input symbol stream through differential delay and first linear combination of the differentially delayed terms. The symbol re-coding procedure of second type re-codes the symbol stream recovered by data slicing, through second linear combination of the symbol stream with delayed result of the second linear combination, and is performed in accordance with a modular arithmetic. One of the first and second linear combinations is subtractive, and the other is additive. The results of the second linear combination are the corrected symbol decoding results.

[21] **Appl. No.:** 746,520

[22] **Filed:** Nov. 12, 1996

[31] **Int. Cl.:** H04N 5/38

[52] **U.S. Cl.:** 348/21; 348/470; 348/725; 348/607

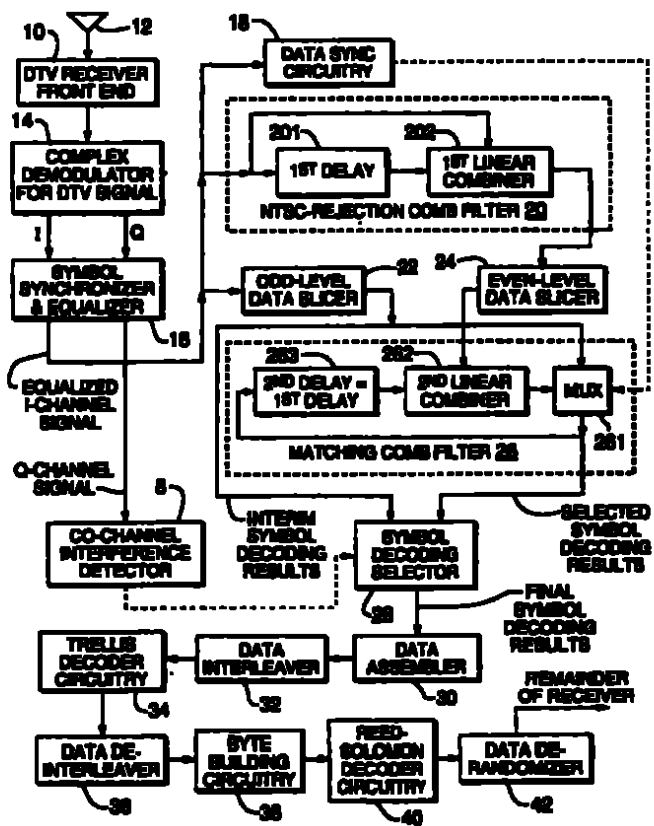
[58] **Field of Search:** 348/21, 607, 611, 348/613, 465, 725, 470; 375/251, 350, 261, 345, 346

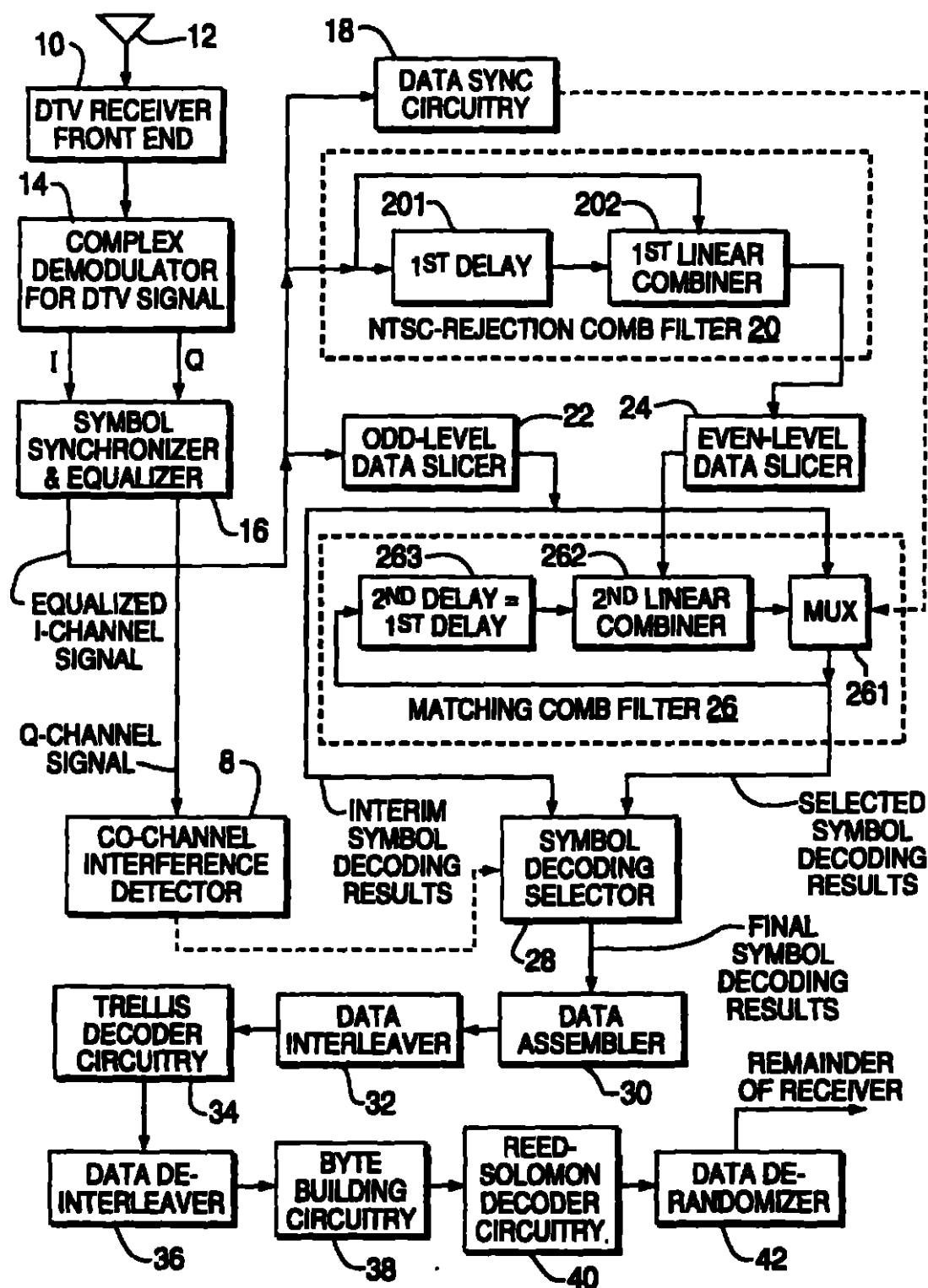
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31 Claims, 4 Drawing Sheets





ONE OF 1ST & 2ND LINEAR COMBINERS IS
A SUBTRACTOR & THE OTHER IS AN ADDER

FIG. 1

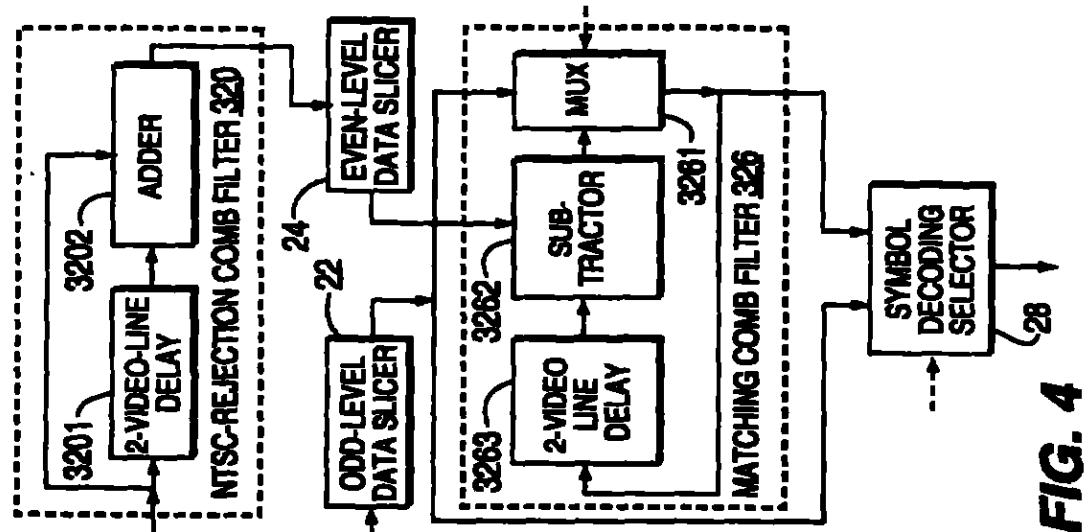


FIG. 4

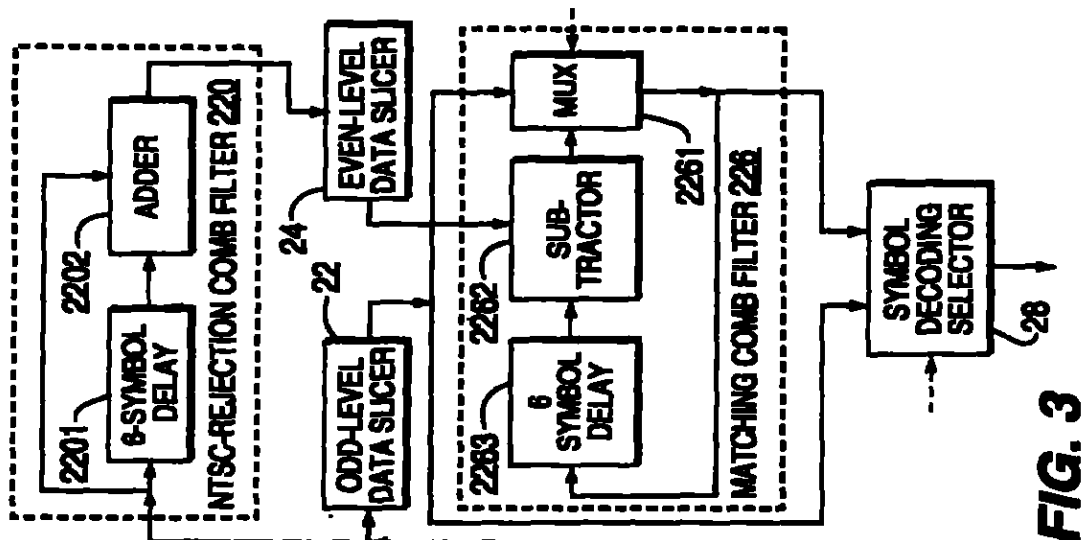


FIG. 3

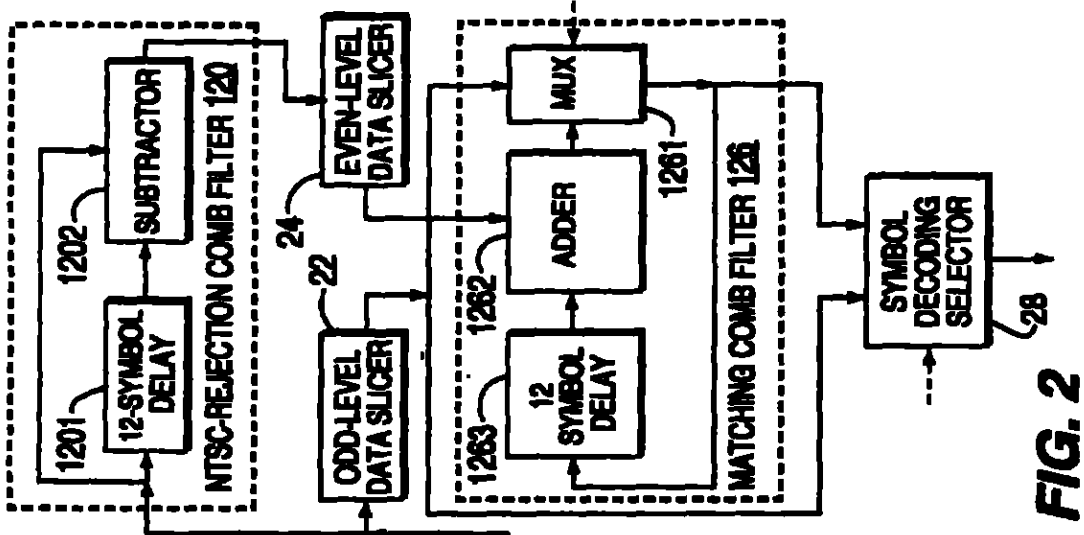


FIG. 2

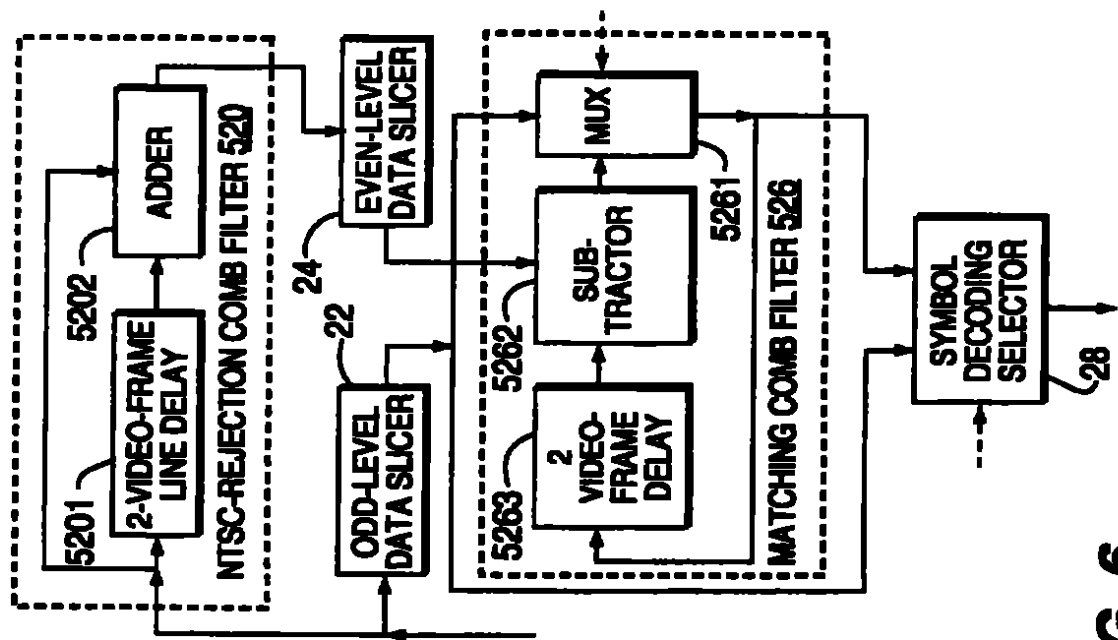


FIG. 5

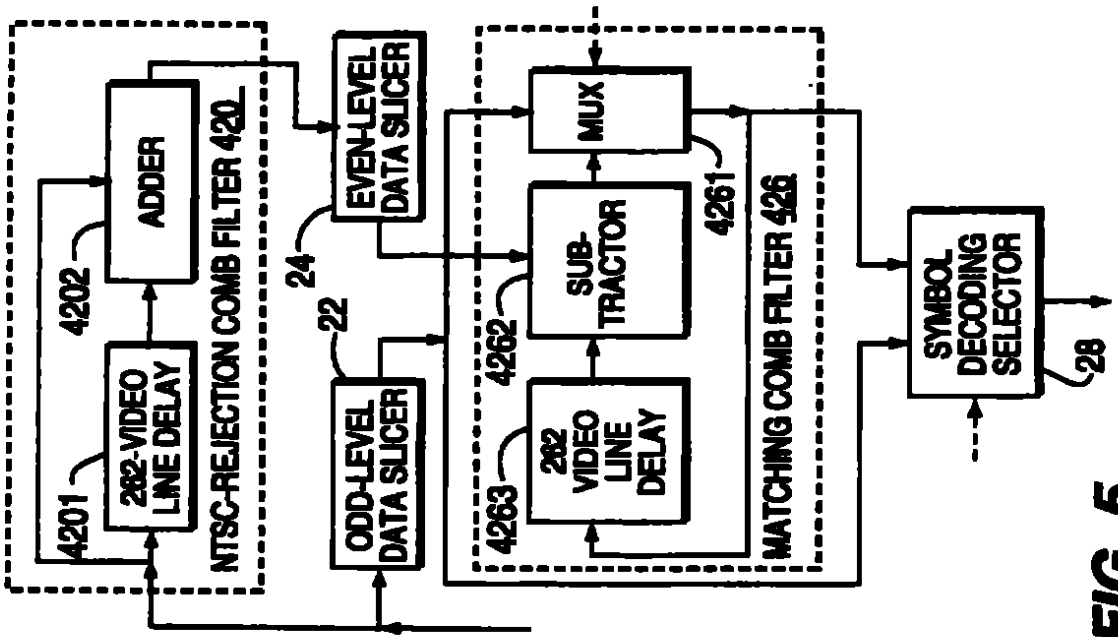


FIG. 6

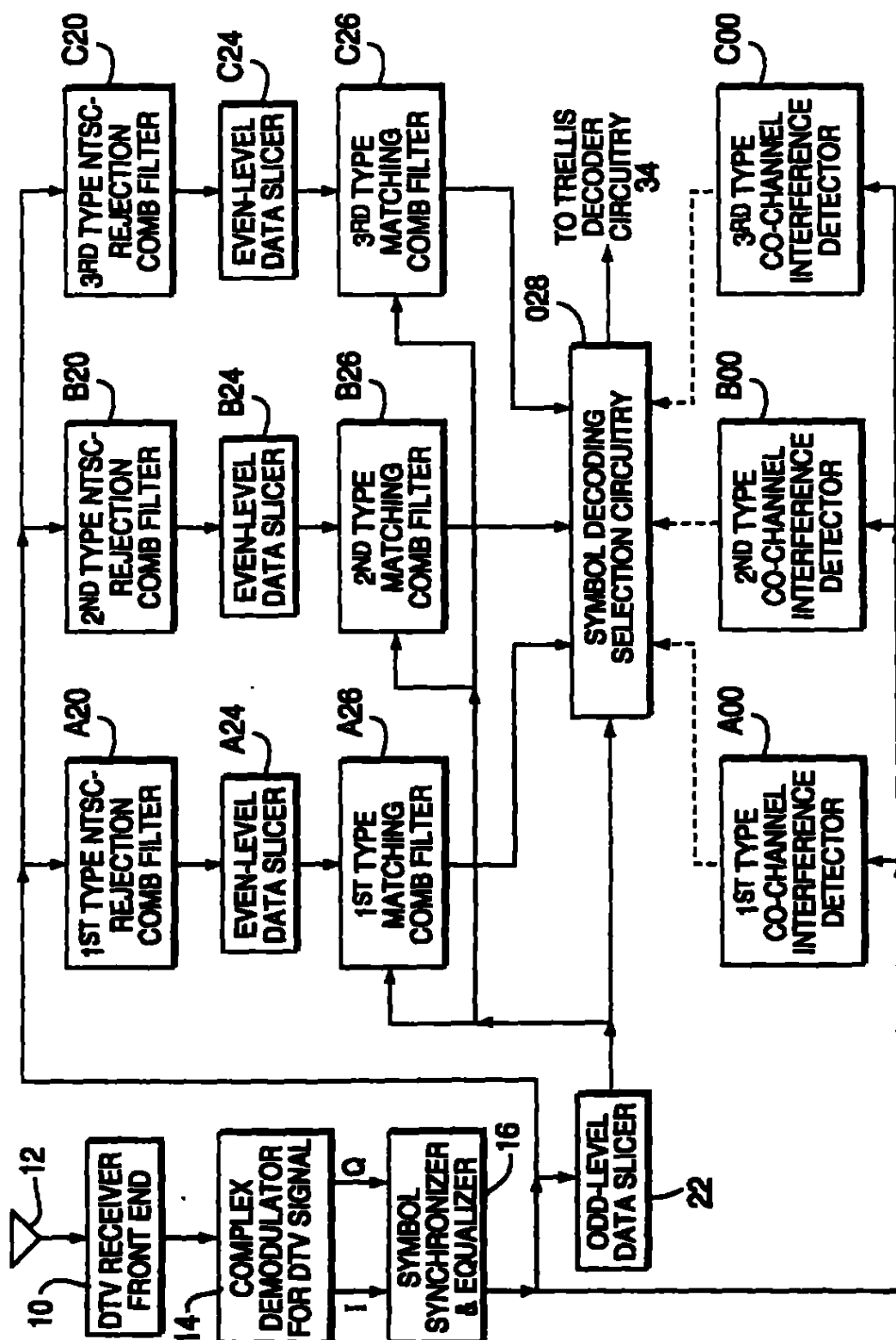


FIG. 7

A, B AND C ARE RESPECTIVE INTEGERS OF DIFFERENT VALUES SELECTED FROM 1, 2, 3, 4 & 5

DIGITAL TELEVISION RECEIVER WITH ADAPTIVE FILTER CIRCUITRY FOR SUPPRESSING NTSC CO-CHANNEL INTERFERENCE

The present invention relates to digital television systems, such as the digital high-definition television (HDTV) system used for terrestrial broadcasting in the United States of America in accordance with the Advanced Television Sub-Committee (ATSC) standard, and more particularly, to digital television receivers with adaptive filter circuitry for suppressing co-channel interference from analog television signals, such as those conforming to the National Television Systems Committee (NTSC) standard.

BACKGROUND OF THE INVENTION

The standard for digital HDTV signal terrestrial broadcasting in the United States of America is capable of accommodating the transmission of other digital television (DTV) formats, such as the parallel transmission of four television signals having normal definition in comparison to an NTSC analog television signal. DTV transmitted by vestigial-sideband (VSB) amplitude modulation (AM) during terrestrial broadcasting in the United States of America comprises a succession of consecutive-in-time data fields each containing 313 consecutive-in-time data segments. Each segment of data is preceded by a line synchronization code group of four symbols having successive values of +S, -S, -S and +S. The value +S is one level below the maximum positive data excursion, and the value -S is one level above the maximum negative data excursion. The segments of data are each of 77.3 microsecond duration, and there are 832 symbols per data segment for a symbol rate of about 10 MHz. The initial line of each data field is a field synchronization code group that codes a training signal for channel-equalization and multipath suppression procedures. The training signal is a 511-sample pseudo-noise sequence (or "PN-sequence") followed by three 63-sample PN sequences. This training signal is transmitted in accordance with a first logic convention in the first line of each odd-numbered data field and in accordance with a second logic convention in the first line of each even-numbered data field, the first and second logic conventions being one's complementary respective to each other.

The data within data lines are trellis coded using twelve interleaved trellis codes, each a $\frac{2}{3}$ rate trellis code with one uncoded bit. The interleaved trellis codes are subjected to Reed-Solomon forward error-correction coding, which provides for correction of burst errors arising from noise sources such as a nearby unshielded automobile ignition system. The Reed-Solomon coding results are transmitted as 8-level (3 bits/symbol) one-dimensional-constellation symbol coding for over-the-air transmission, which transmissions are made without symbol precoding separate from the trellis coding procedure. The Reed-Solomon coding results are transmitted as 16-level (4 bits/symbol) one-dimensional-constellation symbol coding for cablecast, which transmissions are made without precoding. The VSB signals have their natural carrier wave, which would vary in amplitude depending on the percentage of modulation, suppressed.

The natural carrier wave is replaced by a pilot carrier wave of fixed amplitude, which amplitude corresponds to a prescribed percentage of modulation. This pilot carrier wave of fixed amplitude is generated by introducing a direct component shift into the modulating voltage applied to the balanced modulator generating the amplitude-modulation

sidebands that are supplied to the filter supplying the VSB signal as its response. If the eight levels of 4-bit symbol coding have normalized values of -7, -5, -3, -1, +1, +3, +5 and +7 in the carrier modulating signal, the pilot carrier has a normalized value of 1.25. The normalized value of +S is +5, and the normalized value of -S is -5.

In the earlier development of the DTV art it was contemplated that the DTV broadcaster might be called upon to decide whether or not to use a symbol precoder at the transmitter, which symbol precoder would follow the symbol generation circuitry and provide for matched filtering of symbols, when used together with a comb filter in each DTV receiver used before the data-slicer in the symbol decoder circuitry as a symbol post-coder. This decision would have depended upon whether interference from a co-channel NTSC broadcasting station were expected or not. Symbol precoding would not have been used for data line synchronization code groups or during data lines in which data field synchronization data were transmitted. Co-channel interference is reduced at greater distances from the NTSC broadcasting station(s) and is more likely to occur when certain ionospheric conditions obtain, the summertime months during years of high solar activity being notorious for likelihood of co-channel interference. Such interference will not obtain if there are no co-channel NTSC broadcasting stations, of course. If there were likelihood of NTSC interference within his area of broadcast coverage, it was presumed that the HDTV broadcaster would use the symbol precoder to facilitate the HDTV signal being more easily separated from NTSC interference; and, accordingly, a comb filter would be employed as symbol post-coder in the DTV receiver to complete matched filtering. If there were no possibility of NTSC interference or there were insubstantial likelihood thereof, in order that flat spectrum noise would be less likely to cause erroneous decisions as to symbol values in the trellis decoder, it was presumed that the DTV broadcaster would discontinue using the symbol precoder; and, accordingly, the symbol post-coder would then be disabled in each DTV receiver.

U.S. Pat. No. 5,260,793 issued 9 Nov. 1993 to R. W. Chitt et al. and entitled "RECEIVER POST CODER SELECTION CIRCUIT" selectively employs a comb filter as a symbol post-coder for suppressing NTSC interference accompanying a real or in-phase baseband component (I channel) of the complex output signal of a demodulator used in a digital high-definition television (HDTV) receiver. The presence of NTSC interference in the I-channel component of the demodulator response is detected for developing control signals automatically to enable or disable the comb filter being used for suppressing NTSC co-channel interference. During each data field sync interval, the input signal to and the output signal from an NTSC suppression filter of comb filter type in the HDTV receiver are each compared with a respective signal that is known a priori and is drawn from memory within the HDTV receiver. If the minimum result of comparison with the input signal has less energy than the minimum result of comparison with the output signal from the NTSC suppression filter, this is indicative that the primary cause of variance from expected reception is random noise rather than NTSC co-channel interference. Insofar as the particular digital television receiver is concerned, reception would be better were precoding and post-coding not employed in the system, and it is presumed that the broadcaster has not employed precoding. If the minimum result of comparison with the input signal has more energy than the minimum result of comparison with the output signal from the NTSC suppression filter, this is

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indicative that the primary cause of variance from expected reception is NTSC co-channel interference rather than random noise. Insofar as the particular digital television receiver is concerned, reception would be better were pre-coding and post-coding employed in the system, and it is presumed that the broadcaster has employed precoding.

In the automatic symbol post-coder selection circuitry described in U.S. Pat. No. 5,260,793 applications, symbol post-coding is enabled during times when substantial co-channel NTSC interference is detected at the receiver and is otherwise disabled, without regard to whether the broadcaster employs precoding or not. This undesirably would lead to errors in trellis decoding results when the broadcaster did not employ the symbol precoder, but actual co-channel NTSC interference is substantial. These errors would have required that an over-ride of the automatic symbol post-coder selection circuitry be provided for actuation by the human being viewing the DTV receiver. Actual co-channel NTSC interference can be substantial for portions of the reception area for a broadcast without the broadcaster being aware of the condition, owing to freakish skip conditions, owing to cablecast leakage, owing to inadequate intermediate-frequency image suppression in NTSC receivers, owing to magnetic tape used for digital television recording having remnant previous analog television recording, or owing to some other unusual condition.

If there were to be selective employment of symbol precoding by the transmitter, it would be desirable that the use or non-use of symbol precoding by the transmitter be signaled, so that erroneous selection by the automatic post-coder selection circuitry could be avoided. The use or non-use of precoding by the transmitter could be signaled in the data lines used for field sync. Alternatively, the use or non-use of precoding by the transmitter could be signaled in the packet header information for each data packet. Signaling the use or non-use of precoding by the transmitter in the data lines used for field sync is advantageous over signaling in other data lines, in that the signaling is not affected by the use or non-use of post-coding by the digital television receiver. Currently, however, the digital television standard does not authorize the transmitter to use symbol precoding or to signal the use of symbol precoding.

The current ATSC DTV standard presumes that the suppression of co-channel interfering analog TV signal will be carried out in the trellis decoding process, after the data-slicing procedures associated with symbol decoding. This procedure avoids the problems alluded to above. However, co-channel interfering analog TV signal undesirably introduces errors into the data-slicing processes, which places more burden on the error-correction decoding procedures, trellis decoding and Reed-Solomon decoding. These errors will reduce the broadcast coverage area, which may lose revenue for the commercial DTV broadcaster. So, providing for the suppression of co-channel interfering analog TV signal before data-slicing is still desirable, despite symbol precoding at the DTV transmitter not being authorized by the current ATSC DTV standard.

The term "linear combination" in this specification and the claims appended thereto refers generically to addition and to subtraction, whether performed in accordance with a conventional arithmetic or a modular arithmetic. The term "modular combination" in this specification and the claims appended thereto refers to linear combination carried performed in accordance with a modular arithmetic. That type of coding that re-codes a digital symbol stream through differential delay and linear combination of the differentially delayed terms, exemplified by the symbol post-coding used

in prior-art HDTV receivers, is defined as "symbol re-coding of first type" in this specification and the claims appended hereto. That type of coding that re-codes a digital symbol stream through its modular combination with delayed result of the modular combination, exemplified by the symbol pre-coding used in prior-art HDTV transmitters, is defined as "symbol re-coding of second type" in this specification and the claims appended hereto.

The problem of co-channel interference from analog television signals is viewed in this specification more from the standpoint of being a sometime jamming problem at the receiver, to be solved by adaptive filter circuitry in the receiver, than has been the case in the prior art. So long as the dynamic range of the system channel is not exceeded, so that the co-channel interference can capture the system channel by destroying signal transmission capability for DTV modulation, the performance of the system can be viewed as a superposition of signals problem. The filter circuitry in the receiver is adapted for selecting the digital signal from the co-channel interference caused by the analog television signals, relying on the pronounced correlation and anti-correlation properties of the analog television signals to reduce their energy sufficiently as to capture the system channel from them.

Insofar as the co-channel interference from analog television signals is concerned, it enters the system channel after the DTV transmitter and before the DTV receiver. The use or non-use of symbol precoding at the DTV transmitter has no effect on the co-channel interference from analog television signals. At the DTV receiver, so long as the co-channel interference is not so large as to overload the receiver front-end and capture the system channel, it is advantageous to precede the data slicing circuitry with a comb filter for reducing the energy of higher-energy spectral components of the co-channel interference, thus to reduce the errors occurring during data slicing. The DTV broadcaster should adjust his carrier frequency, which is nominally 310 KHz above the lower limit frequency of the television channel assignment, so that his carrier frequency is optimally offset in frequency from the video carrier of a co-channel NTSC analog TV signal that is likely to interfere. This optimal offset in carrier frequency is exactly 59.75 times the horizontal scan line frequency f_H of the NTSC analog TV signal. The artifacts of the co-channel interference in the demodulated DTV signal will then include beats at 59.75 times the horizontal scan line frequency f_H of the NTSC analog TV signal, generated by heterodyne between the digital HDTV carrier and the video carrier of the co-channel interfering analog TV signal, and beats at 287.25 times f_H , generated by heterodyne between the digital HDTV carrier and the chrominance subcarrier of the co-channel interfering analog TV signal, which beats are quite close in frequency to the fifth harmonic of the beats at 59.75 times f_H . The artifacts will further include beats at approximately 345.75 times f_H , generated by heterodyne between the digital HDTV carrier and the audio carrier of the co-channel interfering analog TV signal, which beats are quite close in frequency to the sixth harmonic of the beats at 59.75 times f_H . The nearly harmonic relationship of these beats allows them all to be suppressed by a single properly designed comb filter incorporating only a few symbol epochs of differential delay. The use of an NTSC-rejection comb filter before data slicing incidentally introduces symbol re-coding of first type.

The data-slicing operation that follows first symbol re-coding in the DTV receiver is a quantizing process that is not destructive of the symbols resulting from the symbol

re-coding of first type. Insofar as the transmission of data is concerned, since the data quantization levels are designed to match the symbol levels. The quantization discriminates against the co-channel interfering analog TV signal remnants that remain after the filtering associated with symbol re-coding of first type and that are appreciably smaller than steps between symbol code levels, however. This is a species of the capture phenomenon in which phenomenon a stronger signal takes at the expense of a weaker one in a quantizing process.

Insofar as the transmission of data is concerned, the digital data symbol stream flows through the full length of the system channel. When symbol re-coding of second type is done as symbol precoding at the DTV transmitter, the additive combination of the differentially delayed data symbol streams is done on a modular basis that does not boost transmitter power or increase average intersymbol distance to help further in overcoming jamming analog TV signal. Instead, the principal mechanism for overcoming jamming analog TV signal is its attenuation vis-a-vis DTV signal, as provided by the comb filtering at the DTV receiver, causing the remnant analog TV signal in the comb filter response to be suppressed by the quantizing effects in the data slicer that immediately follows the comb filter.

The order of performing symbol re-coding procedures of first and second types has no appreciable effect on signal transmission through the system channel under such circumstances, the inventor points out, since neither coding scheme destroys signal transmission capability for the symbol stream. The order of performing symbol re-coding procedures of first and second types has no appreciable effect on the capability of the digital receiver to suppress co-channel interfering analog TV signal, as long as symbol re-coding of the second type is not interposed between symbol re-coding of the first type and the subsequent data slicing. This insight provides the foundation on which the invention is based.

SUMMARY OF THE INVENTION

The invention is directed to the suppression of co-channel interference accompanying multiple-level symbols in a digital receiver, such as a digital television receiver, by using a first comb filter to reduce the energy of the co-channel interference before data slicing. The first comb filter incidentally carries out a symbol re-coding procedure of first type that introduces error into the symbol decoding results generated by the data slicing. A second comb filter carries out a symbol re-coding procedure of second type after the data slicing, to compensate for the symbol re-coding procedure of first type and generate corrected symbol decoding results. The symbol re-coding procedure of first type re-codes an input symbol stream through differential delay and first linear combination of the differentially delayed terms. The symbol re-coding procedure of second type re-codes the symbol stream recovered by data slicing, through second linear combination of the symbol stream with delayed result of the second linear combination, and is performed in accordance with a modular arithmetic. The first linear combination is additive, and the second linear combination is subtractive. The results of the second linear combination are the corrected symbol decoding results.

An aspect of the invention is a method of symbol decoding a stream of $2N$ -level symbols each having a symbol epoch of a specified length in time, which stream of $2N$ -level symbols is susceptible to being accompanied by artifacts of co-channel interfering analog television signal. This method

of symbol decoding generates final symbol decoding results and comprises steps as follow. The stream of $2N$ -level symbols is comb filtered to generate a comb filter response with $(4N-1)$ -level symbols from which any odd artifacts of co-channel interfering analog television signal are suppressed. This step of comb filtering is accomplished by delaying the stream of $2N$ -level symbols by a prescribed number of symbol epochs to generate a delayed stream of $2N$ -level symbols, then linearly combining the stream of $2N$ -level symbols and the delayed stream of $2N$ -level symbols to generate first linear combining results as the comb filter response with $(4N-1)$ -level symbols. The linear combining in this step of comb filtering is an additive procedure. The stream of $2N$ -level symbols is data-sliced to generate interim symbol decoding results, and the comb filter response with $(4N-1)$ -level symbols is data-sliced to generate supplemental symbol decoding results. Selected symbol decoding results are delayed by a prescribed number of said symbol epochs to generate delayed selected symbol decoding results and are linearly combined with the supplemental symbol decoding results to generate second linear combining results. This latter step of linearly combining is a subtractive procedure since the linearly combining in the earlier step of comb filtering is an additive procedure. The interim symbol decoding results are selected to be the selected symbol decoding results at prescribed times and otherwise the second linear combining results are selected to be the selected symbol decoding results. When the stream of $2N$ -level symbols is determined to be currently accompanied by artifacts of co-channel interfering analog television signal of sufficient strength that the selected symbol decoding results are less likely to be in error than the interim symbol decoding results, the selected symbol decoding results are chosen as the final decoding results. When the stream of $2N$ -level symbols is determined not to be currently accompanied by artifacts of co-channel interfering analog television signal of sufficient strength that the selected symbol decoding results are less likely to be in error than the interim symbol decoding results, the interim symbol decoding results are chosen as said final decoding results.

A further aspect of the invention is embodied in a digital receiver, such as a digital television receiver, using a plurality of data slicers, each data slicer preceded by a different type of comb filter for reducing co-channel interference from an analog television signal, and each data slicer succeeded by a comb filter complementary to the comb filter preceding the data slicer for generating an estimate of correct symbol decoding result. Voting circuitry selects one of these estimates as a best estimate to be supplied as input signal to trellis decoder circuitry in the digital receiver.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block schematic diagram of a digital television signal receiver using an NTSC-rejection comb filter before symbol decoding and a matching comb filter after symbol decoding, in accordance with the invention, and using a co-channel interference detector of the type described in U.S. Pat. No. 5,260,793.

FIG. 2 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver when the NTSC-rejection comb filter employs a 12-symbol delay.

FIG. 3 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver when the NTSC-rejection comb filter employs a 6-symbol delay.

FIG. 4 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver when the NTSC-rejection comb filter employs a 2-video-line delay.

FIG. 5 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver when the NTSC-rejection comb filter employs a 262-video-line delay.

FIG. 6 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver when the NTSC-rejection comb filter employs a 2-video-frame delay.

FIG. 7 is a block schematic diagram of a digital television signal receiver constructed in accordance with a further aspect of the invention so as to utilize a plurality of symbol decoders operated in parallel, each preceded by a respective NTSC-rejection comb filter and succeeded by a matching comb filter, with the best estimate of correct symbol decoding being supplied to trellis decoding circuitry.

DETAILED DESCRIPTION

FIG. 1 shows a digital television signal receiver used for recovering error-collected data, which data are suitable for recording by a digital video cassette recorder or for MPEG-2 decoding and display in a television set. The FIG. 1 DTV signal receiver includes the "front end" electronics 10 including tuner and intermediate-frequency (I-F) amplifiers, shown as receiving broadcast DTV signals from an antenna 12. The "front end" electronics 10 preferably are of plural-conversion type including intermediate-frequency amplifiers at more than one intermediate-frequency band. Preferably, a surface-acoustic-wave (SAW) filter is used in at least one intermediate-frequency band to shape channel selection response and reject adjacent channels. This SAW filter cuts off rapidly just beyond 3.38 MHz remove from the suppressed carrier frequency and the pilot carrier, which is of like frequency and of fixed amplitude. This SAW filter accordingly rejects the frequency modulated sound carrier of any co-channel interfering analog TV signal. The sound carrier frequency is 5.75 MHz from the lowest frequency limit of the TV channel and has maximum ± 40 kHz frequency swing.

The sound carrier of any co-channel interfering analog TV signal can also be trap filtered in the "front end" electronics 10. For example, a SAW filter can be used to select the frequency-modulated sound carrier of any co-channel interfering analog TV signal from an I-F signal, and the SAW filter response can be destructively combined with that I-F signal to generate I-F signal substantially free from frequency-modulated sound carrier of any co-channel interfering analog TV signal. Removing the FM sound carrier of any co-channel interfering analog TV signal in the "front end" electronics 10 prevents artifacts therefrom being generated when the final I-F signal is detected to recover baseband symbols and forestalls such artifacts interfering with data-slicing of those baseband symbols during symbol decoding. The prevention of such artifacts interfering with data-slicing of those baseband symbols during symbol decoding is better than can be accomplished by relying on comb-filtering before data-slicing.

The final I-F output signals from the "front end" electronics 10 are supplied to a complex demodulator 14, which demodulates the vestigial-sideband amplitude-modulation DTV signal in the final intermediate-frequency band to recover a real baseband signal and an imaginary baseband signal. Demodulation may be done in the digital regime after analog-to-digital conversion of a final intermediate-frequency band in the few megacycle range as described for example by C. B. Patel et al in U.S. Pat. No. 5,479,449 issued 26 Dec. 1995 and entitled "DIGITAL VSB DETEC-

TOR WITH PHASE TRACKER, AS FOR INCLUSION IN AN HDTV RECEIVER". Alternatively, demodulation may be done in the analog regime, in which case the results are usually subjected to analog-to-digital conversion to facilitate further processing. The digital results of such demodulation procedures conventionally have 8-bit accuracy or more and describe $2N$ -level symbols that encode N bits of data. Currently, $2N$ is eight in the case where the FIG. 1 DTV signal receiver receives a through-the-air broadcast via the antenna 12 and is sixteen in the case where the FIG. 1 DTV signal receiver receives cablecast. The concern of the invention is with the reception of terrestrial through-the-air broadcasts, and FIG. 1 does not show the portions of the DTV receiver providing symbol decoding and error-correction decoding for received cablecast transmissions.

Symbol synchronizer and equalizer circuitry 16 receives at least the digitized real baseband signal from the complex demodulator 14; in the FIG. 1 DTV receiver the circuitry 16 is shown also receiving the digitized imaginary baseband signal. The circuitry 16 includes a digital filter with adjustable weighting coefficients that compensates for ghosts and tilt in the received signal. The symbol synchronizer and equalizer circuitry 16 provides symbol synchronization or "de-rotation" as well as amplitude equalization and ghost removal. Symbol synchronizer and equalizer circuitry in which symbol synchronization is accomplished before amplitude equalization is known from U.S. Pat. No. 5,479,449. In such designs the demodulator 14 will supply oversampled demodulator response containing real and imaginary baseband signals to the symbol synchronizer and equalizer circuitry 16. After symbol synchronization, the oversampled data are decimated to extract baseband I-channel signal at normal symbol rate, to reduce sample rate through the digital filtering used for amplitude equalization and ghost removal. Symbol synchronizer and equalizer circuitry in which amplitude equalization precedes symbol synchronization, "de-rotation" or "phase tracking" is also known to those skilled in the art of digital signal receiver design.

Each sample of the circuitry 16 output signal is resolved to ten or more bits and is, in effect, a digital description of an analog symbol exhibiting one of $(2N-8)$ levels. The circuitry 16 output signal is carefully gain-controlled by any one of several known methods, so the ideal step levels for symbols are known. One method of gain control, preferred because the speed of response of such gain control is exceptionally rapid, regulates the direct component of the real baseband signal supplied from the complex demodulator 14 to a normalized level of +1.25. This method of gain control is generally described in U.S. Pat. No. 5,479,449 and is more specifically described by C. B. Patel et al in U.S. patent application Ser. No. 5,573,454 filed 15 Dec. 1995 and entitled "AUTOMATIC GAIN CONTROL OF RADIO RECEIVER FOR RECEIVING DIGITAL HIGH-DEFINITION TELEVISION SIGNALS".

The output signal from the circuitry 16 is supplied as input signal to data sync circuitry 18, which recovers data field synchronization and data line synchronization information from the equalized baseband I-channel signal. Alternatively, the input signal to data sync circuitry 18 can be obtained prior to equalization. The data sync circuitry 18 is of interest in regard to the invention because it also supplies one or more multiplexer control signals each having two states, each multiplexer control signal a first of those two states at selected times, but otherwise exhibiting a second of those two states.

The equalized I-channel signal samples at normal symbol rate supplied as output signal from the circuitry 16 are

applied as the input signal to an NTSC-rejection comb filter 20. The comb filter 20 includes a first delay device 201 to generate a pair of differentially delayed streams of the 2N-level symbols and a first linear combiner 202 for linearly combining the differentially delayed symbol streams to generate the comb filter 20 response. As described in U.S. Pat. No. 5,260,793, the first delay device 201 can provide a delay equal to the period of twelve 2N-level symbols, and the first linear combiner 202 can be a subtractor. Each sample of the comb filter 20 output signal is resolved to ten or more bits and is, in effect, a digital description of an analog symbol exhibiting one of $(4N-1)=15$ levels.

The symbol synchronizer and equalizer circuitry 16 is presumed to be designed to suppress the direct bias component of its input signal (as expressed in digital samples), which direct bias component has a normalized level of +1.25 and appears in the real baseband signal supplied from the complex demodulator 14 owing to detection of the pilot carrier. Accordingly, each sample of the circuitry 16 output signal applied as comb filter 20 input signal is, in effect, a digital description of an analog symbol exhibiting one of the following normalized levels: -7, -5, -3, -1, +3, +5 and +7. These symbol levels are denominated as "odd" symbol levels and are detected by an odd-level data slicer 22 to generate interim symbol decoding results of 000, 001, 010, 011, 100, 101, 110 and 111, respectively.

Each sample of the comb filter 20 output signal is, in effect, a digital description of an analog symbol exhibiting one of the following normalized levels: -14, -12, -10, -8, -6, -4, -2, 0, +2, +4, +6, +8, +10, +12 and +14. These symbol levels are denominated as "even" symbol levels and are detected by an even-level data slicer 24 to generate supplementary symbol decoding results of 001, 010, 011, 100, 101, 110, 111, 000, 001, 010, 011, 100, 101, 110, and 111, respectively.

A comb filter 26 is used after the data slicers 22 and 24 to generate a matching filter response to the response of the comb filter 20 insofar as symbols are concerned. The comb filter 26 includes a 2-input multiplexer 261, a second linear combiner 262, and a second delay device 263 with delay equal to that of the first delay device 201 in the comb filter 20. The second linear combiner 262 is a modulo-8 adder if the first linear combiner 202 is a subtractor and is a modulo-8 subtractor if the first linear combiner 202 is an adder. The first linear combiner 202 and the second linear combiner 262 may be constructed as respective read-only memories (ROMs) to speed up linear combination operations sufficiently to support the sample rates involved.

The output signal of the multiplexer 261 reproduces one of the two input signals applied to the multiplexer 261, as controlled by a respective multiplexer control signal supplied to the multiplexer 261 from the data sync circuitry 18. The first input signal to the multiplexer 261 corresponds to the interim symbol decoding results supplied from the odd-level data slicer 22, and the multiplexer 261 is conditioned by its respective multiplexer control signal the being in the first of its two states to reproduce the interim symbol decoding results as its output signal. The second input signal to the multiplexer 261 corresponds to second linear combining results supplied from a second linear combiner 262, and the multiplexer 261 is conditioned by its respective multiplexer control signal the being in the second of its two states to reproduce the second linear combining results as its output signal. The output signal from the multiplexer 261 furnishes the response from the matching comb filter 26 and is delayed by the second delay device 263. The second linear combiner 262 combines the supplementary symbol decod-

ing results from the even-level data slicer 24 with the output signal from the second delay device 263.

The FIG. 1 DTV receiver uses a co-channel interference detector 4 of the general type described in U.S. Pat. No. 5,260,793. During each data field sync interval, the co-channel interference detector 4 compares both the input signal to and the output signal from the comb filter 20 with a respective signal that is known a priori and is drawn from memory within the DTV receiver. If the minimum result of comparison with the input signal to the comb filter 20 has less energy than the minimum result of comparison with the output signal from the comb filter 20, the co-channel interference detector 4 output signal is in a first of its two possible states, which first state is indicative that the primary cause of variance from expected reception is random noise rather than NTSC co-channel interference. This first state of the co-channel interference detector 4 output signal conditions the selector 28 to reproduce, as its output signal, the interim symbol decoding results from the odd-level data slicer 22. If the minimum result of comparison with the input signal to the comb filter 20 has more energy than the minimum result of comparison with the output signal from the comb filter 20, the co-channel interference controller 4 output signal is in a second of its two possible states, which second state is indicative that the primary cause of variance from expected reception is NTSC co-channel interference rather than random noise. This first state of the co-channel interference detector 4 output signal conditions the selector 28 to reproduce the comb filter 26 response as its output signal.

The output signal from the symbol decoding selector 28 comprises the final symbol decoding results in 3-parallel-bit groups, assembled by a data assembler 30 for application to a data interleaver 32. The data interleaver 32 commutates the assembled data into parallel data streams for application to trellis decoder circuitry 34. Trellis decoder circuitry 34 conventionally uses twelve trellis decoders. The trellis decoding results are supplied from the trellis decoder circuitry 34 to data de-interleaver circuitry 36 for de-commutation. Byte parsing circuitry 38 converts the data interleaver 36 output signal into bytes of Reed-Solomon error-correction coding for application to Reed-Solomon decoder circuitry 40, which performs Reed-Solomon decoding to generate an error-corrected byte stream supplied to a data de-randomizer 42. The data de-randomizer 42 supplies reproduced data to the remainder of the receiver (not shown). The remainder of a complete DTV receiver will include a packet sorter, an audio decoder, an MPEG-2 decoder and so forth. The remainder of a DTV receiver incorporated in a digital tape recorder/reproducer will include circuitry for converting the data to a form for recording.

The symbol synchronizer and equalizer circuitry 16 is presumed in the foregoing description to be designed to suppress the direct bias component of its input signal (as expressed in digital samples), which direct bias component has a normalized level of +1.25 and appears in the real baseband signal supplied from the complex demodulator 14 owing to detection of the pilot carrier. Alternatively, the symbol synchronizer and equalizer circuitry 16 is designed to preserve the direct bias component of its input signal, which simplifies the design of the equalization filter in the circuitry 16 somewhat. In such case the data-slicing levels in the odd-level data slicer 22 are offset to take into account the direct bias component accompanying the data steps in its input signal. Providing that the first linear combiner 202 is a subtractor, whether the circuitry 16 is designed to suppress or to preserve the direct bias component of its input signal

has no consequence in regard to the data-slicing levels in the even-level data slicer 24. However, if the differential delay provided by the first delay device 201 is chosen so that the first linear combiner 202 is an adder, the data-slicing levels in the even-level data slicer 24 should be offset to take into account the doubled direct bias component accompanying the data steps in its input signal.

Arrangements are possible in which one data slicer replaces the odd-level data slicer 22 and the even-level data slicer 24 with a single data slicer, using multiplexer connections to shift its place in circuit and to provide bias to modify its slicing ranges, but these arrangements are not preferred because of the complexity of operation.

FIG. 2 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver using a species 120 of the NTSC-rejection comb filter 20 and a species 126 of the matching comb filter 26. A subtractor 1202 serves as the first linear combiner in the NTSC-rejection comb filter 120, and a modulo-8 adder 1262 serves as the second linear combiner in the matching comb filter 126. The NTSC-rejection comb filter 120 uses a first delay device 1201 exhibiting a delay of twelve symbol epochs, and the matching comb filter 126 uses a second delay device 1263 also exhibiting a delay of twelve symbol epochs. The 12-symbol delay exhibited by each of the delay devices 1201 and 1263 is close to one cycle delay of the artifact of the analog TV video carrier at 59.75 times the analog TV horizontal scan frequency f_H . The 12-symbol delay is close to five cycles of the artifact of the analog TV chrominance subcarrier at 287.25 times f_H . The 12-symbol delay is close to six cycles of the artifact of the analog TV sound carrier at 345.75 times f_H . This is the reason that the differentially combined response of the subtractor 1202 to the audio carrier, to the video carrier and to frequencies close to chrominance subcarrier differentially delayed by the first delay device 1201 tends to have reduced co-channel interference. However, in portions of a video signal in which edges cross a horizontal scan line, the amount of correlation in the analog TV video signal at such distances in the horizontal spatial direction is quite low.

A species 1261 of the multiplexer 261 is controlled by a multiplexer control signal that is in its first state for twelve symbol epochs at the beginning of each data segment. At other times the multiplexer 1261 control signal is in its second state, provided there is no indication supplied during data slicing or the trellis decoding operations that a symbol decoding result used to form a particular one of the twelve interleaved trellis codes is very likely to have been corrupted. When such indication is supplied, particularly during the earlier portion of a data segment, the multiplexer control signal can be placed into its first state the twelfth following symbol epoch. This will help forestall long running errors that are characteristic of differential coding schemes.

FIG. 3 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver using a species 220 of the NTSC-rejection comb filter 20 and a species 226 of the matching comb filter 26. The NTSC-rejection comb filter 220 uses a first delay device 2201 exhibiting a delay of six symbol epochs, and the matching comb filter 226 uses a second delay device 2263 also exhibiting a delay of six symbol epochs. The 6-symbol delay exhibited by each of the delay devices 2201 and 2263 is close to 0.5 cycle delay of the artifact of the analog TV video carrier at 59.75 times the analog TV horizontal scan frequency f_H , close to 2.5 cycles of the artifact of the analog TV chrominance subcarrier at 287.25 times f_H , and close to 3 cycles of any artifact of the analog TV audio carrier at

345.75 times f_H . An adder 2202 serves as the first linear combiner in the NTSC-rejection comb filter 220, and a modulo-8 subtractor 2262 serves as the second linear combiner in the matching comb filter 226. Since the delay exhibited by the delay devices 2201 and 2263 is shorter than the delay exhibited by the delay devices 1201 and 1263, although nulls near frequencies converted from analog TV carrier frequencies are narrower band, there is more likely to be good anti-correlation in the signals additively combined by the adder 2202 than there is likely to be good correlation in the signals differentially combined by the subtractor 1202. The suppression of the sound carrier is poorer in the NTSC-rejection comb filter 220 response than in the NTSC-rejection comb filter 120 response. However, if the sound carrier of a co-channel interfering analog TV signal has been suppressed by SAW filtering or a sound trap in the "front end" electronics 10, the poor sound rejection of the comb filter 220 is not a problem. The responses to sync tips is reduced in duration using the NTSC-rejection comb filter 220 of FIG. 3 rather than the NTSC-rejection comb filter 120 of FIG. 2, so there is substantially reduced tendency to overwhelm error-correction in the trellis decoding and Reed-Solomon coding.

A species 2261 of the multiplexer 261 is controlled by a multiplexer control signal that is in its first state for six symbol epochs at the beginning of each data segment. At other times the multiplexer 2261 control signal is in its second state, provided there is no indication supplied during data slicing or the trellis decoding operations that a symbol decoding result is very likely to have been corrupted. When such indication is supplied, particularly during the earlier portion of a data segment, the multiplexer control signal can be placed into its first state the sixth following symbol epoch. This will help forestall long running errors that are characteristic of differential coding schemes.

FIG. 4 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver using a species 320 of the NTSC-rejection comb filter 20 and a species 326 of the matching comb filter 26. The NTSC-rejection comb filter 320 uses a first delay device 3201 exhibiting a delay of 1368 symbol epochs, which delay is substantially equal to the duration of two horizontal scan lines of an analog TV signal, and the matching comb filter 326 uses a second delay device 3263 also exhibiting such delay. The first linear combiner in the NTSC-rejection comb filter 320 is an adder 3202, and the second linear combiner in the matching comb filter 326 is a modulo-8 subtractor 3262. A species 3261 of the multiplexer 261 is controlled by a multiplexer control signal that is in its first state during a portion of the first data segment in each data field, which portion is known a priori at the DTV receiver. The symbol codes applied as input signal to the delay device 3261 device during this portion of the first data segment in each data field can be corrected when necessary. At other times the multiplexer 3261 control signal is in its second state, provided there is no indication supplied during data slicing or the trellis decoding operations that a symbol decoding result is very likely to have been corrupted. When such indication is supplied, particularly during the earlier portion of a data field, the multiplexer control signal can be placed into its first state the 1368th following symbol epoch. This will help forestall long running errors that are characteristic of differential coding schemes.

The FIG. 4 NTSC-rejection comb filter 320 is quite good in suppressing demodulation artifacts generated in response to analog TV horizontal synchronizing pulses, as well as suppressing many of the demodulation artifacts generated in

response to analog TV vertical synchronizing pulses and equalizing pulses. These artifacts are the co-channel interference with highest energy. Except where there is scan-line-to-scan-line change in the video content of the analog TV signal over the period of two scan lines, the NTSC-rejection comb filter 320 provides reasonably good suppression of that video content regardless of its color. The suppression of the FM audio carrier of the analog TV signal is reasonably good, in case it has not been suppressed by a tracking rejection filter in the symbol synchronization and equalization circuitry 16. Artifacts of most analog TV color bursts are suppressed in the NTSC-rejection comb filter 320 response, too. Furthermore, the filtering provided by the NTSC-rejection comb filter 320 is "orthogonal" to the NTSC-interference rejection built into the trellis decoding procedures.

A modification that can be made to the portion of the FIG. 1 digital television signal receiver shown in FIG. 44 is to replace the multiplier 3261 with a three-input multiplier permitting correct symbol codes for the portion of the first data segment in each data field known a priori at the DTV receiver to be selected from a memory in the DTV receiver.

FIG. 5 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver using a species 420 of the NTSC-rejection comb filter 20 and a species 426 of the matching comb filter 26. The NTSC-rejection comb filter 420 uses a first delay device 4201 exhibiting a delay of 179,208 symbol epochs, which delay is substantially equal to the period of 262 horizontal scanning lines of an analog TV signal, and the matching comb filter 426 uses a second delay device 4261 also exhibiting such delay. An adder 4202 serves as the first linear combiner in the NTSC-rejection comb filter 420, and a modulo-8 subtractor 4262 serves as the second linear combiner in the matching comb filter 426.

A species 4261 of the multiplier 461 is controlled by a multiplier control signal that is in its first state when field-to-field motion for an analog TV pixel associated with the current symbol epoch is detected. At other times the multiplier 4261 control signal is in its second state, provided there is no indication supplied during data slicing or the trellis decoding operations that a symbol decoding result is very likely to have been corrupted. When such indication is supplied a prescribed number of times, the multiplier control signal can be placed into its first state the 179,208th following symbol epoch. This will help forestall plural-frame running errors for each particular analog TV pixel. Indications of error can also be generated during a portion of the first data segment in each data field, which portion is known a priori at the DTV receiver, and the symbol codes applied as input signal to the delay device by the second delay device 4261 can be corrected when necessary.

The FIG. 5 NTSC-rejection comb filter 420 suppresses most demodulation artifacts generated in response to analog TV vertical synchronizing pulses and equalizing pulses, as well as suppressing all the demodulation artifacts generated in response to analog TV horizontal synchronizing pulses. These artifacts are the co-channel interference with highest energy. Also, the NTSC-rejection comb filter 420 suppresses artifacts arising from the video content of the analog TV signal that does not change from field to field or line-to-line, getting rid of stationary patterns irrespective of their horizontal spatial frequency or color. Artifacts of most analog TV color bursts are suppressed in the NTSC-rejection comb filter 420 response, too.

FIG. 6 is a block schematic diagram showing details of a portion of the FIG. 1 digital television signal receiver using

a species 520 of the NTSC-rejection comb filter 20 and a species 526 of the matching comb filter 26. The NTSC-rejection comb filter 520 uses a first delay device 5201 exhibiting a delay of 718,200 symbol epochs, which delay is substantially equal to the period of two frames of an analog TV signal, and the matching comb filter 526 uses a second delay device 5261 also exhibiting such delay. An adder 5202 serves as the first linear combiner in the NTSC-rejection comb filter 520, and a modulo-8 subtractor 5262 serves as the second linear combiner in the matching comb filter 526.

A species 5261 of the multiplier 261 is controlled by a multiplier control signal that is in its first state when frame-to-frame motion for an analog TV pixel associated with the current symbol epoch is detected. At other times the multiplier 5261 control signal is in its second state, provided there is no indication supplied during data slicing or the trellis decoding operations that a symbol decoding result is very likely to have been corrupted. When such indication is supplied a prescribed number of times, the multiplier control signal can be placed into its first state the 718,200th following symbol epoch. This will help forestall plural-frame running errors for each particular analog TV pixel. Indications of error can also be generated during a portion of the first data segment in each data field, which portion is known a priori at the DTV receiver, and the symbol codes applied as input signal to the delay device by the second delay device 5261 can be corrected when necessary.

The FIG. 6 NTSC-rejection comb filter 520 suppresses all demodulation artifacts generated in response to analog TV vertical synchronizing pulses and equalizing pulses, as well as suppressing all the demodulation artifacts generated in response to analog TV horizontal synchronizing pulses. These artifacts are the co-channel interference with highest energy. Also, the NTSC-rejection comb filter 520 suppresses artifacts arising from the video content of the analog TV signal that does not change over two frames, getting rid of such very stationary patterns irrespective of their spatial frequency or color. Artifacts of all analog TV color bursts are suppressed in the NTSC-rejection comb filter 520 response, too.

One skilled in the art of television system design will discern other properties of correlation and anti-correlation in analog TV signals that can be exploited in the design of NTSC-rejection filters of still other types than those shown in FIGS. 2. The use of NTSC-rejection filters that cascade two NTSC-rejection filters of the types already disclosed increases the 2N levels of the baseband signals to (2N-1) data levels. Such filters may be required to overcome particularly bad co-channel interference problems despite their shortcoming of reducing signal-to-noise for random noise interferences with symbol decoding.

FIG. 7 shows a modification of a digital television signal receiver as thusfar described, constructed in accordance with a further aspect of the invention so as to utilize a plurality of symbol decoders operated in parallel, each preceded by a respective NTSC-rejection comb filter and succeeded by a matching comb filter. The prefixes A, B and C in the identification numbers for the elements of FIG. 9 are different integers which will correspond to respective ones of the integers 1, 2, 3, 4 and 5 when receiver portions as shown in ones of FIGS. 2-6 are employed. The symbol decoding selector 28 that has no decision-making capability of its own is replaced with symbol decoding selection circuitry 628. The symbol decoding selection circuitry 628 has decision-making capability of its own and supplies a best estimate of correct symbol decoding for application to the trellis decoding circuitry 34.

A co-channel interference detector A00 of a first type determines whether co-channel interference from an analog TV signal is such that a first NTSC-rejection filter A20 of a first type will be effective in reducing that interference substantially. The co-channel interference detector A00 includes a first NTSC-extraction comb filter having a comb filter characteristic complementary to the first NTSC-rejection filter A20. The first NTSC-extraction comb filter is arranged to respond to the baseband I-channel signal, and the response of that filter is cored to remove signal excursions within the expected range for symbol levels. The energy of the cored response is then measured to generate an indication to of how effective the NTSC-rejection filter A20 of first type will be in reducing current co-channel interference, which indication is supplied from the co-channel interference detector A00 to the symbol decoding selection circuitry 028.

A co-channel interference detector B00 of a second type determines whether co-channel interference from an analog TV signal is such that a NTSC-rejection filter B20 of second type will be effective in reducing that interference substantially. The co-channel interference detector B00 includes a second NTSC-extraction comb filter having a comb filter characteristic complementary to the NTSC-rejection filter B20. The second NTSC-extraction comb filter is arranged to respond to the baseband I-channel signal and the response of that filter is cored to remove signal excursions within the expected range for symbol levels. The energy of the cored response is then measured to generate an indication to of how effective the NTSC-rejection filter B20 of second type will be in reducing current co-channel interference, which indication is supplied from the co-channel interference detector B00 to the symbol decoding selection circuitry 028.

A co-channel interference detector C00 of a third type determines whether co-channel interference from an analog TV signal is such that a NTSC-rejection filter C20 of third type will be effective in reducing that interference substantially. The co-channel interference detector C00 includes a third NTSC-extraction comb filter having a comb filter characteristic complementary to the NTSC-rejection filter C20. The third NTSC-extraction comb filter is arranged to respond to the baseband I-channel signal and the response of that filter is cored to remove signal excursions within the expected range for symbol levels. The energy of the cored response is then measured to generate an indication to of how effective the NTSC-rejection filter C20 of third type will be in reducing current co-channel interference, which indication is supplied from the co-channel interference detector C00 to the symbol decoding selection circuitry 028.

The odd-level data-slicer 22 supplies interim symbol decoding results to a matching comb filter A26 of a first type, to a matching comb filter B26 of a second type, and to a matching comb filter C26 of a third type. An even-level data-slicer A24 converts the response of the NTSC-rejection filter A20 to first supplemental symbol decoding results for application to the matching comb filter A26. An even-level data-slicer B24 converts the response of the NTSC-rejection filter B20 to second supplemental symbol decoding results for application to the matching comb filter B26. An even-level data-slicer C24 converts the response of the NTSC-rejection filter C20 to third supplemental symbol decoding results for application to the matching comb filter C26.

The symbol decoding selector 028 includes voting circuitry for polling the symbol codes supplied from the odd-level data slicer 22, the matching comb filter A26 of first type, the matching comb filter B26 of second type, and the matching comb filter C26 of third type. If all four of the

symbol decoding results concur, the symbol decoding result concurred to is supplied to the trellis coder circuitry 34. If the symbol decoding results supplied from the odd-level data slicer 22, the matching comb filter A26 of first type, the matching comb filter B26 of second type, and the matching comb filter C26 of third type do not concur a simple voting procedure can be carried out by the voting circuitry to select the decoding result least likely to be in error.

More accurate symbol decoding will be obtained more of the time if a weighted voting procedure is followed in the voting circuitry. The weights for voting can be determined solely from the indications supplied from the co-channel interference detectors A00, B00 and C00. This avoids the need for replicating the trellis decoder circuitry 34. This procedure can be modified to take into account the variances of the decoding results, reducing the weight accorded a decoding result in the voting procedure if it departs from a decoding result concurred in by a majority of the other symbol decoding circuits.

The trellis decoder circuitry 34 may be replicated and the relative success of various symbol decoding decisions can be compared to refine the best estimate of symbol decoding result further. This involves considerably more digital hardware, however.

The best estimate of symbol decoding results are used to correct the summation procedures in the matching comb filters A26, B26 and C26 in variants of the FIG. 7 digital receiver apparatus constructed in accordance with still further aspects of the invention.

The FIG. 7 digital receiver apparatus is modified in yet other embodiments of the invention to use additional parallel data-slicing operations, each carried out by a cascade connection of respective NTSC-rejection filter followed by a respective even-level data slicer followed by a respective matching comb filter. Each additional NTSC-rejection filter is provided an additional co-channel interference detector for determining whether co-channel interference from an analog TV signal is currently such that the NTSC-rejection filter will be effective in suppressing it. While two additional parallel data-slicing operations are shown in FIG. 7, modifications to use still further parallel data-slicing operations can provide capability for refining the best estimate of correct symbol decoding result still further.

The NTSC-rejection comb filter A20 and the matching comb filter A26 circuitry are advantageously chosen to be of types like the NTSC-rejection comb filter 320 and the matching comb filter 326 circuitry of FIG. 6. The NTSC-extraction comb filter A00 then comprises a delay device for differentially delaying the equalized baseband I-channel signal by 718,200 symbol epochs and an subtractor for linearly combining the differentially delayed equalized baseband I-channel signal. (From the standpoint of minimizing digital hardware, the delay device preferably is the delay device 3201 put to dual use.) The high-energy demodulation artifacts generated in response to analog TV synchronizing pulses, equalizing pulses, and color bursts are all suppressed when the NTSC-rejection comb filter A20 additively combines alternate video frames. Also, artifacts arising from the video content of the analog TV signal that does not change over two frames are suppressed, getting rid of stationary patterns irrespective of their spatial frequency or color.

The remaining problem of suppressing demodulation artifacts primarily concerns suppressing those demodulation artifacts arising from frame-to-frame difference at certain pixel locations within the analog TV signal raster. These demodulation artifacts can be suppressed by intra-frame

filtering techniques. The NTSC-rejection comb filter B20 and the matching comb filter B26 circuitry can be chosen to suppress remnant demodulation artifacts by relying on correlation in the horizontal direction, and the NTSC-rejection comb filter C20 and the matching comb filter C26 circuitry can be chosen to suppress remnant demodulation artifacts by relying on correlation in the vertical direction. Consider how such a design decision can be further implemented.

If the sound carrier of a co-channel interfering analog TV signal has not been suppressed by SAW filtering or a sound trap in the "front end" electronics 10, the NTSC-rejection comb filter B20 and the matching comb filter B26 circuitry are advantageously chosen to be of types like the NTSC-rejection comb filter 120 and the matching comb filter 126 circuitry of FIG. 2. The NTSC-extraction comb filter B00 then comprises a delay device for differentially delaying the equalized baseband I-channel signal by twelve symbol epochs and an adder for linearly combining the differentially delayed equalized baseband I-channel signal.

If the sound carrier of a co-channel interfering analog TV signal has been suppressed by SAW filtering or a sound trap in the "front end" electronics 10, the NTSC-rejection comb filter B20 and the matching comb filter B26 circuitry are advantageously chosen to be of types like the NTSC-rejection comb filter 220 and the matching comb filter 226 circuitry of FIG. 3. The NTSC-extraction comb filter B00 then comprises a delay device for differentially delaying the equalized baseband I-channel signal by six symbol epochs and a subtractor for linearly combining the differentially delayed equalized baseband I-channel signal.

The optimal choice of the NTSC-rejection comb filter C20 and the matching comb filter C26 circuitry is less straightforward, because of the choice one must make (in consideration of field interlace in the interfering analog TV signal) whether to choose the temporally closer scan line in the same field or the spatially closer line in the preceding field to be combined with the current scan line in the NTSC-rejection comb filter C20. Choosing the temporally closer scan line in the same field is generally the better choice, since jump cuts between fields are less likely to ravage NTSC rejection by the comb filter C20. With such choice, the NTSC-rejection comb filter C20 and the matching comb filter C26 circuitry are of types like the NTSC-rejection comb filter 320 and the matching comb filter 326 circuitry of FIG. 4. With the other choice instead, the NTSC-rejection comb filter C20 and the matching comb filter C26 circuitry are of types like the NTSC-rejection comb filter 420 and the matching comb filter 426 circuitry of FIG. 5.

The FIG. 7 digital receiver apparatus is modified in yet other embodiments of the invention to use additional parallel data-slicing operations. This allows the NTSC-rejection comb filter C20 and the matching comb filter C26 circuitry to be of types like the NTSC-rejection comb filter 320 and the matching comb filter 326 circuitry of FIG. 4, for example, while still allowing the use of a further NTSC-rejection comb filter and further matching comb filter circuitry of types like the NTSC-rejection comb filter 420 and the matching comb filter 426 circuitry of FIG. 5.

One skilled in the art of digital communications receiver design and acquainted with the foregoing specification and its drawing will be enabled to design many embodiments of the invention other than the preferred ones specifically described. This should be borne in mind when construing the scope of the broader claims which follow. In the claims which follow, the word "said" is used whenever reference is

made to an antecedent, and the word "the" is used for grammatical purposes other than to refer back to an antecedent.

What is claimed is:

1. A method of symbol decoding a stream of $2N$ -level symbols each having a symbol epoch of a specified length in time, which said stream of $2N$ -level symbols is susceptible to being accompanied by artifacts of co-channel interfering analog television signal, said method generating final symbol decoding results and comprising the steps of:

comb filtering said stream of $2N$ -level symbols to generate a comb filter response with $(4N-1)$ -level symbols from which any said artifacts of co-channel interfering analog television signal are suppressed, said step of comb filtering including substeps of delaying said stream of $2N$ -level symbols by a prescribed number of said symbol epochs to generate a delayed stream of $2N$ -level symbols and linearly combining said stream of $2N$ -level symbols and said delayed stream of $2N$ -level symbols, in an addition procedure for generating first linear combining results as said comb filter response with $(4N-1)$ -level symbols;

data-slicing said stream of $2N$ -level symbols to generate interim symbol decoding results;

data-slicing said comb filter response with $(4N-1)$ -level symbols to generate supplemental symbol decoding results;

delaying selected symbol decoding results by a prescribed number of said symbol epochs to generate delayed selected symbol decoding results;

linearly combining said supplemental symbol decoding results with said delayed selected symbol decoding results, in accordance with a subtraction procedure carried out in a modulo- $2N$ arithmetic for generating second linear combining results;

selecting said interim symbol decoding results to be said selected symbol decoding results at prescribed times and otherwise selecting said second linear combining results to be said selected symbol decoding results;

determining when said stream of $2N$ -level symbols is currently accompanied by artifacts of co-channel interfering analog television signal of sufficient strength that said selected symbol decoding results are less likely to be in error than said interim symbol decoding results and when said stream of $2N$ -level symbols is not currently accompanied by artifacts of co-channel interfering analog television signal of sufficient strength that said selected symbol decoding results are less likely to be in error than said interim symbol decoding results;

choosing said interim symbol decoding results as said final decoding results, responsive to it being determined said stream of $2N$ -level symbols is not currently accompanied by artifacts of co-channel interfering analog television signal of sufficient strength that said selected symbol decoding results are less likely to be in error than said interim symbol decoding results; and

choosing said selected symbol decoding results as said final decoding results, responsive to it being determined said stream of $2N$ -level symbols is currently accompanied by artifacts of co-channel interfering analog television signal of sufficient strength that said selected symbol decoding results are less likely to be in error than said interim symbol decoding results.

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2. The method of symbol decoding set forth in claim 1, wherein said prescribed number of said symbol epochs is six.

3. The method of symbol decoding set forth in claim 1, wherein said prescribed number of said symbol epochs is substantially equal to the duration of two horizontal scanning lines of said co-channel interfering analog television signal.

4. The method of symbol decoding set forth in claim 1, wherein said prescribed number of said symbol epochs is substantially equal to the duration of two hundred sixty-two horizontal scanning lines of said co-channel interfering analog television signal.

5. The method of symbol decoding set forth in claim 1, wherein said prescribed number of said symbol epochs is substantially equal to the duration of two video frames of said co-channel interfering analog television signal.

6. In combination:

a digital television signal detection apparatus for supplying a stream of $2N$ -level symbols each having a symbol epoch of a specified length in time, which stream is susceptible to being accompanied by artifacts of co-channel interfering analog television signal;

a first data slicer decoding said stream of $2N$ -level symbols for generating interim symbol decoding results;

a first delay device for exhibiting a delay of a prescribed first number of said symbol epochs, connected to respond to said stream of $2N$ -level symbols with a first delayed stream of $2N$ -level symbols, thereby to generate a first pair of differentially delayed streams of said $2N$ -level symbols;

a first linear combiner which in an addition process linearly combines said first pair of differentially delayed streams of said $2N$ -level symbols susceptible to being accompanied by artifacts of co-channel interfering analog television signal, received as first and second respective input signals of said first linear combiner, to generate a first stream of $(4N-1)$ -level symbols as an output signal of said first linear combiner, said first stream of $(4N-1)$ -level symbols providing a first comb filter response in which said artifacts of co-channel interfering analog television signal are suppressed;

a second linear combiner which in a subtraction process carried out in accordance with a modulo- $2N$ arithmetic linearly combines respective first and second input signals received thereby for supplying a respective output signal therefrom;

a second data slicer decoding said first stream of $(4N-1)$ -level symbols supplied as respective output signal from said first linear combiner, for generating first supplemental symbol decoding results applied to said second linear combiner as said respective first input signal thereof;

a two-input first multiplexer receiving said interim symbol decoding results as a first input signal thereto, receiving the output signal from said second linear combiner as a second input signal thereto, and reproducing as an output signal therefrom one of its said first and said second input signals as selected in response to a first multiplexer control signal;

a second delay device connected for delaying the output signal of said first multiplexer said prescribed first number of symbol epochs to generate said second input signal of said second linear combiner; and

symbol decoding selector circuitry for supplying final symbol decoding results, as selected from estimated

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symbol decoding results, said estimated symbol decoding results including said interim symbol decoding results and further including said output signal from said first multiplexer.

7. The combination of claim 6, wherein said prescribed first number of symbol epochs is six.

8. The combination of claim 6, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two horizontal scan lines of said co-channel interfering analog television signal.

9. The combination of claim 8, wherein said prescribed first number of symbol epochs is one thousand three hundred sixty-eight.

10. The combination of claim 6, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two hundred sixty-two horizontal scan lines of said co-channel interfering analog television signal.

11. The combination of claim 10, wherein said prescribed first number of symbol epochs is one hundred seventy-nine thousand two hundred eight.

12. The combination of claim 6, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two video frames of said co-channel interfering analog television signal.

13. The combination of claim 6, wherein said prescribed first number of symbol epochs is seven hundred eighteen thousand two hundred.

14. The combination of claim 6, further comprising:

a co-channel interference detector connected for generating an indication of when said stream of $2N$ -level symbols supplied from said digital television signal detection apparatus is accompanied by artifacts of co-channel interfering analog television signal that can be suppressed in said first comb filter response and that are of a significant energy level strong enough to interfere with said first data slicer decoding said stream of $2N$ -level symbols, said indication being supplied to said symbol decoding selector circuitry, said symbol decoding selector circuitry selecting said interim symbol decoding results as said final symbol decoding results only if said co-channel interference detector does not generate a current indication that said stream of $2N$ -level symbols supplied from said digital television signal detection apparatus is accompanied by said artifacts of co-channel interfering analog television signal that can be suppressed in said first comb filter response and that are of said significant energy level.

15. The combination of claim 6, further comprising:

a second delay device for exhibiting a delay of a prescribed second number of said symbol epochs, connected to respond to said stream of $2N$ -level symbols with a second delayed stream of $2N$ -level symbols, thereby to generate a second pair of differentially delayed streams of said $2N$ -level symbols;

a third linear combiner which linearly combines said second pair of differentially delayed streams of said $2N$ -level symbols susceptible to being accompanied by artifacts of co-channel interfering analog television signal, received as first and second respective input signals of said third linear combiner, to generate a second stream of $(4N-1)$ -level symbols as an output signal of said third linear combiner, said second stream of $(4N-1)$ -level symbols providing a second comb filter response in which said artifacts of co-channel interfering analog television signal are suppressed;

a fourth linear combiner which linearly combines respective first and second input signals received thereby for

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supplying a respective output signal therefrom, one of said third and said fourth linear combiners being an adder and the other of said first and said second linear combiners being a subtractor;

a third data slicer decoding said second stream of $(4N-1)$ -level symbols supplied as respective output signal from said third linear combiner, for generating second supplemental symbol decoding results applied to said fourth linear combiner as said respective first input signal thereof;

a two-input second multiplexer receiving said interim symbol decoding results as a first input signal thereto, receiving the output signal from said fourth linear combiner as a second input signal thereto, and reproducing as an output signal therefrom one of its said first and said second input signals as selected in response to a second multiplexer control signal, said output signal of said second multiplexer being supplied to said symbol decoding selector as a further one of said estimated symbol decoding results; and

a fourth delay device connected for delaying the output signal of said second multiplexer said prescribed second number of symbol epochs to generate said second input signal of said fourth linear combiner.

16. In combination:

digital television signal detection apparatus for supplying a stream of $2N$ -level symbols each having a symbol epoch of a specified length in time, which stream of $2N$ -level symbols is susceptible to being accompanied by artifacts of co-channel interfering analog television signal;

a first data slicer decoding said stream of $2N$ -level symbols for generating interim symbol decoding results;

a first delay device for exhibiting a delay of a prescribed first number of said symbol epochs, connected to respond to said stream of $2N$ -level symbols with a first delayed stream of $2N$ -level symbols, thereby to generate a pair of differentially delayed streams of said $2N$ -level symbols; and

an adder for adding said pair of differentially delayed streams of said $2N$ -level symbols susceptible to being accompanied by artifacts of co-channel interfering analog television signal, received as first and second respective input signals of said adder, for supplying as a sum output signal a stream of $(4N-1)$ -level symbols in which said accompanying artifacts of co-channel interfering analog television signal will be suppressed.

17. The combination of claim 16, wherein said prescribed first number of symbol epochs is six.

18. The combination of claim 16, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two horizontal scan lines of said co-channel interfering analog television signal.

19. The combination of claim 16, wherein said prescribed first number of symbol epochs is one-thousand three hundred sixty-eight.

20. The combination of claim 16, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two hundred sixty-two hori-

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zontal scan lines of said co-channel interfering analog television signal.

21. The combination of claim 16, wherein said prescribed first number of symbol epochs is one hundred seventy-nine thousand two hundred eight.

22. The combination of claim 16, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two video frames of said co-channel interfering analog television signal.

23. The combination of claim 16, wherein said prescribed first number of symbol epochs is seven hundred eighteen thousand two hundred.

24. The combination of claim 16, further comprising:

a subtractor for differentially combining in accordance with a modulo- $2N$ arithmetic respective first and second input signals received thereby for supplying a respective output signal therefrom;

a second data slicer decoding said stream of $(4N-1)$ -level symbols supplied as respective output signal from said adder, for generating first supplemental symbol decoding results applied to said subtractor as said first input signal thereof;

multiplexer circuitry reproducing as an output signal therefrom one of a plurality of input signals as selected in response to a multiplexer control signal, said multiplexer circuitry receiving said interim symbol decoding results as a first input signal thereto and receiving the output signal from said subtractor as a second input signal thereto, and the output signal from said multiplexer circuitry being used to provide final symbol decoding results; and

a second delay device connected for delaying the output signal of said multiplexer circuitry by said prescribed first number of symbol epochs to generate said second input signal of said subtractor.

25. The combination of claim 24, wherein said prescribed first number of symbol epochs is six.

26. The combination of claim 24, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two horizontal scan lines of said co-channel interfering analog television signal.

27. The combination of claim 24, wherein said prescribed first number of symbol epochs is one-thousand three hundred sixty-eight.

28. The combination of claim 24, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two hundred sixty-two horizontal scan lines of said co-channel interfering analog television signal.

29. The combination of claim 24, wherein said prescribed first number of symbol epochs is one hundred seventy-nine thousand two hundred eight.

30. The combination of claim 24, wherein said prescribed first number of symbol epochs is substantially equal to the number of symbol epochs in two video frames of said co-channel interfering analog television signal.

31. The combination of claim 24, wherein said prescribed first number of symbol epochs is seven hundred eighteen thousand two hundred.

* * * * *

PCT

CHAPTER II

DEMAND

under Article 31 of the Patent Cooperation Treaty.
The undersigned requests that the international application specified below be the subject of international preliminary examination according to the Patent Cooperation Treaty and hereby elects all eligible States (except where otherwise indicated).

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For International Preliminary Examining Authority use only			
Identification of IPEA		Date of receipt of DEMAND	
Box No. I IDENTIFICATION OF THE INTERNATIONAL APPLICATION		Applicant's or agent's file reference 29471/37034	
International application No. PCT/US01/09734	International filing date (day/month/year) 27 March 2001 (27.03.01)	(Earliest) Priority date (day/month/year) 18 April 2000 (18.04.00)	
Title of invention ENHANCED SLICE PREDICTION FEEDBACK			
Box No. II APPLICANT(S)			
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.) ZENITH ELECTRONICS CORPORATION 2000 Millbrook Drive Lincolnshire, Illinois 60069 United States of America		Telephone No. 847/841-8018	
		Facsimile No. 847/841-8003	
		Teleprinter No.	
		Applicant's registration No. with the Office	
State (that is, country) of nationality: US		State (that is, country) of residence: US	
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)			
State (that is, country) of nationality:		State (that is, country) of residence:	
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)			
State (that is, country) of nationality:		State (that is, country) of residence:	
☐ Further applicants are indicated on a continuation sheet.			

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Box No. III AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The following person is ☒ agent ☐ common representative
 and ☒ has been appointed earlier and represents the applicant(s) also for international preliminary examination.
☐ is hereby appointed and any earlier appointment of (an) agent(s) /common representative is hereby revoked.
☐ is hereby appointed, specifically for the procedure before the International Preliminary Examining Authority, in addition to the agent(s)/common representative appointed earlier.

Name and address: *(Family name followed by given name; for a legal entity, full official
The address must include postal code and name of country.)*

JOIKE, Trevor B.
 MARSHALL, GERSTEIN & BORUN
 6300 Sears Tower
 233 S. Wacker Drive
 Chicago, Illinois 60606
 United States of America

Telephone No.
312/474-6300

Facsimile No.
312/474-0448

Teleprinter No.

Agent's registration No. with the Office

☐ Address for correspondence: Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Box No. IV BASIS FOR INTERNATIONAL PRELIMINARY EXAMINATION**Statement concerning amendments:***

1. The applicant wishes the international preliminary examination to start on the basis of:

- ☒ the international application as originally filed.
- the description ☐ as originally filed
☐ as amended under Article 34
- the claims ☐ as originally filed
☐ as amended under Article 19 (together with any accompanying statement)
☐ as amended under Article 34
- the drawings ☐ as originally filed
☐ as amended under Article 34

2. ☐ The applicant wishes any amendment to the claims under Article 19 to be considered as reversed.

3. ☐ The applicant wishes the start of the international preliminary examination to be postponed until the expiration of 20 months from the priority date unless the International Preliminary Examining Authority receives a copy of any amendments made under Article 19 or a notice from the applicant that he does not wish to make such amendments (Rule 69.1(d)). *(This check-box may be marked only where the time limit under Article 19 has not yet expired.)*

* Where no check-box is marked, international preliminary examination will start on the basis of the international application as originally filed or, where a copy of amendments to the claims under Article 19 and/or amendments of the international application under Article 34 are received by the International Preliminary Examining Authority before it has begun to draw up a written opinion or the international preliminary examination report, as so amended.

Language for the purposes of international preliminary examination: English

- ☒ which is the language in which the international application was filed.
☐ which is the language of a translation furnished for the purposes of international search.
☐ which is the language of publication of the international application.
☐ which is the language of the translation (to be) furnished for the purposes of international preliminary examination.

Box No. V ELECTION OF STATES

The applicant hereby elects all eligible States *(that is, all States which have been designated and which are bound by Chapter II of the PCT)*

excluding the following States which the applicant wishes not to elect:

Box No. VI CHECK LIST

The demand is accompanied by the following elements, in the language referred to in Box No. IV, for the purposes of international preliminary examination:

- | | | |
|--|---|--------|
| 1. translation of international application | : | sheets |
| 2. amendments under Article 34 | : | sheets |
| 3. copy (or, where required, translation) of amendments under Article 19 | : | sheets |
| 4. copy (or, where required, translation) of statement under Article 19 | : | sheets |
| 5. letter | : | sheets |
| 6. other (specify) | : | sheets |

For International Preliminary Examining Authority use only

received not received

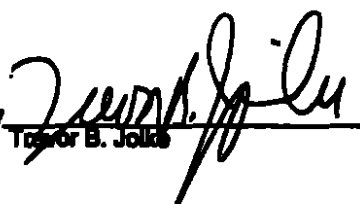
☐	☐
☐	☐
☐	☐
☐	☐
☐	☐
☐	☐

The demand is also accompanied by the item(s) marked below:

- | | |
|--|--|
| 1. ☒ fee calculation sheet | 5. ☐ statement explaining lack of signature |
| 2. ☐ original separate power of attorney | 6. ☐ sequence listing in computer readable form |
| 3. ☐ original general power of attorney | 7. ☐ other (specify): |
| 4. ☐ copy of general power of attorney; reference number, if any: | |

Box No. VII SIGNATURE OF APPLICANT, AGENT OR COMMON REPRESENTATIVE

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the demand).

By  Date 05 Oct 2001
Thomas B. Jolke

For International Preliminary Examining Authority use only

1. Date of actual receipt of DEMAND:

2. Adjusted date of receipt of demand due to CORRECTIONS under Rule 60.1(b):

3. ☐ The date of receipt of the demand is AFTER the expiration of 19 months from the priority date and item 4 or 5, below, does not apply.

☐ The applicant has been informed accordingly.

4. ☐ The date of receipt of the demand is WITHIN the period of 19 months from the priority date as extended by virtue of Rule 80.5.

5. ☐ Although the date of receipt of the demand is after the expiration of 19 months from the priority date, the delay in arrival is EXCUSED pursuant to Rule 82.

For International Bureau use only

Demand received from IPEA on:

PCT

FEE CALCULATION SHEET

Annex to the Demand

372

<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">International application No.</td> <td>PCT/US01/09734</td> </tr> <tr> <td>Applicant's or agent's file reference</td> <td>29471/37034</td> </tr> </table>	International application No.	PCT/US01/09734	Applicant's or agent's file reference	29471/37034	For International Preliminary Examining Authority use only Date stamp of the IPEA
International application No.	PCT/US01/09734				
Applicant's or agent's file reference	29471/37034				
Applicant ZENITH ELECTRONICS CORPORATION					
CALCULATION OF PRESCRIBED FEES					
1. Preliminary examination fee	2,998.29 P				
2. Handling fee <i>(Applicants from certain States are entitled to a reduction of 75% of the handling fee. Where the applicant is (or all applicants are) so entitled, the amount to be entered at H is 25% of the handling fee.)</i>	287.81 H				
3. Total of prescribed fees Add the amounts entered at P and H and enter total in the TOTAL box	3,286.10 TOTAL				
MODE OF PAYMENT					
☒ authorization to charge deposit account with the IPEA (see below)	☐ cash				
☐ cheque	☐ revenue stamps				
☐ postal money order	☐ coupons				
☐ bank draft	☐ other (specify):				
AUTHORIZATION TO CHARGE (OR CREDIT) DEPOSIT ACCOUNT <i>(This mode of payment may not be available at all IPEAs)</i>					
☒ Authorization to charge the total fees indicated above.	IPEA/ <u>EP</u>				
☒ <i>(This check-box may be marked only if the conditions for deposit accounts of the IPEA so permit) Authorization to charge any deficiency or credit any overpayment in the total fees indicated above.</i>	Deposit Account No.: <u>28300287</u>				
	Date: <u>05 Oct 2001</u>				
	Name: <u>Trevor B. Jolke</u>				
	Signature: <u><i>Trevor B. Jolke</i></u>				

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

PCT

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To:

JOIKE, Trevor B.
MARSHALL, GERSTEIN & BORUN
6300 Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
ETATS-UNIS D'AMERIQUE

NOTIFICATION OF RECEIPT
OF DEMAND BY COMPETENT INTERNATIONAL
PRELIMINARY EXAMINING AUTHORITY(PCT Rules 59.3(e) and 61.1(b), first sentence
and Administrative Instructions, Section 601(a))RECEIVED
OCT 23
MARSHALL GERSTEINDate of mailing
(day/month/year)

16. 10. 01

Applicant's or agent's file reference
29471/37034

IMPORTANT NOTIFICATION

International application No.

PCT/US 01/ 09734

International filing date (day/month/year)

27/03/2001

Priority date (day/month/year)

18/04/2000

Applicant

ZENITH ELECTRONICS CORPORATION

1. The applicant is hereby notified that this International Preliminary Examining Authority considers the following date as the date of receipt of the demand for international preliminary examination of the international application:

05/10/2001

2. This date of receipt is:

- ☒ the actual date of receipt of the demand by this Authority (Rule 61.1(b)).
☐ the actual date of receipt of the demand on behalf of this Authority (Rule 59.3(e)).
☐ the date on which this Authority has, in response to the invitation to correct defects in the demand (Form PCT/IPEA/404), received the required corrections.

3. ☐ ATTENTION: That date of receipt is AFTER the expiration of 19 months from the priority date. Consequently, the election(s) made in the demand does (do) not have the effect of postponing the entry into the national phase until 30 months from the priority date (or later in some Offices) (Article 39(1)). Therefore, the acts for entry into the national phase must be performed within 20 months from the priority date (or later in some Offices) (Article 22). For details, see the PCT Applicant's Guide, Volume II.

- ☐ (If applicable) This notification confirms the information given by telephone, facsimile transmission or in person on:

4. Only where paragraph 3 applies, a copy of this notification has been sent to the International Bureau.

Name and mailing address of the IPEA/



European Patent Office
D-80298 Munich
Tel. (+49-89) 2399-0, Tx: 523656 epmu d
Fax: (+49-89) 2399-4465

Authorized officer

AIMELE MURILLO J

Tel. (+49-89) 2399-8039



PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

- Fax nr: 312-474-0448

- 5 pages -

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To:

JOIKE, Trevor B.
MARSHALL, GERSTEIN & BORUN
6300 Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
ETATS-UNIS D'AMERIQUE

**Confirmation
FAX-Bestätigung**

PCT

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL PRELIMINARY
EXAMINATION REPORT
(PCT Rule 71.1)

RECEIVED

JUL 17 2002

Date of mailing (day/month/year)	11.07.2002
-------------------------------------	------------

Applicant's or agent's file reference 29471/37034	MARSHALL GERSTEIN	IMPORTANT NOTIFICATION
International application No. PCT/US01/09734	International filing date (day/month/year) 27/03/2001	Priority date (day/month/year) 18/04/2000
Applicant ZENITH ELECTRONICS CORPORATION		

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the International preliminary examination report and its annexes, if any, established on the international application.
2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.
3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.
4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

For the purpose of deciding whether the claimed invention is patentable or not, the elected Offices may apply criteria additional to or different from the criteria on which the international preliminary examination report is based (see Articles 27(5), 33(5)). Additional criteria may include e.g. exemptions from patentability and the requirements of enabling disclosure and of clarity and support of claims.

Name and mailing address of the IPEA/  European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tlx 523056 epmu d Fax: +49 89 2399 - 4465	Authorized officer Barrio Baranano, A Tel. +49 89 2399-8821
--	--



PATENT COOPERATION TREATY

375 10
RECEIVED

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

PCT

04 2002

SCHIFF HARDIN & WAITE
US PATENT OFFICE

WRITTEN OPINION

(PCT Rule 66)

To:

JOIKE, Trevor B.
MARSHALL, GERSTEIN & BORUN
6300 Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
ETATS-UNIS D'AMERIQUE

Date of mailing
(day/month/year)

24/01/2002

Applicant's or agent's file reference

29471/37034

REPLY DUE

within 1 / 00 months/days
from the above date of mailing

International application No.

PGT/US 01/09734

International filing date (day/month/year)

27/03/2001

Priority date (day/month/year)

18/04/2000

International Patent Classification (IPC) or both national classification and IPC

H04L27/02

Applicant

ZENITH ELECTRONICS CORPORATION

1. This written opinion is the first drawn up by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

- I ☒ Basis of the opinion
- II ☐ Priority
- III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Rule 66.2(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

3. The applicant is hereby invited to reply to this opinion.

When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also For an additional opportunity to submit amendments, see Rule 66.4. For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4bis. For an informal communication with the examiner, see Rule 66.5.

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 18/08/2002.

Name and mailing address of the IPEA/

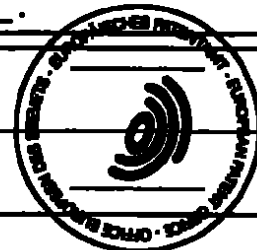


European Patent Office
D-80298 Munich
Tel. (+49-89) 2399-0, Tx: 523656 epmu d
Fax: (+49-89) 2399-4465

Authorized officer

Examiner

Formalities officer
(incl. extension of time limits)
Tel. (+49-89) 2399 2828



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I. Basis of the opinion

1. The basis of this written opinion is the application as originally filed.

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

2. The question of whether the claimed invention appears to be novel, to involve an inventive step, or to be industrially applicable has not been and will not be the subject of the international preliminary examination (Article 34 (4) (a) (i) (ii) PCT; see also international search report) in respect of:

- 2.1 Applications having an unnecessary plurality of independent claims (generally not more than 1 independent claim in the same category is necessary; Article 6 PCT);

- 2.2 unsearched subject-matter (Article 17 (2) (a), Rule 66.1 (e) PCT), e.g.

- 2.2.1 claimed subject-matter under Rule 39.1 PCT,

- 2.2.2 applications where the description, the claims, or the drawings fail to comply with the prescribed requirements to such an extent that no meaningful search could have been carried out;

- 2.3 claimed subject-matter under Rule 67.1 PCT.

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability

3. To the extent that the international preliminary examination has been carried out (see item III above), the following is pointed out:

In light of the documents cited in the international search report, it is considered that the invention as claimed in at least one of the independent claims does not appear to meet the criteria mentioned in Article 33 (1) PCT, i.e. does not appear to be novel and/or to involve an inventive step.

4. If amendments are filed, the Applicant must comply with the requirements of Rule 66.8 PCT and indicate the basis in the originally filed application of the amendments made (Article 34 (2) (b) PCT) otherwise these amendments will not be taken into consideration for the establishment of international preliminary examination.
The attention of the applicant is drawn to the fact that if the application contains an unjustified plurality of independent claims no examination of any of the claims will be carried out.

• • **SCHIFF HARDIN & WAITE**

• A Partnership Including Professional Corporations

• • 6800 Sears Tower, Chicago, Illinois 60606-6473
Telephone (312) 258-5500 Facsimile (312) 258-5700

Chicago
Washington
New York
Merrillville
Dublin

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February 11, 2002

VIA TELEFAX

European Patent Office /IPEA
Erhardtstrasse 27
D-80331 Muenchen
Germany

RE: PCT International Application No. PCT/US01/09734
Zenith Electronics Corporation
Our Ref. No. FP01,0519WO (formerly 29471/37034)

Dear Ladies and Gentlemen:

The Examiner in the above captioned application has refused to exam the application, citing several PCT Articles and Rules. Applicant requests clarification for the reasons given below.

First, the examiner asserted that there are too many independent claims, citing Article 6. Article 6 essentially states that the claims shall define the invention, shall be clear and concise, and shall be fully supported by the description. Because there is only one independent claim in each application, because the claims define the invention, because the claims are clear and concise, and because the claims are fully supported by the description, applicant has complied with this article.

Second, the examiner asserts that the subject matter is unsearched, citing PCT Article 17(2)(a) and Rule 66.1(e). Article 17(2)(a) essentially provides that, if the examination authority considers that (i) the application relates to subject matter which the searching authority is not required to search and decides not to search or (ii) the description, drawings, or claims cannot support a meaningful search, then no search will be established. Neither of these sections applies since applicant has already received a search report. Rule 66.1(e) states that claims relating to subject for which no international search report has been established need not be examined. However, an international search report has been issued.

February 11, 2002
Page 2

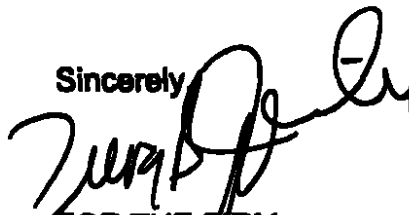
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Third, the examiner asserts that there is claimed subject matter under PCT Rule 39.1. This rule essentially provides that a search need not be conducted if the subject matter of the application relates to (i) scientific or mathematical theories, (ii) plants or animals, (iii) methods of doing business, (iv) medical treatments, (v) mere presentations of information, or (vi) computer programs. Again, none of these sections apply since applicant has already received an international search report. Also, it is hard to see how the items listed in this rule apply to the claims.

Fourth, the examiner essentially repeats a portion of Article 17(2)(a) which has been discussed above.

Fifth, the examiner asserts that there is claimed subject matter under PCT Rule 67.1. This rule is not very different from PCT Rule 39.1, which has been discussed above.

Accordingly, applicant has difficulty in understanding the Written Opinion mailed January 24, 2002 and asks for a clarification.

Sincerely

FOR THE FIRM
Trevor B. Jolke

TBJ/edr

PATENT COOPERATION TREATY

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From the:
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

- Fax nr: 312-474-0448

- 5 pages -

PCT 379

To:

JOIKE, Trevor B.
MARSHALL, GERSTEIN & BORUN
6300 Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
ETATS-UNIS D'AMERIQUE

Confirmation
FAX-Bestätigung

WRITTEN OPINION

(PCT Rule 66)

RECEIVED

MAY 21 2002

Date of mailing
(day/month/year)

14.05.2002

Applicant's or agent's file reference
29471/37034

REPLY DUE

within 1 month(s)
from the above date of mailing

International application No.
PCT/US01/09734

International filing date (day/month/year)
27/03/2001

Priority date (day/month/year)
18/04/2000

International Patent Classification (IPC) or both national classification and IPC

H04L27/02

Applicant

ZENITH ELECTRONICS CORPORATION

1. This written opinion is the second drawn up by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

- I ☒ Basis of the opinion
- II ☐ Priority
- III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☐ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain document cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

3. The applicant is hereby invited to reply to this opinion.

When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also: For an additional opportunity to submit amendments, see Rule 66.4. For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 bis. For an informal communication with the examiner, see Rule 66.6.

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 66.2 is: 18/08/2002.

Name and mailing address of the international preliminary examining authority:

 European Patent Office
D-80298 Munich
Tel. +49 89 2399 - 0 Tx: 523656 epmu d
Fax: +49 89 2399 - 4485

Authorized officer / Examiner

Snell, T

Formalities officer (incl. extension of time limits)
Barrio Baranano, A
Telephone No. +49 89 2399 8821



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I. Basis of the opinion

1. With regard to the elements of the international application (Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed").

Description, pages:

1-45 as originally filed

Claims, No.:

1-19 as originally filed

Drawings, sheets:

1/12-12/12 as originally filed

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
☐ the language of publication of the international application (under Rule 48.3(b)).
☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
☐ filed together with the international application in computer readable form.
☐ furnished subsequently to this Authority in written form.
☐ furnished subsequently to this Authority in computer readable form.
☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
☐ the claims, Nos.:

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☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been and will not be examined in respect of:

☐ the entire international application,

☒ claims Nos. 1-19,

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (*specify*):

☒ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. 1-19 are so unclear that no meaningful opinion could be formed (*specify*):
see separate sheet

☒ the claims, or said claims Nos. 1-19 are so inadequately supported by the description that no meaningful opinion could be formed.

☐ no international search report has been established for the said claims Nos. .

2. A written opinion cannot be drawn due to the failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

☐ the written form has not been furnished or does not comply with the standard.

☐ the computer readable form has not been furnished or does not comply with the standard.

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Re Item III

Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The formulation of claim 1 is currently too obscure and lacking support in the description to enable a meaningful opinion as to novelty and inventive step to be formed, for the following reasons (Article 6 PCT).
 - (i) It is not clear what should be understood by the terms "first and second data" in the context of the embodiments described (for example, this could relate to data decoded by the inner and outer decoders, or to data from different sources, eg video and auxiliary data (cf fig. 3 "Discard:")).
 - (ii) Furthermore, there is no apparent support in the description for their having different bit rates, since the input signal contains data at a particular single symbol rate.
 - (iii) It is unclear what the purpose of the "first data" is, since they play no role in the method as currently claimed.
 - (iv) The feature "In response to the input and the decoder" is not clear or supported by the description; the embodiment of claim 1 appears to be based on figure 19, but this embodiment does not show the prediction enhancer as being responsive to the input signal. Moreover it is not clear which decoder is referred to.
2. It is suggested to file a new method claim 1 based on the matter described on page 4, lines 1 to 15 of the description and figure 19. The dependent claims should be adapted accordingly.
3. As claims 2-19 are dependent on claim 1, they suffer from the same objection of lack of clarity and support as claim 1 (Article 6 PCT).
4. The description should be adapted to any new claims (Rule 5.1(a)(iii) PCT).
5. In order to facilitate the examination of the conformity of the amended application

**WRITTEN OPINION
SEPARATE SHEET**

International application No. PCT/US01/09734

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with the requirements of Article 19(2) PCT, the applicant is requested to clearly identify the amendments carried out, irrespective of whether they concern amendments by addition, replacement or deletion, and to indicate the passages of the application as filed on which these amendments are based.

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 October 2001 (25.10.2001)

PCT

(10) International Publication Number
WO 01/78495 A3

(51) International Patent Classification: H04L 27/02, 27/06, 25/06, H04N 7/66, 7/52, 5/00

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(21) International Application Number: PCT/US01/09734

(22) International Filing Date: 27 March 2001 (27.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/198,014 18 April 2000 (18.04.2000) US
60/255,476 13 December 2000 (13.12.2000) US
60/255,464 13 December 2000 (13.12.2000) US
09/804,237 13 March 2001 (13.03.2001) US

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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Published:
— with international search report

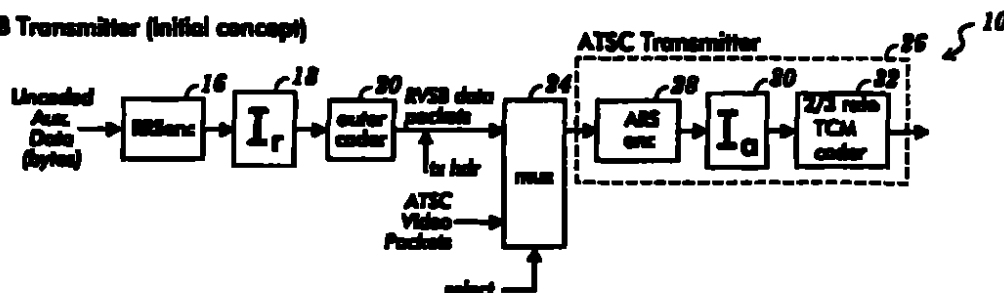
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(88) Date of publication of the international search report:
28 March 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MODULATION SELECTION AND DECODING

KVSB Transmitter (Initial concept)



(57) Abstract: Enhanced slice prediction is based upon ATSC 8 VSB data when robust 8 VSB data are not available and is based upon robust 8 VSB data when robust 8 VSB data are available.

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/09734

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04L27/02 H04L27/06 H04L25/06 H04N7/66 H04N7/52
H04N5/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04L H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
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A		2-19
Y	US 5 923 711 A (WILLMING DAVID A) 13 July 1999 (1999-07-13) abstract column 1 column 2 claims 1,2 figure 4	1
A		2-19
	-/-	



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

30 October 2001

Date of mailing of the international search report

07/11/2001

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INTERNATIONAL SEARCH REPORT

Int. Appl. No. PCT/US 01/09734

International Application No.

PCT/US 01/09734

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