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51. **CLASIFICACION INTERNACIONAL**

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1 SOLICITUD DE:

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2 SOLICITANTE (71)	Nombre: **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** Dirección: Hewlett-Packard Company, Intellectual Property Administration, 20555 S.H. 249, Houston, Texas 77070, Estados Unidos de América Nacionalidad o Domicilio: Estados Unidos de América Lugar de Constitución: Estados Unidos de América Teléfono: Fax: E-mail	**IDENTIFICACIÓN** C.C. ☐ NIT ☐ C.E. ☐ Otro ☐ Cual_____ Número _____
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10 **ANEXOS**

- [x] Comprobante de pago de la tasa de presentación de la solicitud. $ 501.000
- [x] Documento que acredita la existencia y representación legal cuando el solicitante sea persona jurídica.
- [x] Poderes, si fuere el caso. **Fotocopia autenticada**
- [ ] Documento de cesión del inventor al solicitante o a su causante.
- [ ] Declaraciones.
- [x] Copia de la solicitud internacional. (Resumen, descripción, reivindicaciones, dibujos)
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- [ ] Copia del examen preliminar efectuado por la IPEA.
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- [ ] De ser el caso, información sobre otras solicitudes de patente o títulos obtenidos en el extranjero por el mismo titular o su causante, relacionadas parcial o totalmente con la invención de esta solicitud.
- [x] Otros: Tarjeta de Propietarios
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11 FIGURA CARACTERÍSTICA:

12 Solicito la concesión de la patente,

NOMBRE: JUAN PABLO CADENA SARMIENTO

FIRMA: _____

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Declarations under Rule 4.17:
— *as to the identity of the inventor (Rule 4.17(i))*
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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(54) Title: GATE-COUPLED EPROM CELL FOR PRINTHEAD

(57) Abstract: An EPROM cell (270) in a printhead control circuit for an inkjet printer, having exactly one polysilicon layer (256) and a conductive layer (260) disposed above the polysilicon layer, includes a control transistor (272) and an EPROM transistor (274). The control and EPROM transistors each have floating gates (280, 282) comprising a portion of the polysilicon layer (256), and an electrical interconnection, comprising a portion of the conductive layer (260), interconnects the floating gate (280) of the control transistor (272) and the floating gate (282) of the EPROM transistor (274).

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GATE-COUPLED EPROM CELL FOR PRINTHEAD

BACKGROUND

An inkjet printing system is a type of fluid ejection device, and includes a printhead, an ink supply, and an electronic controller that controls the printhead. The printhead ejects liquid ink drops through an array of orifices or nozzles disposed in a die by rapidly heating small volumes of ink located in vaporization chambers. The ink is heated with small electric heaters, such as thin film resistors or firing resistors. Heating the ink causes a portion of the liquid ink to vaporize and thereby eject a single drop through the nozzle toward a sheet of print medium, such as a sheet of paper, to print an image. The ink nozzles are typically arranged in one or more arrays in the printhead die, such that properly sequenced ejection of ink from the nozzles causes characters or other images to be printed as the printhead scans across the print medium.

To eject each drop of ink, the electronic controller that controls the printhead activates an electrical current from a power supply external to the printhead. The electrical current passes through a selected firing resistor to heat the ink in a corresponding selected vaporization chamber and eject the ink through a corresponding nozzle. Known drop generators include a firing resistor, a corresponding vaporization chamber, and a corresponding nozzle.

In inkjet printing systems it is desirable to have several characteristics of each print cartridge easily identifiable by a controller, and it is desirable to have such identification information supplied directly by the print cartridge. This "identification information" can provide information to the controller to adjust the operation of the printer and ensure correct operation. Additionally, as the different types of fluid ejection devices and their operating parameters increase,

there is a need to provide a greater amount of identification information without adding further interconnections to the flex tab circuit or increasing the size of the die to provide such identification information.

For these and other reasons, pen identification cells have been developed and integrated with the circuitry of inkjet printhead dies. In one configuration, the printhead circuitry is a negative-channel metal-oxide semiconductor (NMOS) circuit, and the identification cells are configured to be addressed individually. Each identification cell includes an identification bit that stores one bit of information.

The identification bits of the identification cells typically employ fuses and, though they are different from standard programmable read-only memory (PROM) chips, these bits are programmed and used in basically the same way. To program the chip, a relatively high current is selectively routed to certain fuses to cause them to burn out. Bits where fuses remain have a value of 1, while those where the fuses have been burned out provide a value of 0 in the binary logic of the circuit.

Programming and using ROM chips in this way has some drawbacks. If a chip is improperly programmed initially, there is no way to fix it, and the chip must be discarded. Additionally, fuses are relatively large, and can be unreliable. In inkjet printhead circuits, for example, fuses can damage the inkjet orifice layer during programming, and after a fuse burns out, metal debris from the fuse can be drawn into the ink and cause blockage in a pen, or result in poor quality printing.

In recent years, electronically programmable read-only memory (EPROM) devices have also been developed. Unlike PROM chips, EPROM chips do not include fuses. Like typical ROM chips, EPROMs include a conductive grid of columns and rows. The cell at each intersection has two gates that are separated from each other by a thin oxide layer that acts as a dielectric. One of the gates is called a floating gate and the other is called a control gate or input gate. The floating gate's only link to the row is through the control gate. A blank EPROM has all of the gates fully open, giving each cell a

value of 1. That is, the floating gate initially has no charge, which causes the threshold voltage to be low.

To change the value of the bit to 0, a programming voltage (e.g. 10 to 16 volts) is applied to the control gate and drain. This programming voltage draws excited electrons to the floating gate, thereby increasing the threshold voltage. The excited electrons are pushed through and trapped on the other side of the thin oxide layer, giving it a negative charge. These negatively charged electrons act as a barrier between the control gate and the floating gate. During use of the EPROM cell, a cell sensor monitors the threshold voltage of the cell. If the threshold voltage is low (below the threshold level), the cell has a value of 1. If the threshold voltage is high (above the threshold level), the cell has a value of zero.

Because EPROM cells have two gates at each intersection, an EPROM chip requires additional layers compared to a standard NMOS or PROM chip, including many such chips that are frequently used in inkjet printhead circuits. Consequently, while some of the drawbacks of fuses in NMOS circuits could be eliminated by the application of EPROM circuitry, the use of a typical EPROM cell either requires that the chip be provided with additional layers, which increases the cost and complexity of the chip, or that a separate EPROM chip be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Various features and advantages of the invention will be apparent from the detailed description which follows, taken in conjunction with the accompanying drawings, which together illustrate, by way of example, features of the invention, and wherein:

FIG. 1 is a block diagram of one embodiment of an ink jet printing system;

FIG. 2 is a diagram illustrating a portion of one embodiment of a printhead die;

FIG. 3 is a schematic diagram illustrating one embodiment of an ink jet printhead firing cell array;

FIG. 4 is a schematic diagram of one embodiment of an identification cell in one embodiment of a printhead die;

FIG. 5 is a schematic diagram of a typical EPROM transistor;

FIG. 6 is a cross-sectional view showing the circuitry layers in a typical EPROM chip;

FIG. 7 is a cross-sectional view showing the layers in one embodiment of an ink jet printhead die providing the circuitry shown in FIG. 3;

FIG. 8 is a schematic diagram of one embodiment of a gate-coupled EPROM cell that can be adapted for use as an identification bit in the printhead circuitry of FIG. 4;

FIG. 9 is a schematic diagram of one embodiment of an identification cell having a gate-coupled EPROM identification bit; and

FIG. 10 is a schematic diagram of an array of gate-coupled EPROM cells for a printhead circuit.

DETAILED DESCRIPTION

Reference will now be made to exemplary embodiments illustrated in the drawings, and specific language will be used herein to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended. Alterations and further modifications of the inventive features illustrated herein, and additional applications of the principles of the invention as illustrated herein, which would occur to one skilled in the relevant art and having possession of this disclosure, are to be considered within the scope of the invention.

Shown in FIG. 1 is a block diagram of one embodiment of an inkjet printing system 20. The inkjet printing system generally includes an inkjet printhead assembly 22, and a fluid supply assembly, such as the ink supply assembly 24. The inkjet printing system also includes a mounting assembly 26, a media transport assembly 28, and an electronic controller 30. A power supply 32 provides power to the various electrical components of the system.

In the embodiment shown in FIG. 1, the inkjet printhead assembly 22 includes at least one printhead or printhead die 40 that ejects drops of ink

through a plurality of orifices or nozzles 34 toward a print medium 36, so as to print onto the print medium. The print medium can be any type of suitable sheet material, such as paper, card stock, transparencies, Mylar®, fabric, and the like. Typically, the nozzles 34 are arranged in one or more columns or arrays such that properly sequenced ejection of ink from the nozzles causes characters, symbols, and/or other graphics or images to be printed upon print medium as the inkjet printhead assembly and print medium are moved relative to each other. The printhead 40 is one embodiment of a fluid ejection device. While the following description refers to the ejection of ink from the printhead assembly 22, it is to be understood that other liquids, fluids or flowable materials, including clear fluid, may be ejected from the printhead assembly.

The ink supply assembly 24 is one embodiment of a fluid supply assembly, and provides ink to the printhead assembly 22. The ink supply assembly includes a reservoir 38 for storing ink, which flows from the reservoir to the inkjet printhead assembly. The ink supply assembly and inkjet printhead assembly can form either a one-way ink delivery system or a recirculating ink delivery system. In a one-way ink delivery system, substantially all of the ink provided to the inkjet printhead assembly is consumed during printing. In a recirculating ink delivery system, only a portion of the ink provided to the printhead assembly is consumed during printing. In such a system, ink not consumed during printing is returned to the ink supply assembly.

In one embodiment of an inkjet printing system, the inkjet printhead assembly 22 and ink supply assembly 24 are housed together in an inkjet cartridge or pen. Alternatively, the ink supply assembly can be separate from the inkjet printhead assembly, and provide ink to the inkjet printhead assembly through an interface connection, such as a supply tube (not shown). In either embodiment, the reservoir 38 can be removed, replaced, and/or refilled.

The mounting assembly 26 positions the inkjet printhead assembly 22 relative to the media transport assembly 28, which positions the print medium 36 relative to the inkjet printhead assembly. A print zone 37 is thus defined adjacent to the nozzles 34 in an area between the inkjet printhead assembly and the print medium. The inkjet printhead assembly can be a scanning type

printhead assembly, wherein the mounting assembly includes a carriage (not shown) for moving the inkjet printhead assembly relative to the media transport assembly to scan the print medium. Alternatively, the inkjet printhead assembly can be a non-scanning type printhead assembly, wherein the mounting assembly fixes the inkjet printhead assembly at a prescribed position relative to the media transport assembly 28.

The electronic controller or printer controller 30 typically includes a processor, firmware, and other electronics, or any combination thereof, for communicating with and controlling the inkjet printhead assembly 22, the mounting assembly 26, and the media transport assembly 28. The electronic controller receives data 39 from a host system, such as a computer, and usually includes memory (not shown) for temporarily storing the data. Typically, the data is sent to the inkjet printing system 20 along an electronic, infrared, optical, or other information transfer path. The data represents, for example, a document to be printed, and includes one or more print job commands and/or command parameters, thereby forming a print job for the inkjet printing system. The pattern of ejected ink drops is determined by the print job commands and/or command parameters.

The inkjet printhead assembly 22 can include one printhead 40, or it can be a wide-array or multi-head printhead assembly. The inkjet printhead assembly can include a carrier, which carries the printhead dies, provides electrical communication between the printhead dies and electronic controller 30, and provides fluidic communication between the printhead dies and the ink supply assembly 24.

Provided in FIG. 2 is a diagram illustrating a portion of one embodiment of a printhead die 40. The printhead die includes an array of printing or fluid ejecting elements 42. The printing elements are formed on a substrate 44, which has an ink feed slot 46 formed therein. The ink feed slot provides a supply of liquid ink to the printing elements, and is one embodiment of a fluid feed source. Other embodiments of fluid feed sources include but are not limited to corresponding individual ink feed holes feeding corresponding

vaporization chambers and multiple shorter ink feed trenches that each feed corresponding groups of fluid ejecting elements.

A thin-film structure 48 is provided with an ink feed channel 54 formed therein. This channel communicates with the ink feed slot 46 formed in the substrate 44. An orifice layer 50 has a front face 50a and a nozzle opening 34 formed in the front face. The orifice layer also has a nozzle chamber or vaporization chamber 56 formed therein, which communicates with the nozzle opening and the ink feed channel of the thin-film structure. A firing resistor 52 is positioned within the vaporization chamber, and conductive leads 58 electrically couple this firing resistor to circuitry controlling the application of electrical current through selected firing resistors. As used herein, the term "drop generator" 60 includes the firing resistor 52, the nozzle chamber or vaporization chamber 56 and the nozzle opening 34.

During printing, ink flows from the ink feed slot 46 to the vaporization chamber 56 via the ink feed channel 54. The nozzle opening 34 is operatively associated with the firing resistor 52, such that droplets of ink within the vaporization chamber are ejected through the nozzle opening (e.g., substantially normal to the plane of the firing resistor) and toward the print medium 36 upon energizing of the firing resistor.

There are a variety of types of printhead dies. These include thermal printheads, piezoelectric printheads, electrostatic printheads, and any other type of fluid ejection device known in the art that can be integrated into a multi-layer structure. The substrate 44 can be formed, for example, of silicon, glass, ceramic, or a stable polymer, and the thin-film structure 48 can be formed to include one or more passivation or insulation layers of silicon dioxide, silicon carbide, silicon nitride, tantalum, polysilicon glass, or other suitable material. The thin-film structure also includes at least one conductive layer, which defines the firing resistor 52 and leads 58. The conductive layer can be made of, for example, aluminum, silver, gold, tantalum, tantalum-aluminum, or other metal or metal alloy. Firing cell circuitry, such as described in detail below, can be implemented in the substrate and thin-film layers.

The orifice layer 50 can be of a photoimageable epoxy resin, such as an epoxy referred to as SU8, marketed by Micro-Chem, of Newton, Massachusetts. Techniques for fabricating the orifice layer with SU8 or other polymers are well known to those of skill in the art. In one embodiment, the orifice layer is formed of two separate layers, referred to as a barrier layer (e.g., a dry film photo resist barrier layer) and a metal orifice layer (e.g., a nickel, copper, iron/nickel alloys, palladium, gold, or rhodium layer) formed over the barrier layer. Other suitable materials can also be employed to form the orifice layer.

Shown in FIG. 3 is a schematic diagram of a portion of one embodiment of an inkjet printhead firing cell circuit 80. The firing cell circuit includes a plurality of fire groups 82 (e.g. six fire groups), each fire group comprising an array of pre-charged firing cells 84. A first fire group 82a and a portion of a second fire group 82b are shown in FIG. 3. The pre-charged firing cells in each fire group are schematically arranged into 13 rows and eight columns. The number of pre-charged firing cells and their layout may vary as desired.

The eight columns of pre-charged firing cells 84 are electrically coupled to eight data lines 88, labeled D1-D8. Each of the firing cells in each column of pre-charged firing cells is electrically coupled to one of the data lines, and these data lines extend to the corresponding columns of pre-charged firing cells in fire group 82b and subsequent fire groups (not shown).

The rows of pre-charged firing cells 84 are electrically coupled to address lines 86, labeled A1-A7, that receive address signals. Each pre-charged firing cell in a row of pre-charged firing cells, referred to herein as a row subgroup or subgroup, is electrically coupled to the same pair of the address lines, this pair being unique for each row subgroup. The array of firing cells shown in the fire group 82 includes 13 row subgroups, but it will be apparent that the array can include any suitable number of subgroups. The address lines also extend to connect with row subgroups of fire group 82b and subsequent fire groups (not shown).

The pre-charge line 90a (labeled PRE 1) receives a pre-charge signal, and provides the pre-charge signal to all of the pre-charged firing cells 84 in the

first fire group 82a. Additional fire groups each have a separate pre-charge line, such as pre-charge line 90b (labeled PRE2) for fire group 82b.

A select line 92a (labeled SEL 1) receives a select signal and provides this select signal to all firing cells 84 in a corresponding fire group 82 and a fire line 94a (labeled FIRE 1) provides a fire signal to all pre-charged firing cells in the associated fire group. The fire line is electrically coupled to the firing resistors (52 in FIG. 2) of all pre-charged firing cells 84 in one fire group. Additional fire groups each have their own separate select and fire lines.

Additionally, all pre-charged firing cells 84 in the array 80 are electrically coupled to a reference line 96 that is tied to a reference voltage, such as ground. Given this structure, the pre-charged firing cells in a row subgroup of pre-charged firing cells are electrically coupled to the same address lines 86, pre-charge line 90, select line 92, fire line 94, and ground line 96.

The firing cells 84 cause the individual firing resistors (52 in FIG. 2) of the ink nozzles to selectively operate, so as to eject ink in the desired pattern. The fire groups are first precharged through the respective PRE lines 90. Address signals are provided on the address lines 86 to address one row subgroup in each of the fire groups 82, including one row subgroup in the pre-charged fire group. Data signals are provided on data lines 88 to provide data to all fire groups, including the addressed row subgroup in the pre-charged fire group. Next, a select signal is provided on the select line 92 of the pre-charged fire group to select the pre-charged fire group. The select signal defines a discharge time interval for discharging the node capacitance on each drive switch (not shown) in a pre-charged firing cell that is either not in the addressed row subgroup in the selected fire group or addressed in the selected fire group and receiving a high level data signal. The node capacitance does not discharge in pre-charged firing cells that are addressed in the selected fire group and receiving a low-level data signal. A high voltage level on the node capacitance turns the drive switch on (conducting).

After drive switches in the selected fire group 82 are set to conduct or not conduct, an energy pulse or voltage pulse is provided on the fire line 94 of the selected fire group. Pre-charged firing cells 84 that have conducting drive

switches conduct current through the firing resistor (52 in FIG. 2) to heat ink and eject ink from the corresponding drop generator (60 in FIG. 2). In operation, the plurality of fire groups 82 can be selected to fire in succession, or other sequences, and non-sequential selections may also be utilized. The address signals provided on the address lines 86 can be set to one row subgroup address during each cycle through the fire groups, and thereby cycle through the 13 row subgroup addresses in each fire group before repeating a row subgroup address. After the last row subgroup, address signals select the first row subgroup to begin the address cycle over again.

With fire groups 82 operated in succession, the select signal for one fire group is used as the pre-charge signal for the next fire group. The pre-charge signal for one fire group precedes the select signal and fire signal for the one fire group. After the pre-charge signal, data signals are multiplexed in time and stored in the addressed row subgroup of the one fire group by the select signal. The select signal for the selected fire group is also the pre-charge signal for the next fire group. After the select signal for the selected fire group is complete, the select signal for the next fire group is provided. Pre-charged firing cells 84 in the selected subgroup fire or heat ink based on the stored data signal as the fire signal, including an energy pulse, is provided to the selected fire group.

As noted above, it can be desirable to provide a greater amount of identification information in the printhead circuit, without adding further interconnections to the flex tab circuit or increasing the size of the die to provide such identification information. Accordingly, identification cells have been developed that can be included in the printhead circuitry, such as that shown in FIG. 3. Provided in FIG. 4 is a schematic diagram of one embodiment of an identification cell 100 that can be fabricated in the circuitry of one embodiment of a printhead die (40 in FIGS. 1 & 2). The printhead die can include a plurality of such identification cells electrically coupled to one identification line 102 which receives an identification signal and provides the identification signal to the identification cells.

The identification cell 100 includes a memory element or identification bit, indicated at 103. The memory element stores one bit of information. In one

embodiment, depicted in FIG. 4, the memory element comprises a fuse, represented by fuse element 104 and fuse resistance 108. The identification cell includes a drive transistor or drive switch 106 electrically coupled to the memory element 103. The drive switch can be a FET (Field Effect Transistor) having a drain-source path that is electrically coupled at one end to one terminal of the memory element and at the other end to a reference 110, such as ground. The other terminal of the memory element is electrically coupled to the identification line 102. The identification line receives an identification signal and provides the identification signal to the memory element. The identification signal, including the program signal and the read signal, can be conducted through the memory element if the drive switch 106 is turned on (conducting). This allows for only specific identification cells on a single identification line to respond to read and programming signals on the identification line, while other identification cells on the same identification line do not respond to the read and programming signals.

The gate of the drive switch 106 forms a storage node capacitance 112, which functions as a memory to store charge pursuant to the sequential activation of the pre-charge transistor 114 and the select transistor 116. The drain-source path and gate of the pre-charge transistor are electrically coupled to the pre-charge line 118 that receives a pre-charge signal. The pre-charge line can be electrically connected to the pre-charge line 90 in FIG. 3.

The gate of the drive switch 106 is a control input that is electrically coupled to the drain-source path of the pre-charge transistor 114 and the drain-source path of the select transistor 116. The gate of the select transistor is electrically coupled to the select line 120 that receives a select signal. The select transistor can be electrically connected to the select line (92 in FIG. 3). The storage node capacitance 112 is shown in dashed lines, as it is part of the drive switch 106. Alternatively, a capacitor separate from the drive switch can be used to store charge.

The identification cell also includes a first transistor 122, a second transistor 124 and a third transistor 126 having drain-source paths that are electrically coupled in parallel. The parallel combination of these three

transistors is electrically coupled between the drain-source path of the select transistor 116 and the reference 110. The serial circuit including the select transistor coupled to the parallel combination of the first, second and third transistors is electrically coupled across the node capacitance 112 of the drive switch 106.

The gates of the first, second, and third transistors, 122, 124 and 126, are electrically coupled to three of the data lines of the associated fire group (82 in FIG. 3). The three data lines so connected can be any unique group of three of the eight data lines D1-D8 associated with the corresponding fire group. As shown in FIG. 4, the data lines can be those labeled DI-D3 in the fire group 82 in FIG. 3.

The pre-charge signal can be the pre-charge signal provided on pre-charge line 90a (labeled PRE 1) to the fire group 82, and the select signal can be the select signal provided on select line 92a (labeled SEL 1) to the fire group 82 in FIG. 3. To program the memory element 103, the identification cell 100 receives enabling signaling, including the pre-charge signal, select signal and data signals D1-D3 to turn on the drive switch 106. The identification line 102 provides the program signal in the identification signal to the memory element. The program signal provides a relatively high voltage (e.g. 16 volts) through the memory element to the conducting drive switch and reference 110. This high voltage changes the state of the memory element from a low resistive state to a high resistive state by burning out the fuse 104.

To read the state of the memory element 103, the identification cell 100 receives enabling signaling, including the pre-charge signal, select signal and data signals DI-D3 to turn on the drive switch 106. The identification line 102 provides the read signal in the identification signal to the memory element. The read signal provides a current through the memory element to the conducting drive switch 106 and reference 110. The voltage on the identification line can be detected to determine the resistive state of the memory element. In one embodiment, the memory element is determined to be in the high resistive state if the resistance is greater than about 1000 ohms (i.e. the fuse is burned out)

and in the low resistive state if the resistance is less than about 400 ohms (i.e. the fuse is intact).

Using the configuration of FIG. 4, each identification cell 100 can be individually enabled, and thereby can be programmed on an individual basis. Also, since the identification cells can be read individually, the combinations utilized to store data are greatly increased. For example, a single identification cell can be utilized in multiple combinations that each represents different information.

With three of eight data signals DI-D8 selecting each identification cell 100 in a plurality of identification cells, up to fifty six different identification cells can be selected by combinations of three of the eight data signals. Thus, with one pre-charge line, one select line, eight data lines, and one identification line the circuit can control fifty six identification bits, or about 5.1 identification cell bits per control line. Alternatively, each identification cell can be configured to respond to any suitable number of data signals, such as two or four or more data signals.

It should be noted that while Figure 4 discloses utilizing a single identification line 102 that is coupled to each of the identification cells 100, more than one identification line may be utilized, thus allowing a larger number of identification cells. Also, the number of identification cells that are provided may be more or less than 56 depending of factors such as the size of the die, the operating parameters of the fluid ejection device, or other considerations. Also, the number of identification cells that are encoded with information may be less than the total number of identification cells on the die.

While the identification cell configuration described above can be used in a variety of ways to store identification information on the printhead, fuses present some drawbacks noted earlier. The inventor has recognized that electronically programmable read-only memory, or EPROM, can be desirable to eliminate fuses in NMOS circuits, such as in ink jet printheads and other applications. EPROM cells do not include fuses, and provide a number of advantages over NMOS bits.

Shown in FIG. 5 is a schematic diagram of a typical EPROM cell or bit 210. An EPROM cell generally includes an input gate 212 (also called a control gate), a floating gate 214, and a semiconductor substrate 216 that includes a source 218 and a drain 220. As shown in FIG. 5, the substrate is provided with N+ doped regions adjacent to the source and drain, respectively, and a p doped region 222 therebetween. The control gate and floating gate are capacitively coupled together, with a dielectric material 224 between them, such that the control gate voltage is coupled to the floating gate. Another layer of dielectric material 226 is also disposed between the floating gate 214 and the semiconductor substrate 216.

A high voltage bias on the drain 220 generates energetic "hot" electrons. A positive voltage bias between the control gate 212 and the drain pulls some of these hot electrons onto the floating gate 214. As electrons are pulled onto the floating gate, the threshold voltage of the cell, that is, the voltage required to cause the gate/drain to conduct current, increases. If sufficient electrons are pulled onto the floating gate, those electrons will block current flow such that the threshold voltage will eventually increase to a level above a desired threshold voltage (e.g. the operating voltage of the circuit). This will cause the cell to block current at that voltage level, which changes the operating state of the cell from a 1 to a zero. After programming of the cell, a cell sensor (not shown) is used during normal operation to detect the state of the EPROM cell.

Because EPROM cells include two gates at each bit location, these chips require more layers than a PROM or NMOS chip as is typically used in an inkjet printhead circuit. Shown in FIG. 6 is a cross-sectional view of the layers in a typical EPROM chip 230. Disposed atop the semiconducting silicon substrate 232 is a gate oxide 236. Disposed atop the gate oxide layer is a layer of polysilicon material 238, in which the floating gate (14 in FIG. 5) is formed. When properly doped, this polysilicon material functions as a conductor. The gate oxide layer 236 functions as a dielectric layer (26 in FIG. 5) between the floating gate and the semiconductor substrate.

Disposed atop the floating gate layer is another layer 240 of gate oxide material, which provides another dielectric layer, atop which is another layer of

polysilicon 242, in which the control gate (12 in FIG. 5) is formed. Disposed atop the control gate layer are one or more metal layers 244, 248, separated by another dielectric layer 246. The metal layers provide row and column lines for the EPROM circuit, and also make the various electrical connections between the control gate, the drain, and other components of the circuit.

These circuit layers in a typical EPROM circuit are in contrast to the layers found in a typical inkjet printhead circuit. A cross-sectional view of the layers in an inkjet control chip 250, such as that providing the inkjet firing control circuit shown in FIG. 3, is given in FIG. 7. This chip includes a semiconductor substrate 252, atop which is an oxide layer 254 (such as silicon dioxide, SiO_2), followed by a polysilicon layer 256, a dielectric layer 258, then a Metal 1 layer 260 and Metal 2 layer 264, these metal layers being separated by a dielectric layer 262.

The two metal layers 260, 264 provide the conductors for the address lines, data lines, pre-charge, select, and fire lines, and other circuit connections. It will be apparent that this layer configuration lacks an additional polysilicon layer and gate dielectric that would be needed for creation of a standard EPROM cell. Prior attempts to implement EPROM's in this type of circuit have focused on adding additional process steps to add an extra floating gate and gate dielectric. Another option is to add a separate EPROM chip. Both of these options add complexity and cost

Advantageously, the inventor has developed a gate-coupled structure and method for providing EPROM functionality using the layers in this PROM chip, without adding process layers and cost. Shown in FIG. 8 is a schematic diagram of a gate-coupled EPROM bit 270 that can be created using the existing layers of the inkjet pen control chip shown in FIG. 7. The gate-coupled EPROM bit comprises two transistors having their floating gates tied together. The first transistor 272 is a control transistor, and the second transistor is the EPROM transistor 274. The control transistor includes two control connections or control terminals, the first terminal 276 being labeled Control1, and the second terminal 278 being labeled Control2.

The floating gate 280 of the control transistor 272 is electrically coupled to the floating gate 282 of the EPROM transistor 274. The EPROM transistor includes a drain 284 and source 286, which can be connected to ground. The floating gate voltage is dependent upon the overlap capacitance of the source and drain of the control transistor 272, and whether the gate of the control transistor is on. The overlap and gate capacitance couple the voltage at Control1 and Control2 to the floating gate. The capacitance needs to be large enough to provide adequate coupling voltage to the floating gate. A standard EPROM uses the capacitance in the dielectric layer between the control gate and the floating gate to couple the voltage to the floating gate. In the gate-coupled device disclosed herein, the gate to drain overlap capacitance between Control1 276 couples the voltage at Control1 to the floating gate. The gate to source overlap capacitance at Control2 278 couples the voltage at Control2 to the floating gate. The goal is to find some capacitance structure to couple to the floating gate. In this configuration, the gate oxide layer (254 in FIG. 7) that provides the gate capacitance of a standard transistor is used in a reverse direction to provide this capacitance.

This gate-coupled structure is fully compatible with the printhead layer structure shown in FIG. 7, and only requires modification of the geometric layout of the various circuit layers. The floating gates 280, 282 of the control and EPROM transistors, as well as the coupling connection between them, can be fabricated in the polysilicon layer 256 of the printhead circuit. Further, these floating gate regions in the polysilicon layer can be electrically interconnected by the Metal1 layer 260. The gate/drain coupling is from the n+ drain region of the substrate 252 to the gate, through the gate oxide layer 254. The Metal1 layer 260 can be configured to connect the source of the control transistor 272 (Control2, 278) to the drain of the EPROM transistor 274 (Drain 284). One advantageous feature of this configuration is that there is both source and drain coupling to the floating gate. This provides additional capacitive coupling from the control node to the floating gate. In general, the more capacitive coupling the better.

Referring again to FIG. 8, the gates 276, 278 of the control transistor 272 can be tied together, or Control2 can be tied to the drain of the EPROM transistor 274. For some implementations, Control1, Control2 and Drain can be tied to separate voltages to get more efficient coupling. With Control2 278 and Drain 284 tied together, the voltage on Drain can limit the voltage on Control2, and the amount of voltage coupled to the floating gate 280.

In one embodiment, a space efficient layout can be obtained by tying the Drain 284 of the EPROM transistor 274 to the source (Control2) 278 of the control transistor 272. If a resistor is not needed to limit the drain current (e.g., limiting overheating by controlling pulse width instead, or relying on the resistance of the Select transistors (when implemented in arrays) to limit the current), Control1, Control2 and Drain can all be tied together. This configuration provides a high level of coupling in a small area, but also has higher sensitivity to excess drain current and overheating.

Alternatively, the drain 284 of the EPROM transistor 274 can be tied to the source (Control2) 278 of the control transistor 272, with a resistor 277 (shown in dashed lines in FIG. 8) between Control1 276 and Control2 278 to limit drain current. This configuration can be more robust with respect to drain current problems, though the voltage at the Control2-Drain node will be lower, and will provide less voltage to the floating gate.

Another approach is to hook the terminals 278 and 276 of the control transistor 272 together, with a resistor 283 (shown in dashed lines in FIG. 8) in series between them and the Drain 284 of the EPROM transistor 274. The resistor would limit current into the Drain, but the voltage at the nodes labeled Control1 and Control2 would still be at maximum voltage for greater voltage coupling to the floating gate.

Programming of this gate-coupled EPROM cell 270, like typical EPROM cells, is done by applying a voltage pulse to the terminals 276, 278 of the control transistor 272. This is done in order to provide a quantity of hot electrons to the floating gate 280. It is desirable that the voltage on the Drain 284 be close to the breakdown voltage of the circuit. The breakdown voltage is the voltage at which the EPROM transistor 274 begins to conduct with the gate below

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threshold voltage (gate at zero volts). In one embodiment, the inventor has programmed the EPROM circuit at a voltage of about 16 ±1 V where the circuit has a breakdown voltage of 15 Volts

As noted above, Control2 278 can be tied to the Drain 284 with a resistor 283 (having a resistance of, e.g., 100 ohm) in order to limit the breakdown voltage. Additionally, the physical size of the channel (gate) length – that is, the length of the channel under the gates of the EPROM transistor 274 – can be manipulated to modify the breakdown voltage. For example, a narrower gate length will lower the breakdown voltage. In one embodiment, the inventor has used a gate length of from 3.0μm to 3.5μm, instead of 4μm for this purpose.

The time required for programming is a function of the floating gate voltage, the quantity of hot electrons drawn to the floating gate, the threshold voltage change desired, the total gate structure capacitance, and the thickness of the gate oxide (layer 254 in FIG. 7). The gate oxide thickness determines the percentage of energetic hot electrons that are able to reach the floating gate 280. In one embodiment, the floating gate voltage is in the range of 5 volts to 12 volts, though other voltage ranges can be used. The floating gate voltage depends upon the voltage on the control terminals 276, 278 of the control transistor 272, and the coupling ratio of the silicon substrate and polysilicon layers (252, 256, respectively, in FIG. 7). While the desired hot electrons will be provided with any gate oxide thickness, the thickness of the gate oxide will sometimes be fixed for a given chip configuration. For example, in one embodiment of a printhead control chip, the thickness of the gate oxide is fixed at about 700 Å.

The quantity of hot electrons provided during programming is higher when programming is done at close to the breakdown voltage, and with higher current. In one embodiment, the inventor has programmed with a 25 mA current, though other currents can also be used. The inventor has also contemplated a 20 mA programming current, for example, and other currents can also be used. A range for the threshold voltage that the inventor has used is from 3 volts to 7 volts, but other threshold voltage ranges can also be used.

Under the above parameters, the inventor has found that a 10 millisecond programming time can be used. However, different programming times can also be used, particularly if the various parameters mentioned above are varied. For example, the programming time can range from less than 100 μs to as much as several seconds (e.g. 4 seconds).

Reading of the EPROM cells is done by detecting the threshold voltage across the gate-coupled EPROM cell 270 using a cell sensor (not shown) elsewhere in the circuit. Detecting the threshold voltage can be done either by setting the gate/drain voltage and measuring the corresponding current, or by setting the current and measuring the voltage. The inventor has found that the on resistance (R_{on}) of the EPROM cell changes by a factor of about 2 before and after programming.

The inventor has built and tested this type of EPROM cell in a laboratory setting. In the test setup, a modified cell was built to monitor the floating gate voltage. A voltage pulse was applied to the gate and drain to program the EPROM cell to a desired threshold voltage. To test the cell to sense the gate voltage, the gate of a second sense transistor (not shown) was connected to the floating gate of the EPROM cell. This causes the gate voltage of the sense transistor to be the same as the floating gate voltage. The on resistance (R_{on}) of the second transistor is proportional to the gate voltage. By monitoring the on resistance of the second transistor, the floating gate voltage could be determined.

The gate-coupled EPROM cell shown in FIG. 8 can be incorporated into circuitry in which each EPROM identification cell is associated with a separate control circuit, like that of FIG. 4, or the gate-coupled identification bits can be incorporated into an array of identification cells that share control circuitry. Shown in FIG. 9 is one embodiment of a gate-coupled EPROM cell associated with individual control circuitry. This figure shows a portion of the circuitry of the identification cell of FIG. 4, with the gate-coupled EPROM cell 270 inserted in place of the identification bit (103 in FIG. 4). Such a configuration will provide one control line per cell, with the operation of each EPROM cell being controlled by an individual control transistor. This sort of configuration has a larger

physical size than the shared-circuitry arrangement, but is similar to some control schemes currently used with fuses.

As shown in FIG. 9, the identification line 102 is connected to the gates of the control transistor 272 and the drain of the EPROM transistor 274, and the source 286 of the EPROM transistor is coupled to the drain of the drive switch 106, which has its source coupled to ground 110. A narrower gate 282a can be provided on the EPROM transistor 274 to provide lower breakdown voltage. This allows the gate-coupled EPROM cell to obtain an adequate quantity of hot electrons at the EPROM transistor without exceeding the breakdown voltages of other transistors on the circuit. As discussed above with respect to FIG. 8, a resistor 283 (e.g. about 100 ohms) could be added between the drain 284 of the EPROM transistor 274 and the source 278 of the control transistor 272, or a resistor 277 can be placed between the source of the control transistor and the drain 276 of the control transistor. The method chosen would depend upon layout decisions and technique used to control drain current.

Referring back to FIG. 9, when the transistor 106 is turned on, the source of the EPROM transistor 274 is essentially at ground, and the EPROM cell functions as described for the cell in Fig 8. A voltage on the ID line 102 couples thru the gate oxide of the control transistor 272 to the floating gate (280/282 in FIG. 8). A high voltage (16V) will program the EPROM. A lower voltage will be used to read by detecting the threshold voltage or the on resistance. If the transistor 106 is off, any voltage applied to the ID line will not have a path to ground, and the EPROM cell will not be affected

Shown in FIG. 10 is a partial schematic diagram of an EPROM array 300 that can be produced using the gate-coupled EPROM cell disclosed herein. In this configuration an array of gate-coupled EPROM identification bits share control circuitry. In this array, a plurality of gate-coupled EPROM cells 270 are arranged in rows and columns. The input line of each gate-coupled EPROM cell is tied to the input voltage V_{in} (designated at 304) through input line 308. The source line 286 of each EPROM transistor 274 is tied to the drain of a row transistor 310. The row transistors are tied through their sources 312 to the drains of column transistors 314. If desired, a drain current limiting resistor (not

shown) can be added to the EPROM cell, as described above with respect to Fig 9. Rather than an individual resistor for each gate-coupled cell, a single resistor 322 (shown in dashed lines in FIG. 10) could be provided to feed all of the transistors in parallel. This resistor can be connected between the voltage Vin and the drain of the EPROM transistor (284 in FIG. 8), with a single line from Vin to the resistor, and separate lines 324 (shown in dashed lines in FIG. 10) extending from the resistor to the drains of each of the EPROM transistors in the array. The connection between the source and drain of the EPROM control transistor 272 would then be removed, and all of the control transistor-drain connections of the EPROM cell 270 would be tied directly to the input line 308.

The row lines, labeled 316a for Row 1, 316b for Row 2, etc., connect to the gates of all row select transistors 310 in a given row. The sources 312 of all row transistors in a given column are connected to the drain of the column transistor 314 for that column. The gates 318 of each column transistor are connected to a voltage source (not shown) through column lines (not shown). The sources 320 of the column transistors are connected to a common voltage, such as ground. The column transistors are labeled 314a for Column 1, 314b for Column 2, and so on.

The row transistors 310 and column transistors 314 allow selection of the specific gate-coupled EPROM cells, both for programming and reading. The column transistors are normal transistors, and the interconnects to these transistors can be fabricated in the Metal 1 layer (260 in FIG. 7). Some advantages of this circuit are that it is more compact than implementation of identification cells with separate control circuitry, and it doesn't require the Metal2 layer and its associated layout rules. Additionally, the size of the gate-coupled EPROM array 300 is not limited by the configuration of the printhead firing cell control circuitry (80 in FIG. 3). This array can be as large or as small as desired, regardless of the number of data lines associated with the firing cell control circuit.

To program a cell 270 of the array 300, the cell is selected by applying a voltage to one row line (e.g. 316a) and one column line (e.g. to the gate of

column transistor 314a), and then a pulse of relatively high voltage V_{in} (e.g. 16V) is applied. To sense the condition of the cell, a lower input voltage V_{in} pulse (e.g. 5V) is applied in the same way, and the current is monitored. In this array, there is no high voltage across the drain to the source of the EPROM transistor except when programming. Advantageously, there are no drain to gate voltage coupling issues because the drain and gate of the EPROM transistors switch together. In addition, gate to drain coupling is actually advantageous because it increases the voltage coupling to the gate.

The inventor has found that the size of the row select transistors 316 is significant because they must handle the programming current, such as 20 mA, 25 mA, or higher. For this purpose, the inventor has used row select transistors having a width of 150 µm. It will be apparent that smaller sizes can be used for lower programming current, and larger sizes will be needed for higher current.

In operation, a row signal turns on all row control transistors 316 in that row. A column signal turns on a selected column control transistor 314. An input voltage V_{in} is then applied, and only the cell 270 with both its row and column transistor turned on will have the full voltage across it. All other cells will have the source of the EPROM transistor floating. That is, the source of the EPROM transistor will not be driven to any fixed voltage, but will just float to the voltages on the other terminals. There will be no voltage across the EPROM transistor.

An EPROM array can be configured in the manner described above for use in providing pen ID bits in an inkjet printhead. In this configuration, the row and column signals can be supplied by the shift register of the pen control circuit. That is, rather than drive the row and column lines individually, the respective values can be shifted into a shift register, and driven from the shift register outputs. The shift register addresses the row and column selects of the 2x10 array. It will be apparent to those skilled in the art of semiconductor design that the geometric configuration of the circuitry can be configured in a variety of ways.

The inventor has built and programmed a 4-bit array based on the above design. After programming, the EPROM cells have held their charge for over a year.

The reliability and longevity of the gate-coupled EPROM cell described herein depends upon a number of factors. Because the structure is different than the typical EPROM cell configuration, some aspects of the resultant design affect its robustness. For example, the larger size of the floating gate (280 in FIG. 8) can allow more area for leakage current. Additionally, the gate oxide (254 in FIG. 7) is not processed for absolute minimum leakage current.

Additionally, the flatness of the layers can affect their performance. Slight undulations in layer surfaces and variations in the thickness of the different layers can cause charge concentrations and leakage between the layers. In a pen control circuit configured with the layers of the PROM chip shown in FIG. 7, for example, the thickness and flatness of the polysilicon layer 256 and adjacent dielectric layer 254 are not as critical for operation of the PROM circuit. This factor affects the level of quality control applied to formation of these layers. However, in an EPROM circuit, these factors have a greater effect.

At the same time, there are other factors that affect fuses that do not affect EPROMS, or that do not affect them in the same way or to the same extent. As noted above, fuses have a number of drawbacks that are frequently bothersome. It is believed that EPROMs will ultimately be more reliable than fuses in the application disclosed herein. Where the possible limitations of the gate-coupled EPROM cell disclosed herein can be tolerated, this configuration can be useful without the need to increase quality control. This is true of inkjet pens. The design life for an inkjet pen is usually about 18 months, primarily because inkjet cartridges are usually sold soon after manufacture, and because the pen then gets used up. Consequently, if the EPROM cells can reliably hold their charge for that time period, there is little likelihood that the device will not work as intended. However, this same structure can be effectively used in other applications where greater reliability is desired by exerting greater control over the flatness and thickness of the layers.

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The gate-coupled EPROM structure disclosed herein can replace fuses in inkjet pen control circuits without adding process layers and cost. This configuration provides cells that are larger than traditional EPROM cells, but smaller than fuses.

The gate-coupled identification cells can be used to store a wide variety of identification information indicating features of or other information about the printhead die. For example, a printer employing a printhead having EPROM identification cells can use the identification information for a wide variety of purposes to optimize printing quality or perform other functions. For example, selected identification cells can store identification information about the printhead die, or about the inkjet cartridge or pen in which the printhead die is inserted, such as information indicating an out of ink detection level.

The identification cells can also store identification information indicating a thermal sense resistance (TSR) value to determine the temperature of the printhead. Selected identification cells can store identification information indicating a printhead uniqueness number to identify and properly respond to the printhead. Identification cells can be used to store identification information indicating an ink drop weight for a printhead. A printer can account for the drop weight values stored in selected identification cells and the out of ink detection level information stored in other selected identification cells to determine actual out of ink detection levels.

The printer can also use identification information for marketing purposes, such as regional marketing and original equipment manufacturer (OEM) marketing. For example, selected identification cells store identification information indicating a marketing region for the fluid ejection device. In one embodiment, selected identification cells can store identification information indicating the seller of an OEM fluid ejection device. Selected identification cells can also store identification indicating whether an OEM printer is unlocked. For example, the OEM printer can respond to the OEM unlocked information to unlock an OEM printer, such that the OEM printer can accept OEM printheads sold by a given company or group of companies and printheads sold by

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companies other than the given company or group of companies, such as the actual original manufacturer company.

Selected identification cells store identification information indicating the product type and product revision of a fluid ejection device. The product type and product revision can be used by a printer to ascertain physical characteristics about a printhead. Product revision physical characteristics, such as spacing between nozzle columns, that may change in future products can also be stored in selected identification cells of a printhead. In this embodiment, the product revision physical characteristic information can be used by the printer to adjust for the physical characteristic changes between product revisions.

Gate-coupled EPROM cells configured this way can also be used for many other purposes in addition to those noted above. Because the charge on the floating gate of the EPROM transistor (282 in FIG. 8) is cumulative, this configuration can be used to store cumulative quantities. For example, in an inkjet printhead, the gate-coupled EPROM cells can be successively reprogrammed to track the number of pages printed out, or for other purposes. Since programming of EPROM cells modifes the threshold voltage of the EPROM cell 270, successive programming of these cells can be used to control analog circuits, such as to create a variable time delay. Other applications are also possible.

It is to be understood that the above-referenced arrangements are illustrative of the application of the principles of the present invention. It will be apparent to those of ordinary skill in the art that numerous modifications can be made without departing from the principles and concepts of the invention as set forth in the claims.

CLAIMS

What is claimed is:

1. An EPROM cell in a printhead control circuit for an inkjet printer, the control circuit having a semiconductor substrate, one and only one polysilicon layer disposed above the semiconductor substrate, and a conductive layer disposed above the polysilicon layer, the EPROM cell comprising:

a control transistor, having a floating gate comprising a portion of the polysilicon layer;

an EPROM transistor, having a floating gate comprising a portion of the polysilicon layer; and

an electrical interconnection, comprising a portion of the conductive layer, interconnecting the floating gate of the control transistor and the floating gate of the EPROM transistor.

2. An EPROM cell in accordance with claim 1, wherein the control transistor comprises a first control terminal and a second control terminal, and further comprising an electrical interconnection between the first and second control terminals.

3. An EPROM cell in accordance with claim 2, wherein the electrical interconnection between the first and second control terminals comprises a resistance.

4. An EPROM cell in accordance with claim 1, wherein the control transistor comprises a first control terminal and a second control terminal, and the EPROM transistor comprises a drain, and further comprising an electrical interconnection between the second control terminal of the control transistor and the drain of the EPROM transistor.

5. An EPROM cell in accordance with claim 4, wherein the electrical interconnection between the second control terminal of the control transistor and the drain of the EPROM transistor comprises a resistance.

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6. An EPROM cell in accordance with claim 1, wherein the control transistor comprises a first control terminal and a second control terminal, and the EPROM transistor comprises a drain, and further comprising an electrical interconnection between the first and second control terminals of the control transistor and the drain of the EPROM transistor.

7. An EPROM cell in accordance with claim 6, wherein the electrical interconnection between the first and second control terminals of the control transistor and the drain of the EPROM transistor includes a resistance

8. An EPROM cell in accordance with claim 1, wherein a programming charge applied to the floating gate of the EPROM transistor is cumulative, such that the EPROM cell can be successively charged to store cumulative values.

9. An EPROM cell in accordance with claim 1, wherein the control transistor includes a drain connection, and the EPROM transistor includes a source connection, and further comprising an input line, connected to the drain connection of the control transistor, whereby programming signals can be provided to the EPROM transistor.

10. An EPROM cell in accordance with claim 9, further comprising a drive transistor, having a drain connected to the source of the EPROM transistor, a gate of the drive transistor being associated with a precharge line, a select line, and a data line of an array of firing cells, whereby programming and reading of the EPROM cell can be controlled by signals sent through the input line and through the precharge line, the select line, and the data line.

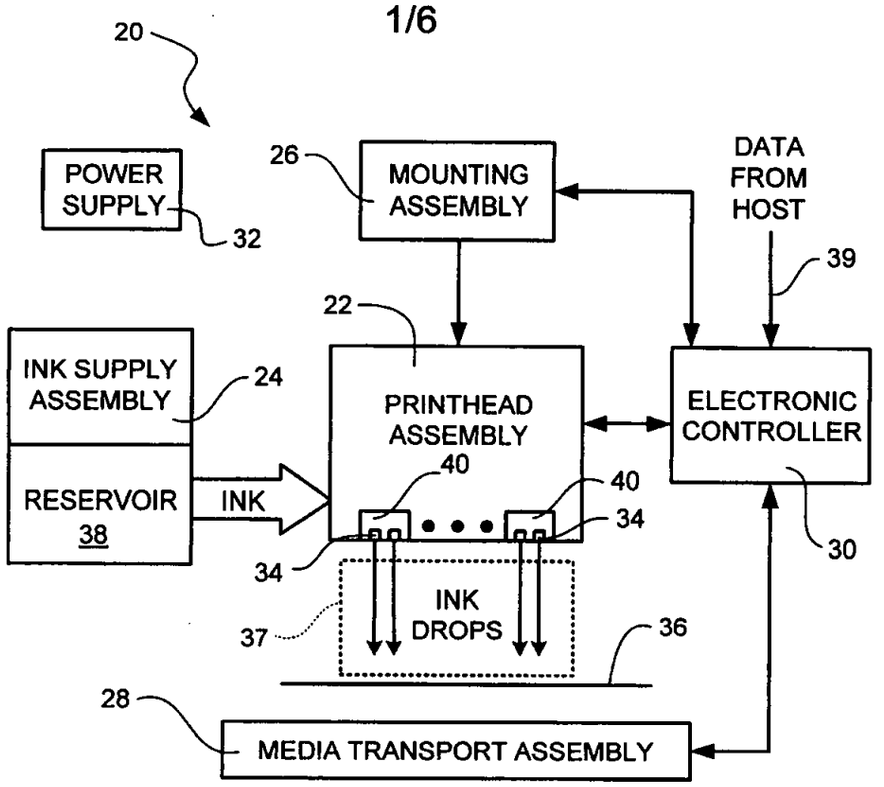
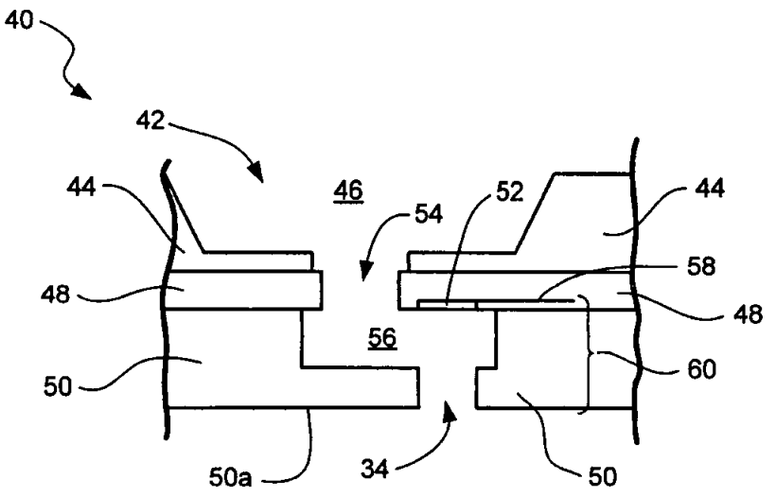

20
POWER SUPPLY
32
26
MOUNTING ASSEMBLY
DATA FROM HOST
39
22
INK SUPPLY ASSEMBLY
24
PRINTHEAD ASSEMBLY
ELECTRONIC CONTROLLER
RESERVOIR 38
INK
40
40
34
34
30
INK DROPS
37
36
28
MEDIA TRANSPORT ASSEMBLY

FIG. 1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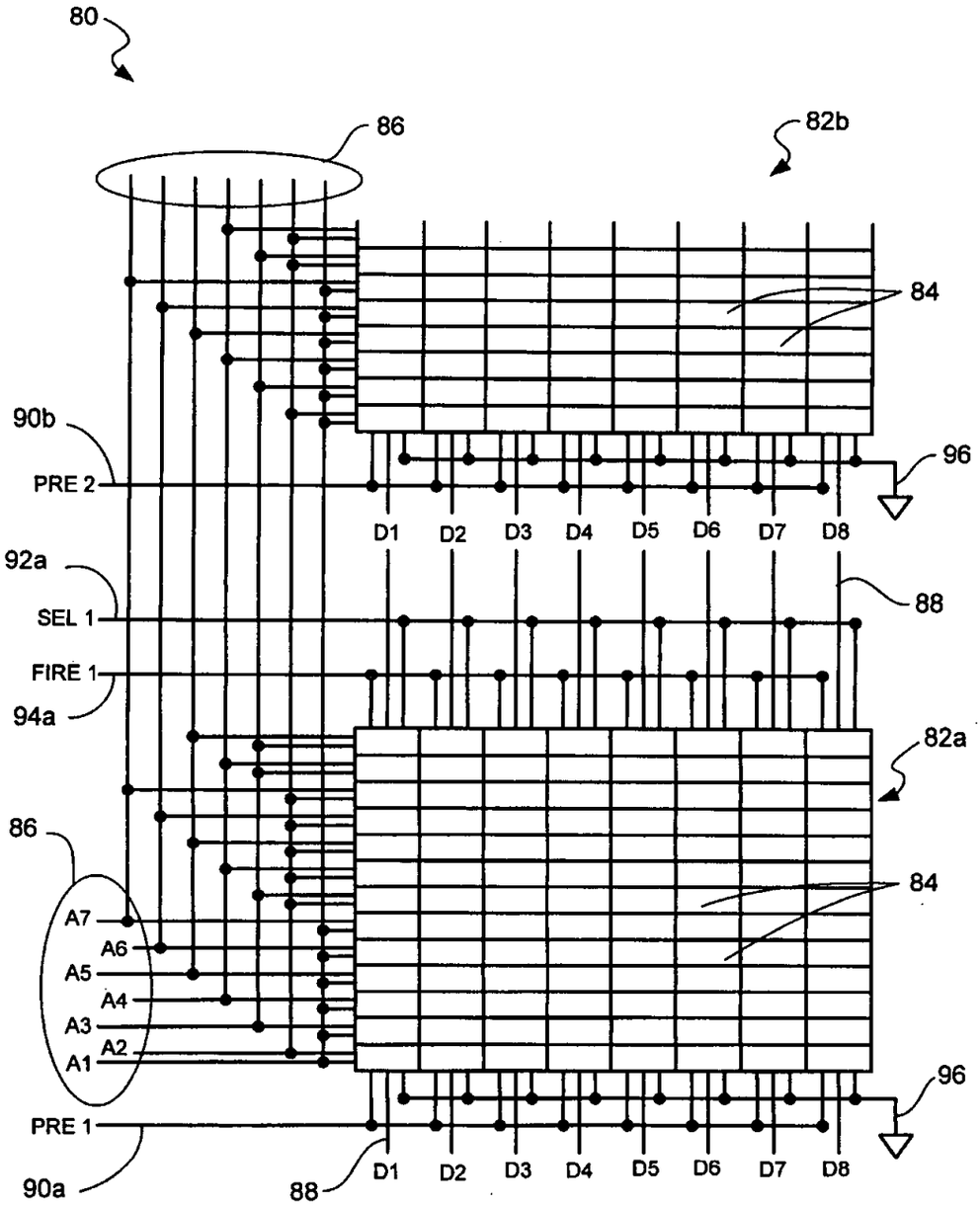
56
50
60
50a
34
50

FIG. 2


80
86
82b
84
90b
PRE 2
96
D1
D2
D3
D4
D5
D6
D7
D8
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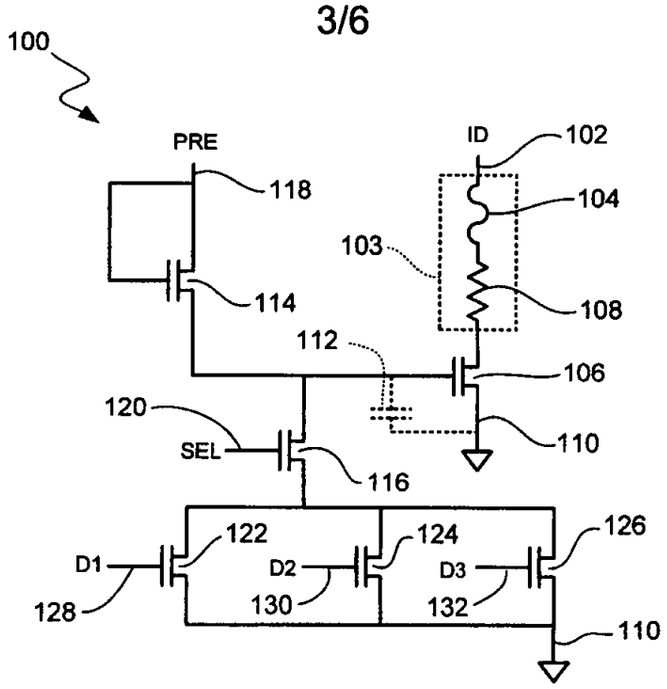
88
FIRE 1
94a
82a
86
84
A7
A6
A5
A4
A3
A2
A1
96
PRE 1
90a
88
D1
D2
D3
D4
D5
D6
D7
D8

FIG. 3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PRE
118
114
ID
102
104
103
108
112
106
120
SEL
116
110
122
124
126
D1
D2
D3
128
130
132
110

FIG. 4

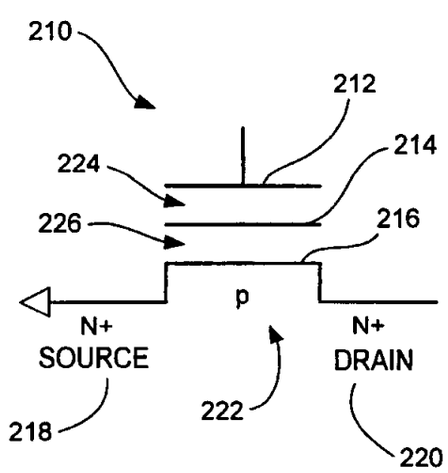
210
212
214
224
226
216
p
N+
SOURCE
N+
DRAIN
218
222
220

FIG. 5

36

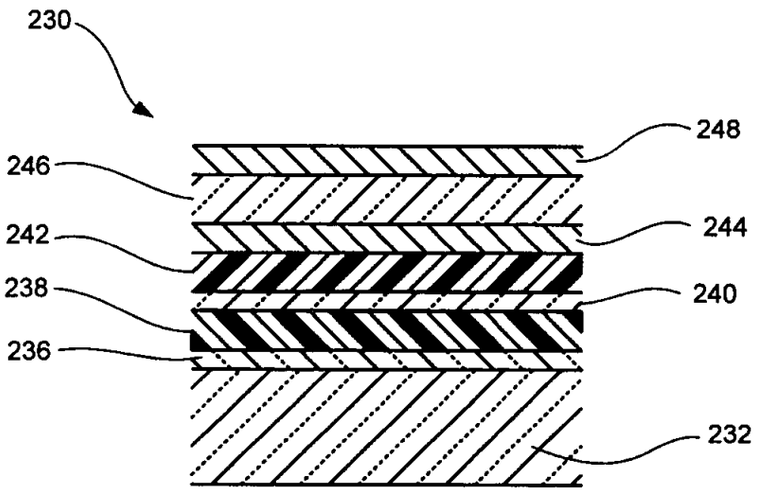
230
248
246
244
242
240
238
236
232

FIG. 6

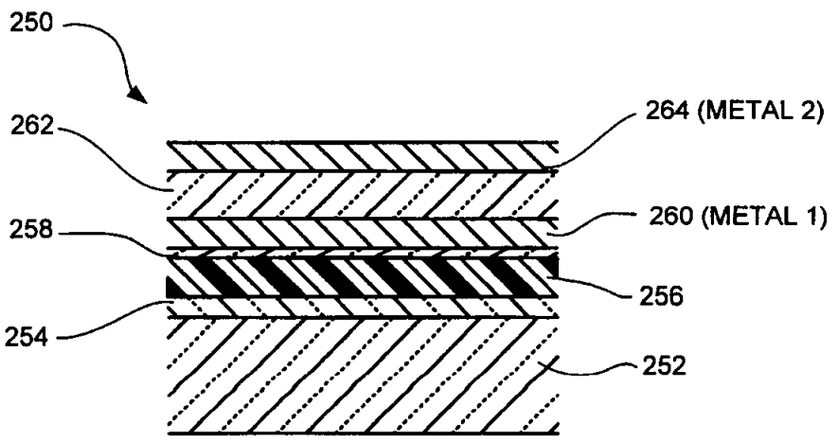
250
264 (METAL 2)
262
260 (METAL 1)
258
256
254
252

FIG. 7

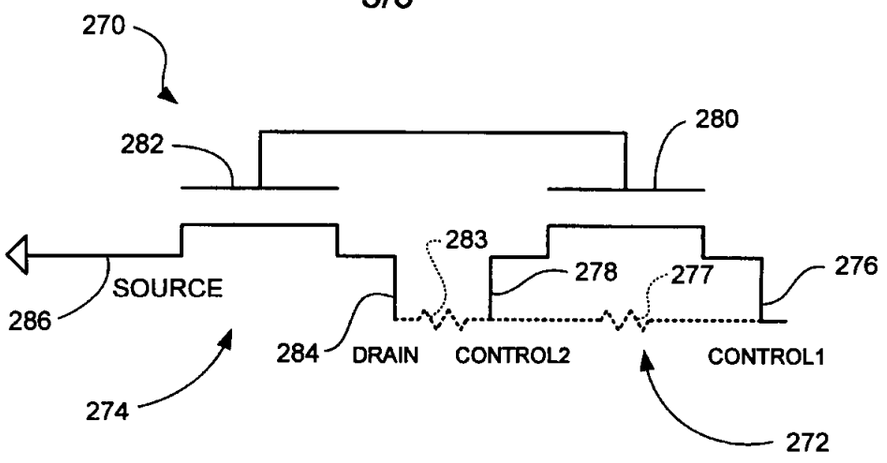
270
282
280
283
278
277
276
SOURCE
286
284
DRAIN
CONTROL2
CONTROL1
274
272

FIG. 8

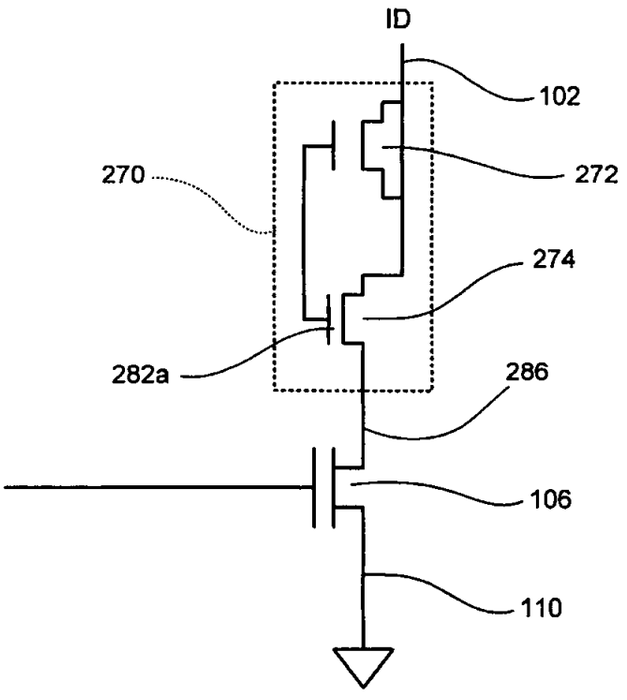
ID
102
270
272
274
282a
286
106
110

FIG. 9

38

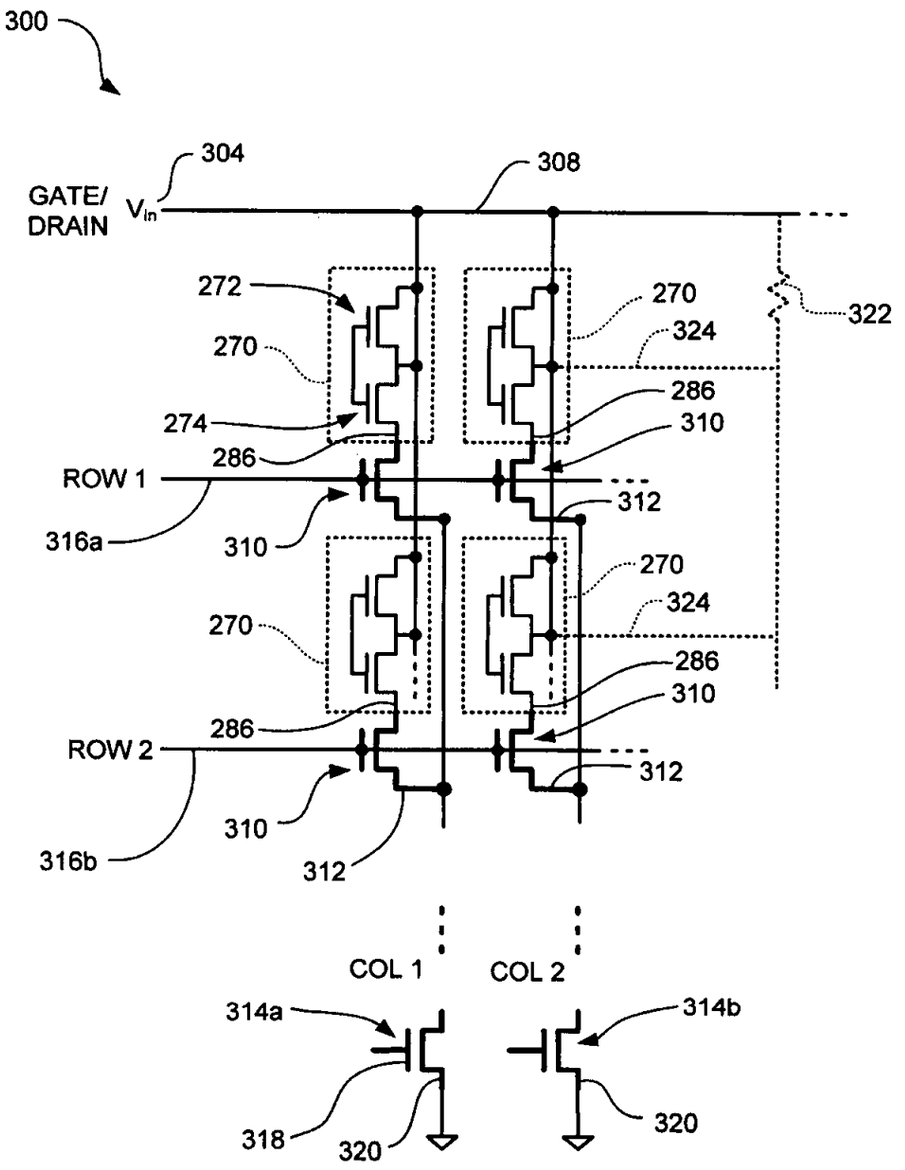
300
304
308
GATE/
DRAIN
V_{in}
272
270
274
286
310
312
322
324
ROW 1
316a
ROW 2
316b
COL 1
COL 2
314a
314b
318
320

FIG. 10

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Declaraciones bajo la Regla 4.17:

— *de la condición de inventor (Regla 4.17(i))*
— *en lo que respecta al derecho del solicitante de solicitar y de que se le otorgue una patente, (Regla 4.17(ii))*
— *en lo que respecta al derecho del solicitante de reivindicar la prioridad de la primera solicitud (Regla 4.17(iii))*

Publicado:
— *con informe internacional de búsqueda y a volverse a publicar al recibo de dicho informe*

Para códigos de dos letras y otras abreviaturas, remítase a las "Notas Guía sobre Códigos y Abreviaturas" que aparece al comienzo de cada edición regular del Boletín Oficial PCT.

WO 2007/120988 A2

(54) **Título**: CELDA EPROM, ACOPLADA A COMPUERTA, PARA CABEZAL DE IMPRESIÓN

(57) **Extracto:** Una celda EPROM (**270**) en un circuito de control de un cabezal de impresión para una impresora de chorro de tinta, que tiene exactamente una capa de silicio policristalino (**256**) y una capa conductora (**260**) dispuesta encima de la capa de silicio policristalino, incluye un transistor de control (**272**) y un transistor EPROM (**274**). Los transistores de control y EPROM tienen cada uno compuertas flotantes (**280**, **282**) que comprenden una porción de la capa de silicio policristalino (**256**), y una interconexión eléctrica, que comprende una porción de la capa conductora (**260**), interconecta la compuerta flotante (**280**) del transistor de control (**272**) y la compuerta flotante (**282**) del transistor EPROM (**274**).

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CELDA EPROM ACOPLADA A COMPUERTA PARA CABEZAL DE IMPRESIÓN

ANTECEDENTES

Un sistema de impresión de chorro de tinta es un tipo de dispositivo de eyección de fluido e incluye un cabezal de impresión, un suministro de tinta y un controlador electrónico que controla el cabezal de impresión. El cabezal de impresión eyecta gotas de tinta líquida a través de un arreglo de orificios o boquillas, dispuesto en una matriz, calentando rápidamente pequeños volúmenes de tinta localizados en cámaras de vaporización. La tinta se calienta con minúsculos calentadores eléctricos, tales como resistores de película delgada o resistores de encendido (***"firing resistors"***). El calentar la tinta hace que una porción de la tinta líquida se vaporice y, con ello, eyecte una gota única a través de la boquilla hacia una hoja de medio de impresión, tal una hoja de papel, para imprimir una imagen. Las boquillas de tinta se disponen típicamente en uno o más arreglos en la matriz del cabezal de impresión, de modo que la eyección consecutiva de tinta de las boquillas hace que se impriman caracteres u otras imágenes a medida que el cabezal de impresión recorre el medio de impresión.

Para eyectar cada gota de tinta, el controlador electrónico que controla el cabezal de impresión activa una corriente eléctrica de un suministro de energía externo al cabezal de impresión. La corriente eléctrica pasa a través de un resistor de encendido seleccionado para calentar la tinta en una cámara de vaporización seleccionada correspondiente y eyectar la tinta a través de una boquilla correspondiente. Generadores de gotas conocidos incluyen un resistor de encendido, una cámara de vaporización correspondiente y una boquilla correspondiente.

En sistemas de impresión de chorro de tinta es deseable tener varias características de cada cartucho de impresión fácilmente identificables por un controlador, y es deseable tener tal información de identificación suministrada directamente por el cartucho de impresión. Esta "información de identificación" puede proveer información al controlador para ajustar la

operación de la impresora y garantizar la correcta operación. Adicionalmente, a medida que aumentan los diferentes tipos de dispositivos de eyección de fluido y sus parámetros de operación, existe una necesidad de proporcionar una mayor cantidad de información de identificación sin agregar interconexiones adicionales al circuito flexible de interconexión automática (***"the flex tab circuit"***) o aumentar el tamaño de la matriz para proporcionar tal información de identificación.

Por estas y otras razones, se han desarrollado celdas de identificación de pluma e integrado con el conjunto de circuitos de las matrices de cabezal de impresión de chorro de tinta. En una configuración el conjunto de circuitos del cabezal de impresión es un circuito semiconductor de óxido metálico negativo (NMOS), y las celdas de identificación se configuran para ser direccionadas individualmente. Cada celda de identificación incluye un bit de identificación que almacena un bit de información.

Los bits de identificación de las celdas de identificación emplean típicamente fusibles y, aunque son diferentes de los chips estándar de memoria de solo lectura programable (PROM), estos bits se programan y usan básicamente en la misma forma. Para programar el chip, una corriente relativamente alta se enruta selectivamente a ciertos fusibles para hacer que se quemen. Los bits donde quedan los fusibles tienen un valor de 1, mientras que aquellos donde los fusibles se han quemado proporcionan un valor de 0 en la lógica binaria del circuito.

La programación y uso de chips ROM de esta forma tiene algunas desventajas. Si un chip se programa inicialmente de manera inapropiada, no hay forma de arreglarlo, y el chip tiene que descartarse. Adicionalmente, los fusibles son relativamente grandes y pueden no ser confiables. En circuitos de cabezal de impresión de chorro de tinta, por ejemplo, los fusibles pueden dañar la capa de orificios de chorro de tinta durante la programación y, luego de que un fusible se quema, restos de metal del fusible pueden arrastrarse a la tinta y ocasionar bloqueo en una pluma, o resultar en una pobre calidad de impresión.

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En años recientes, se han desarrollado igualmente dispositivos de memoria de solo lectura electrónicamente programable (EPROM). A diferencia de los chips PROM, los chips EPROM no incluyen fusibles. Al igual de los chips ROM, los EPROMs incluyen una rejilla conductora de columnas y filas. La celda en cada intersección tiene dos compuertas que se separan una de otra mediante una delgada capa de óxido que actúa como un dieléctrico. Una de las compuertas se denomina una compuerta flotante y la otra se denomina una compuerta de control o compuerta de entrada. El único vínculo de la compuerta flotante a la fila se da a través de la compuerta de control. Un blanco EPROM tiene todas las compuertas completamente abiertas, dándole a cada celda un valor de 1. Es decir, inicialmente la compuerta flotante no tiene carga, lo cual hace que el voltaje umbral sea bajo.

Para cambiar el valor del bit a 0, se aplica un voltaje de programación (por ejemplo 10 a 16 voltios) a la compuerta de control y drenaje. Este voltaje de programación atrae electrones excitados a la compuerta flotante, aumentando así el voltaje umbral. Los electrones excitados se empujan a través y se atrapan en el otro lado de la capa de óxido delgada, dándole una carga negativa. Estos electrones cargados negativamente actúan como una barrera entre la compuerta de control y la compuerta flotante. Durante el empleo de la celda EPROM, un sensor de celda monitorea el voltaje umbral de la celda. Si el voltaje umbral es bajo (por debajo del nivel umbral), la celda tiene un valor de 1. Si el voltaje umbral es alto (por encima del nivel umbral), la celda tiene un valor de cero.

Debido a que las celdas EPROM tienen dos compuertas en cada intersección, un chip EPROM requiere capas adicionales, comparado con un chip NMOS o PROM estándar, incluidos muchos chips similares que se usan frecuentemente en circuitos de cabezal de impresión de chorro de tinta. En consecuencia, aunque algunas de las desventajas de los fusibles en circuitos NMOS podrían eliminarse por la aplicación del conjunto de circuitos EPROM, el uso de una celda EPROM típica o bien requiere que el

chip se provea con capas adicionales, lo cual aumenta el costo y la complejidad del, o bien que se provea un chip EPROM separado.

BREVE DESCRIPCIÓN DE LOS DIBUJOS

Varias características y ventajas de la invención serán evidentes a partir de la siguiente descripción detallada, tomada en conjunción con los dibujos acompañantes, los cuales ilustran en forma conjunta, a modo de ejemplo, características de la invención, y en donde:

FIG. 1 es un diagrama de bloques de una incorporación de un sistema de impresión de chorro de tinta;

FIG. 2 es un diagrama que ilustra una porción de una incorporación de una matriz de cabezal de impresión;

FIG. 3 es un diagrama esquemático que ilustra una incorporación de un arreglo de celdas de encendido de un cabezal de impresión de chorro de tinta;

FIG. 4 es un diagrama esquemático de una incorporación de una celda de identificación en una incorporación de una matriz de cabezal de impresión;

FIG. 5 es un diagrama esquemático de un transistor EPROM típico;

FIG. 6 es una vista en sección transversal, que muestra las capas del sistema de circuitos eléctricos en un chip EPROM típico;

FIG. 7 es una vista en sección transversal, que muestra las capas en una incorporación de una matriz de cabezal de impresión de chorro de tinta que provee el sistema de circuitos eléctricos mostrado en FIG. 3;

FIG. 8 es un diagrama esquemático de una incorporación de una celda EPROM acoplada a una compuerta, que puede adaptarse para uso como un bit de identificación en el sistema de circuitos eléctricos del cabezal de impresión de FIG. 4;

FIG. 9 es un diagrama esquemático de una incorporación de una celda de identificación que tiene un bit de identificación EPROM acoplado a una compuerta; y

FIG. 10 es un diagrama esquemático de un arreglo de celdas EPROM acopladas a compuerta para un circuito de cabezal de impresión.

DESCRIPCIÓN DETALLADA

Se hará ahora referencia a incorporaciones ejemplares, ilustradas en los dibujos, y se empleará lenguaje específico en esta solicitud para describir los mismos. Se entenderá no obstante que, con ello, no se pretende una limitación del ámbito de la invención. Se considerarán dentro del ámbito de la invención alteraciones y otras modificaciones de las características inventivas ilustradas en esta solicitud, y aplicaciones adicionales de los principios de la invención como se ilustran en esta solicitud, que se le ocurrirían a una persona experta en el arte relevante y en posesión de esta divulgación, tienen que considerarse dentro del ámbito.

En FIG. 1 se ilustra un diagrama de bloques de una incorporación de un sistema de impresión de chorro de tinta **20**. El sistema de impresión de chorro de tinta incluye generalmente un ensamble de cabezal de impresión de chorro de tinta **22** y un ensamble de suministro de fluido, tal como el ensamble de suministro de tinta **24**. El sistema de impresión de chorro de tinta incluye asimismo un ensamble de montaje **26**, un ensamble de transporte de medios **28** y un controlador electrónico **30**. Un suministro de energía **32** provee energía a los varios componentes eléctricos del sistema.

En la incorporación mostrada en FIG. 1, el ensamble de cabezal de impresión de chorro de tinta **22** incluye por lo menos un cabezal de impresión o matriz de cabezal de impresión **40** que eyecta gotas de tinta a través de una pluralidad de orificios o boquillas **34** hacia un medio de impresión **36**, con el fin de imprimir sobre el medio de impresión. El medio de impresión puede ser cualquier tipo de material en hojas apropiado, tal como papel, cartulina, transparencias, Mylar®, tela y similares. Típicamente, las boquillas **34** se disponen en una o más columnas o arreglos de modo que la eyección secuenciada adecuadamente de tinta de las boquillas hace que se impriman caracteres, símbolos, y/u otros gráficos o imágenes sobre el medio de impresión a medida que el ensamble de cabezal

de impresión de chorro de tinta y el medio de impresión se mueven uno en relación con el otro. El cabezal de impresión **40** es una incorporación de un dispositivo de eyección de fluido. Aunque la siguiente descripción se refiere a la eyección de tinta del ensamble de cabezal de impresión **22**, hay que entender que otros líquidos, fluidos o materiales que fluyen, incluido un fluido transparente, pueden eyectarse del ensamble de cabezal de impresión.

El ensamble de suministro de tinta **24** es una incorporación de un ensamble de suministro de fluido y provee tinta al ensamble de cabezal de impresión **22**. El ensamble de suministro de tinta incluye un depósito **38** para almacenar tinta, que fluye del depósito al ensamble de cabezal de impresión de chorro de tinta. El ensamble de suministro de tinta y el ensamble de cabezal de impresión de chorro de tinta pueden formar o bien un sistema de entrega de tinta de una sola vía o bien un sistema de entrega de tinta con recirculación. En un sistema de entrega de tinta de una sola vía, sustancialmente toda la tinta suministrada al ensamble de cabezal de impresión de chorro de tinta se consume durante la impresión. En un sistema de entrega de tinta con recirculación, sólo una porción de la tinta suministrada al ensamble de cabezal de impresión se consume durante la impresión. En tal sistema, la tinta no consumida durante la impresión se recircula al ensamble de suministro de tinta.

En una incorporación de un sistema de impresión de chorro de tinta, el ensamble de cabezal de impresión de chorro de tinta **22** y el ensamble de suministro de tinta **24** se alojan juntos en un cartucho de tinta o pluma. Alternativamente, el ensamble de suministro de tinta puede estar separado del ensamble de cabezal de impresión de chorro de tinta, y suministrar tinta al ensamble de cabezal de impresión de chorro de tinta a través de una conexión de interfase, tal como un tubo de suministro (no mostrado). En cualquiera de las dos incorporaciones, el depósito **38** puede retirarse, reemplazarse y/o recargarse.

El ensamble de montaje **26** posiciona el ensamble de cabezal de impresión de chorro de tinta **22** en relación con el ensamble de transporte de medios **28**, el cual posiciona el medio de impresión **36** en relación con el

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ensamble de cabezal de impresión de chorro de tinta. Se define por lo tanto una zona de impresión **37** adyacente a las boquillas **34** en un área entre el ensamble de cabezal de impresión de chorro de tinta y el medio de impresión. El ensamble de cabezal de impresión de chorro de tinta puede ser un ensamble de cabezal de impresión tipo escaneador, en donde el ensamble de montaje incluye un carro (no mostrado) para mover el ensamble de cabezal de impresión de chorro de tinta en relación con el ensamble de transporte de medios para escanear el medio de impresión. Alternativamente, el ensamble de cabezal de impresión de chorro de tinta puede ser un ensamble de cabezal de impresión tipo no escaneador, en donde el ensamble de montaje fija el ensamble de cabezal de impresión de chorro de tinta en una posición prescrita, relativa al ensamble de transporte de medios **28**.

El controlador electrónico o controlador de la impresora **30** incluye típicamente un procesador, un programa fijo (***"firmware"***) y demás electrónica, o cualquier combinación de los mismos, para comunicar con y controlar el ensamble de cabezal de impresión de chorro de tinta **22**, el ensamble de montaje **26** y el ensamble de transporte de medios **28**. El controlador electrónico recibe datos **39** de un servidor de base de datos (***"a host system"***), tal como un computador y, usualmente, incluye memoria (no mostrado) para almacenar temporalmente los datos. Típicamente, los datos se envían al sistema de impresión de chorro de tinta **20** junto con una ruta electrónica, infrarroja, óptica, u otra ruta de transferencia de información. Los datos representan, por ejemplo, un documento a imprimirse, e incluye uno o más comandos de trabajos de impresión y/o parámetros de comandos, formando así un trabajo de impresión para el sistema de impresión de chorro de tinta. El patrón de las gotas de tinta eyectadas se determina por los comandos de trabajos de impresión y/o parámetros de comandos.

El ensamble de cabezal de impresión de chorro de tinta **22** puede incluir un cabezal de impresión **40**, o puede ser un arreglo amplio o ensamble de cabezal de impresión multi-cabezas. El ensamble de cabezal de impresión de chorro de tinta puede incluir un soporte, que soporta las

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impresión de chorro de tinta puede incluir un soporte, que soporta las matrices del cabezal de impresión, provee comunicación eléctrica entre las matrices del cabezal de impresión y el controlador electrónico **30** y provee comunicación fluida entre las matrices del cabezal de impresión y el ensamble de suministro de tinta **24**.

En FIG. 2 se provee un diagrama que ilustra una porción de una incorporación de una matriz de cabezal de impresión **40**. La matriz del cabezal de impresión incluye un arreglo de elementos de impresión o eyección de fluido **42**. Los elementos de impresión se forman en un sustrato **44**, que tiene una ranura de alimentación de tinta **46** formada en él. La ranura de alimentación de tinta provee un suministro de tinta líquida a los elementos de impresión, y es una incorporación de una fuente de alimentación de fluido. Otras incorporaciones de fuentes de alimentación de fluido incluyen, sin limitación, los correspondientes huecos individuales de alimentación de tinta que alimentan las correspondientes cámaras de vaporización y múltiples fosas más cortas de alimentación de tinta, que alimentan cada uno grupos correspondientes de elementos de eyección de fluido.

Una estructura de película delgada **48** se provee con un canal de alimentación de tinta **54** formada en ella. Este canal comunica con la ranura de alimentación de tinta **46** formada en el sustrato **44**. Una capa de orificios **50** tiene una cara frontal **50a** y una abertura de boquilla **34** formada en la cara frontal. La capa de orificios tiene también una cámara de boquilla o cámara de vaporización **56** formada en ella, que comunica con la abertura de boquilla y el canal de alimentación de tinta de la estructura de película delgada. Un resistor de encendido (***"a firing resistor"***) **52** se ubica en la cámara de vaporización, e hilos conductores (***"conductive leads"***) **58** acoplan eléctricamente este resistor de encendido al sistema de circuitos eléctricos, que controla la aplicación de corriente eléctrica a través de los resistores de encendido seleccionados. Tal como se emplea en esta solicitud, el término "generador de gotas" **60** incluye el resistor de

encendido **52**, la cámara de boquilla o cámara de vaporización **56** y la abertura de boquilla **34**.

Durante la impresión, fluye tinta de la ranura de alimentación de tinta **46** a la cámara de vaporización **56** mediante el canal de alimentación de tinta **54**. La abertura de boquilla **34** se asocia operativamente con el resistor de encendido **52**, de modo que gotículas de tinta en la cámara de vaporización se eyecten a través de la abertura de boquilla (por ejemplo, sustancialmente normal al plano del resistor de encendido) y hacia el medio de impresión **36** luego de energizar del resistor de encendido.

Existe una variedad de tipos de matrices de cabezal de impresión. Éstas incluyen cabezales de impresión térmicos, cabezales de impresión piezoeléctricos, cabezales de impresión electrostáticos y cualquier otro tipo de dispositivo de eyección de fluido conocido en el arte, que pueda integrarse en una estructura multi-capa. El sustrato **44** puede formarse, por ejemplo, de silicio, vidrio, cerámica, o un polímero estable, y la estructura de película delgada **48** puede formarse para incluir una o más capas de pasivación o aislamiento de dióxido de silicio, carburo de silicio, nitruro de silicio, tantalio, vidrio silicio policristalino, u otro material apropiado. La estructura de película delgada incluye además por lo menos una capa conductora, que define el resistor de encendido **52** y los hilos **58**. La capa conductora puede fabricarse, por ejemplo, de aluminio, plata, oro, tantalio, tantalio-aluminio, u otro metal o aleación de metal. El sistema de circuitos eléctricos de la celda de encendido, tal como se describe en detalle a continuación, puede implementarse en el sustrato y las capas de película delgada.

La capa de orificios **50** puede ser de una resina epóxica fotoimprimible (***"a photoimageable resin"***), tal como un epóxido designado como SU8, comercializado por Micro-Chem, de Newton, Massachusetts. Técnicas para fabricar la capa de orificios con SU8 u otros polímeros son bien conocidas por aquellas personas de habilidad en el arte. En una incorporación, la capa de orificios se forma de dos capas separadas, designadas como una capa barrera (por ejemplo, una capa barrera foto-

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resistente de película seca) y una capa de orificios metálica (por ejemplo, una capa de níquel, cobre, aleaciones de hierro/níquel, paladio, oro, o rodio) formada sobre la capa barrera. Otros materiales apropiados pueden emplearse igualmente para formar la capa de orificios.

En FIG. 3 se muestra un diagrama esquemático de una porción de una incorporación de un circuito de celda de encendido de cabezal de impresión de chorro de tinta **80**. El circuito de celda de encendido incluye una pluralidad de grupos de encendido **82** (por ejemplo, seis grupos de encendido), comprendiendo cada grupo de encendido un arreglo de celdas de encendido pre-cargadas **84**. Un primer grupo de encendido **82a** y una porción de un segundo grupo de encendido **82b** se muestran en FIG. 3. Las celdas de encendido pre-cargadas en cada grupo de encendido se disponen esquemáticamente en 13 filas y 8 columnas. El número de celdas de encendido pre-cargadas y su distribución pueden variar según se desee.

Las 8 columnas de las celdas de encendido pre-cargadas **84** se acoplan eléctricamente a 8 líneas de encendido **88**, marcadas D1-D8. Cada una de las celdas de encendido en cada columna de celdas de encendido pre-cargadas se acopla eléctricamente a una de las líneas de encendido, y estas líneas de encendido se extienden a las correspondientes columnas de celdas de encendido pre-cargadas en el grupo de encendido **82b** y los grupos de encendido subsiguientes (no mostrados).

Las filas de celdas de encendido pre-cargadas **84** se acoplan eléctricamente para direccionar las líneas **86**, marcadas A1-A7, que reciben señales de dirección. Cada celda de encendido pre-cargada en una fila de celdas de encendido pre-cargadas, designada en esta solicitud como un subgrupo de filas o subgrupo, se acopla eléctricamente al mismo par de las líneas de dirección, siendo este par único para cada subgrupo de filas. El arreglo de celdas de encendido mostrado en el grupo de encendido **82** incluye 13 subgrupos de filas, pero será evidente que el arreglo puede incluir cualquier número apropiado de subgrupos. Las líneas de dirección se extienden también para conectarse con subgrupos de filas del grupo de encendido **82b** y grupos subsiguientes de encendido (no mostrados).

La línea de pre-carga **90a** (marcada PRE 1) recibe una señal de pre-carga, y provee la señal de pre-carga a todas las celdas de encendido pre-cargadas **84** en el primer grupo de encendido **82a**. Grupos de encendido adicionales tienen cada uno una línea de pre-carga separada, tal como la línea de pre-carga **90b** (marcada PRE2) para el grupo de encendido **82b**.

Una línea selectora **92a** (marcada SEL 1) recibe una señal selectora y provee esta señal a todas las celdas de encendido **84** en un grupo de encendido correspondiente **82** y una línea de encendido **94a** (marcada FIRE 1) provee una señal a todas las celdas de encendido pre-cargadas en el grupo de encendido asociado. La línea de encendido se acopla eléctricamente a los resistores de encendido (**52** en FIG. 2) de todas las celdas de encendido pre-cargadas **84** en un grupo de encendido. Grupos adicionales de encendido tienen cada uno sus propias líneas selectoras y de encendido separadas.

Adicionalmente, todas las celdas de encendido pre-cargadas **84** en el arreglo **80** se acoplan eléctricamente a una línea de referencia **96**, está unida a un voltaje de referencia, tal como un polo a tierra. Dada esta estructura, las celdas de encendido pre-cargadas en un subgrupo de filas de celdas de encendido pre-cargadas se acoplan eléctricamente a las mismas líneas de dirección **86**, la línea de pre-carga **90**, la línea selectora **92**, la línea de encendido **94** y la línea de polo a tierra **96**.

Las celdas de encendido **84** hacen que los resistores de encendido individuales (**52** en FIG. 2) de las boquillas de tinta operen selectivamente, con el fin de que eyecten tinta en el patrón deseado. Los grupos de encendido se pre-cargan primeramente a través de las líneas PRE **90** respectivas. Se proveen señales de dirección en las líneas de dirección **86** para direccionar un subgrupo de filas en cada uno de lo grupos de encendido **82**, incluido un subgrupo de filas en el grupo de encendido pre-cargado. Señales de datos se proveen en las líneas de encendido **88** para proporcionar datos a todos los grupos de encendido, incluido el grupo de filas direccionadas en el grupo de encendido pre-cargado. A continuación, se provee una señal selectora en la línea selectora **92** del grupo de

encendido pre-cargado para seleccionar el grupo de encendido pre-cargado. La señal selectora define un intervalo de tiempo de descarga para descargar la capacitancia de nodo en cada interruptor de mando (***"drive switch"***) (no mostrado) en una celda de encendido pre-cargada que, o bien no está en el subgrupo de filas direccionadas en el grupo de encendido seleccionado o bien se direcciona en el grupo de encendido seleccionado y que recibe una señal de datos de alto nivel. La capacitancia de nodo no descarga en celdas de encendido pre-cargadas que se direccionan en el grupo de encendido seleccionado y que reciben una señal de datos de bajo nivel. Un nivel de alto voltaje en el nodo de capacitancia activa el interruptor de mando (conducir).

Una vez los interruptores de accionamiento en el grupo de encendido seleccionado **82** se ajustan para conducir o no conducir, se provee un pulso de energía o pulso de voltaje en la línea de encendido **94** del grupo de encendido seleccionado. Celdas de encendido pre-cargadas **84**, que tienen interruptores de mando conductores, conducen corriente a través del resistor de encendido (**52** en FIG. 2) para calentar tinta y eyectar tinta del generador de gotas correspondiente (**60** en FIG. 2). En operación, la pluralidad de grupos de encendido **82** puede seleccionarse para encender en sucesión, u otras secuencias, y pueden utilizarse igualmente selecciones no consecutivas. Las señales de dirección provistas en las líneas de dirección **86** pueden ajustarse a una dirección de subgrupo de filas durante cada ciclo a través de los grupos de encendido y, así, realizan un ciclo a través de las direcciones del subgrupo de 13 filas en cada grupo de encendido antes de repetir una dirección de un subgrupo de filas. Después del último subgrupo de filas, las señales de dirección seleccionan el primer subgrupo de filas para iniciar el ciclo de direcciones de nuevo.

Con los grupos de encendido **82** operados en sucesión, la señal selectora para un grupo de encendido de usa como la señal de pre-carga para el siguiente grupo de encendido. La señal de pre-carga para un grupo de encendido precede a la señal selectora y a la señal de encendido para el un grupo de encendido. Después de la señal de pre-carga, las señales de los

datos se multiplexan en tiempo y se almacenan en el subgrupo de filas direccionadas de un grupo de encendido por la señal selectora. La señal selectora para el grupo de encendido seleccionado es también la señal de pre-carga para el siguiente grupo de encendido. Una vez completa la señal selectora para el grupo de encendido seleccionado, se provee la señal selectora para el siguiente grupo de encendido. Celdas de encendido pre-cargadas **84** en el subgrupo seleccionado encienden o calientan tinta basándose en la señal de datos almacenada a medida que la señal de encendido, incluido un pulso de energía, se provee al grupo de encendido seleccionado.

Como ya se anotó, puede ser deseable provee una mayor cantidad de información de identificación en el circuito del cabezal de impresión, sin agregar interconexiones adicionales al circuito flexible de interconexión automática o aumentar el tamaño de la matriz para proporcionar tal información de identificación. En consecuencia, se han desarrollado celdas de identificación que pueden incluirse en el conjunto de circuitos del cabezal de impresión, tales como las ilustradas en FIG. 3. En FIG. 4 se ilustra un diagrama esquemático de una incorporación de una celda de identificación **100** que puede fabricarse en el conjunto de circuitos de una incorporación de una matriz de cabezal de impresión (**40** en FIGS. 1 & 2). La matriz del cabezal de impresión puede incluir una pluralidad de tales celdas de identificación acopladas eléctricamente a una línea de identificación **102** que recibe una señal de identificación y provee la señal de identificación a las celdas de identificación.

La celda de identificación **100** incluye un elemento de memoria o bit de identificación, indicado en **103**. El elemento de memoria almacena un bit de información. En una incorporación, ilustrada en FIG. 4, el elemento de memoria comprende un fusible, representado por elemento de fusible **104** y la resistencia del fusible **108**. La celda de identificación incluye un transistor de mando o interruptor de mando **106** acoplado eléctricamente al elemento de memoria **103**. El interruptor de mando puede ser FET (Transistor de Efecto Campo - ***Field Effect Transistor***) con una ruta

drenaje-fuente que se acopla eléctricamente en un extremo a una terminal del elemento de memoria y en el otro extremo a una referencia **110**, tal como un polo a tierra. La otra terminal del elemento de memoria se acopla eléctricamente a la línea de identificación **102**. La línea de identificación recibe una señal de identificación y provee la señal de identificación al elemento de memoria. La señal de identificación, incluidas la señal del programa y la señal de lectura, puede conducirse a través del elemento de memoria si el interruptor de mando **106** se activa (conducir). Esto permite que únicamente celdas de identificación específicas en una sola línea de identificación respondan a señales de lectura y programación en la línea de identificación, mientras que otras celdas de identificación en la misma línea de identificación no respondan a las señales de lectura y programación.

La compuerta del interruptor de mando **106** forma una capacitancia de nodo de almacenamiento **112**, que funciona como una memoria para almacenar carga luego de la activación secuencial del transistor de pre-carga **114** y el transistor selector **116**. La ruta drenaje-fuente y la compuerta del transistor de pre-carga se acoplan eléctricamente a la línea de pre-carga **118** que recibe una señal de pre-carga. La línea de pre-carga puede conectarse eléctricamente a la línea de pre-carga **90** en FIG. 3.

La compuerta del interruptor de mando **106** es una entrada de control que se acopla eléctricamente a la ruta drenaje-fuente del transistor de pre-carga **114** y la ruta drenaje-fuente del transistor selector **116**. La compuerta del transistor selector se acopla eléctricamente a la línea selectora **120** que recibe una señal selectora. El transistor selector puede conectarse eléctricamente a la línea selectora (**92** en FIG. 3). La capacitancia de nodo de almacenamiento **112** se muestra en líneas de rayas, ya que es parte del interruptor de mando **106**. Alternativamente, puede usarse un capacitador separado del interruptor de mando para almacenar carga.

La celda de identificación incluye además un primer transistor **122**, un segundo transistor **124** y un tercer transistor **126** con rutas drenaje-fuente que se acoplan eléctricamente en paralelo. La combinación paralela de estos tres transistores se acopla eléctricamente entre la ruta drenaje-fuente del

transistor selector **116** y la referencia **110**. El circuito en serie, incluido el transistor selector acoplado a la combinación paralela de los transistores primero, segundo y tercero se acopla eléctricamente a través de la capacitancia de nodo **112** del interruptor de mando **106**.

Las compuertas de los transistores primero, segundo y tercero, **122**, **124** y **126**, se acoplan eléctricamente a tres de las líneas de encendido del grupo de encendido apropiado (**82** en FIG. 3). Las tres líneas de encendido así conectadas pueden ser cualquier grupo único de tres de las ocho líneas de encendido D1-D8 asociadas con el grupo de encendido correspondiente. Como se muestra en FIG. 4, las líneas de encendido pueden ser aquellas marcadas D1-D3 en el grupo de encendido **82** en FIG. 3.

La señal de pre-carga puede ser la señal de pre-carga provista en la línea de pre-carga **90a** (marcada PRE 1) al grupo de encendido **82**, y la señal selectora puede ser la señal selectora provista en la línea selectora **92a** (marcada SEL 1) al grupo de encendido **82** en FIG. 3. Para programar el elemento de memoria **103**, la celda de identificación **100** recibe señalización de habilitación, incluida la señal de pre-carga, la señal selectora y las señales de datos D1-D3 para activar el interruptor de mando **106**. La línea de identificación **102** provee la señal del programa en la señal de identificación al elemento de memoria. La señal del programa provee un voltaje relativamente alto (por ejemplo, 16 voltios) a través del elemento de memoria al interruptor de mando conductor y la referencia **110**. Este alto voltaje cambia el estado del elemento de memoria de un estado resistivo bajo a un estado resistivo alto quemando el fusible **104**.

Para leer el estado del elemento de memoria **103**, la celda de identificación **100** recibe señalización de habilitación, incluidas la señal de pre-carga, la señal selectora y las señales de los datos D1-D3 para activar el interruptor de mando **106**. La línea de identificación **102** provee la señal de lectura en la señal de identificación al elemento de memoria. La señal de lectura provee una corriente a través del elemento de memoria al interruptor de mando conductor **106** y la referencia **110**. El voltaje en la línea de identificación puede detectarse para determinar el estado resistivo del

elemento de memoria. En una incorporación, se determina que el elemento de memoria está en el estado resistivo alto si la resistencia es mayor que alrededor de 1.000 ohmios (es decir, el fusible se quema) y en el estado resistivo bajo si la resistencia es menor que alrededor de 400 ohmios (es decir, el fusible está intacto).

Utilizando la configuración de FIG. 4, cada celda de identificación **100** puede habilitarse individualmente y, así, puede programarse sobre una base individual. Además, puesto que las celdas de identificación pueden leerse individualmente, se aumentan en gran medida las combinaciones utilizadas para almacenar datos. Por ejemplo, una sola celda de identificación puede utilizarse en combinaciones múltiples que representan cada una información diferente.

Con tres de ocho señales de datos D1-D8 seleccionando cada celda de identificación **100** en una pluralidad de celdas de identificación, pueden seleccionarse hasta cincuenta y seis celdas de identificación diferentes mediante combinaciones de tres de las ocho señales de datos. Por lo tanto, con una línea de pre-carga, una línea selectora, ocho líneas de encendido y una línea de identificación, el circuito puede controlar cincuenta y seis bits de identificación, o alrededor de 5.1 bits de celda de identificación por línea de control. Alternativamente, cada celda de identificación puede configurarse para responder a cualquier número apropiado de señales de datos, tales como dos o cuatro o más señales de datos.

Debe anotarse que aunque la Figura 4 divulga utilizar una sola línea de identificación **102** que se acopla a cada una de las celdas de identificación **100**, puede utilizarse más una línea de identificación, permitiendo en esa forma un mayor número de celdas de identificación. Además, el número de celdas de identificación, que se proveen, puede ser mayor o menor que 56, dependiendo de factores tales como el tamaño de la matriz, los parámetros de operación del dispositivo de eyección de fluido, u otras consideraciones. Asimismo, el número de celdas de identificación que se codifican con información puede ser menor que el número total de celdas de identificación en la matriz.

Aunque la configuración de la celda de identificación ya descrita puede usarse en una variedad de modos para almacenar información de identificación en el cabezal de impresión, los fusibles presentan algunas desventajas anotadas anteriormente. El inventor ha reconocido que memoria de solo lectura programable electrónicamente, o EPROM, puede ser deseable para eliminar fusibles en circuitos NMOS, tales como en cabezales de impresión de chorro de tinta y otras aplicaciones. Las celdas EPROM no incluyen fusibles, y proporcionan un número de ventajas sobre los bits NMOS.

En FIG. 5 se ilustra un diagrama esquemático de una celda EPROM típica o bit **210**. Una celda EPROM incluye generalmente una compuerta de entrada **212** (también llamada un compuerta control), una compuerta flotante **214** y un sustrato semiconductor **216** que incluye una fuente **218** y un drenaje **220**. Como se muestra en FIG. 5, el sustrato se provee con regiones dopadas con N+, adyacentes a la fuente y drenaje, respectivamente, y una región dopada **p 222** entre ellas. La compuerta de control y la compuerta flotante están acopladas con capacitancia una con otra, con un material dieléctrico **224** entre ellos, de modo que el voltaje de la compuerta de control se acopla a la compuerta flotante. Otra capa de material dieléctrico **226** se dispone igualmente entre la compuerta flotante **214** y el sustrato semiconductor **216**.

Un ajuste de polarización de alto voltaje (***"a high voltage bias"***) en el drenaje **220** genera electrones "calientes" energéticos. Un ajuste de polarización de voltaje positivo entre la compuerta de control **212** y el drenaje atrae algunos de estos electrones calientes a la compuerta flotante **214**. A medida que los electrones son atraídos a la compuerta flotante, el voltaje umbral de la celda, es decir, aumenta el voltaje requerido para hacer que la compuerta/drenaje conduzca corriente. Si se atraen electrones suficientes a la compuerta flotante, esos electrones bloquearán el flujo de corriente de modo que el voltaje umbral aumentará eventualmente a un nivel por encima de un voltaje umbral deseado (por ejemplo, el voltaje de operación del circuito). Esto hará que la celda bloquee la corriente en ese

nivel de voltaje, que cambia el estado de operación de la celda de un 1 a un 0. Luego de programar la celda, se usa un sensor de celda (no mostrado) durante la operación normal para detectar el estado de la celda EPROM.

Debido a que las celdas EPROM incluyen dos compuertas en cada ubicación de bit, estos chips requieren más capas que un chip PROM o NMOS chip como se usa típicamente en un circuito de cabezal de impresión de chorro de tinta. En FIG. 6 se ilustra una vista de sección transversal de las capas en un chip EPROM típico **230**. Dispuesta encima de un sustrato de silicio semiconductor **232** se halla una capa de óxido de compuerta **236**. Dispuesta encima de la capa de óxido de compuerta se halla una capa de material silicio policristalino **238**, en la cual se forma la compuerta flotante (**14** en FIG. 5). Cuando se dopa apropiadamente, este material silicio policristalino funciona como un conductor. La capa de óxido de compuerta **236** funciona como una capa dieléctrica (**26** en FIG. 5) entre la compuerta flotante y el sustrato semiconductor.

Dispuesta encima de la capa de la compuerta flotante se encuentra otra capa **240** de un material de óxido de compuerta, que proporciona otra capa dieléctrica, encima de la cual se halla otra capa de silicio policristalino **242**, en la cual se forma la compuerta de control (**12** en FIG. 5). Dispuesta encima de la capa de la compuerta de control se encuentran una o más capas metálicas **244**, **248**, separadas por otra capa dieléctrica **246**. Las capas metálicas proveen líneas de filas y columnas para el circuito EPROM y, además, establecen varias conexiones eléctricas entre la compuerta de control, el drenaje y otros componentes del circuito.

Estas capas del circuito en un circuito EPROM típico se encuentran en contraste con las capas halladas en un circuito típico de cabezal de impresión de chorro de tinta. Una vista de sección transversal de las capas en un chip de control de chorro de tinta **250**, como la que provee el circuito de control de encendido de chorro de tinta ilustrado en FIG. 3, se da en FIG. 7. Este chip incluye un sustrato semiconductor **252**, encima de la cual se encuentra una capa de óxido **254** (tal como dióxido de silicio, SiO_2), seguida por una capa de silicio **256**, una capa dieléctrica **258**, luego una

capa metálica 1 **260** y una capa metálica 2 **264**, separándose estas capas metálicas por una capa dieléctrica **262**.

Las dos capas metálicas **260**, **264** proveen los conductores para las líneas de dirección, las líneas de encendido, las líneas de pre-carga, selectoras y de encendido, y otras conexiones del circuito. Será evidente que esta configuración de capa carece de una capa de silicio policristalino adicional y dieléctrica de compuerta que se necesitarían para la creación de una celda EPROM estándar. Intentos previos por implementar EPROM's en este tipo de circuito se han centrado en agregar pasos del proceso adicionales para añadir una compuerta flotante extra y un dieléctrico de la compuerta. Otra opción es agregar un chip EPROM separado. Estas dos opciones agregan costos y complejidad.

Ventajosamente, el inventor ha desarrollado una estructura acoplada a una compuerta y un método para proporcionar funcionalidad EPROM usando las capas en este chip PROM, sin agregar capas de proceso y costos. En FIG. 8 se ilustra un diagrama esquemático de un bit EPROM acoplado a una compuerta **270**, que puede crearse usando las capas existentes del chip de control de pluma de chorro de tinta mostrado en FIG. 7. El bit EPROM acoplado a una compuerta comprende dos transistores con sus compuertas flotantes unidas una con otra. El primer transistor **272** es un transistor de control, y el segundo transistor es el transistor EPROM **274**. El transistor de control incluye dos conexiones de control o terminales de control, marcándose la primera terminal **276** Control 1, y la segunda terminal **278** Control 2.

La compuerta flotante **280** del transistor de control **272** se acopla eléctricamente a la compuerta flotante **282** del transistor EPROM **274**. El transistor EPROM incluye un drenaje **284** y una fuente **286**, que pueden conectarse a tierra. El voltaje de compuerta flotante es dependiente de la capacitancia de recubrimiento de la fuente y el drenaje del transistor de control **272**, y de si la compuerta del transistor de control está activada. La capacitancia de recubrimiento y la compuerta acoplan el voltaje en Control 1 y Control 2 a la compuerta flotante. Se necesita que la capacitancia

necesita sea lo suficientemente grande para proporcionar un voltaje de acoplamiento adecuado a la compuerta flotante. Una EPROM estándar emplea la capacitancia en la capa dieléctrica entre la compuerta de control y la compuerta flotante para acoplar el voltaje a la compuerta flotante. En el dispositivo acoplado a compuerta divulgado en esta solicitud, la capacitancia de recubrimiento compuerta a drenaje entre Control 1 **276** acopla el voltaje en Control 1 a la compuerta flotante. La capacitancia de recubrimiento compuerta a fuente en Control 2 **278** acopla el voltaje en Control 2 a la compuerta flotante. El objetivo es hallar cierta estructura de capacitancia para acoplar a la compuerta flotante. En esta configuración, la capa de óxido de la compuerta (**254** en FIG. 7), que provee la capacitancia de la compuerta de un transistor estándar se usa en una dirección inversa para proporcionar esta capacitancia.

Esta estructura acoplada a compuerta es completamente compatible con la estructura de capa del cabezal de impresión mostrada en FIG. 7, y sólo requiere modificación de la distribución geométrica de las diferentes capas del circuito. Las compuertas flotantes **280**, **282** de los transistores de control y EPROM, así como la conexión de acoplamiento entre ellos, pueden fabricarse en la capa de silicio policristalino **256** del circuito del cabezal de impresión. Además, estas regiones de la compuerta flotante en la capa de silicio policristalino pueden interconectarse eléctricamente por la capa metálica 1 **260**. El acoplamiento compuerta/drenaje va desde la región de drenaje **n+** del sustrato **252** a la compuerta, a través de la capa de óxido de la compuerta **254**. La capa metálica 1 **260** puede configurarse para conectar la fuente del transistor de control **272** (Control 2, **278**) al drenaje del transistor EPROM **274** (Drenaje **284**). Una característica ventajosa de esta configuración es que existe un acoplamiento tanto de fuente como de drenaje a la compuerta flotante. Esto provee acoplamiento capacitativo adicional desde el nodo de control a la compuerta flotante. En general, entre mayor sea el acoplamiento capacitativo, mejor.

Con referencia nuevamente a FIG. 8, las compuertas **276**, **278** del transistor de control **272** pueden unirse unas con otras, o el Control 2 puede

amarrarse al drenaje del transistor EPROM **274**. Para algunas implementaciones, el Control 1, el Control 2 y el Drenaje pueden amarrarse a voltajes separados para obtener un acoplamiento más eficiente. Con el Control 2 **278** y el Drenaje **284** amarrados uno con otro, el voltaje en el Drenaje puede limitar el voltaje en el Control 2 y la cantidad de voltaje acoplado a la compuerta flotante **280**.

En una incorporación, una distribución eficiente en espacio puede obtenerse amarrando el Drenaje **284** del transistor EPROM **274** a la fuente (Control 2) **278** del transistor de control **272**. Si no se necesita un resistor para limitar la corriente de drenaje (por ejemplo, limitar el sobrecalentamiento controlando en su lugar la amplitud del pulso, o basándose en la resistencia de los transistores selectores (cuando se implementan en arreglos) para limitar la corriente), Control 1, Control 2 y Drenaje pueden amarrarse todos en forma conjunta. Esta configuración proporciona un alto nivel de acoplamiento en un área pequeña, pero tiene también una sensibilidad más alta a un exceso de corriente de drenaje y sobrecalentamiento.

Alternativamente, el drenaje **284** del transistor EPROM **274** puede amarrarse a la fuente (Control 2) **278** del transistor de control **272**, con un resistor **277** (mostrado en líneas de rayas en FIG. 8) entre Control 1 **276** y Control 2 **278** para limitar la corriente de drenaje. Esta configuración puede ser más robusta con respecto a problemas de corriente de drenaje, aunque el voltaje en el nodo Control 2-Drenaje será más bajo y proporcionará menos voltaje a la compuerta flotante.

Otro método es enganchar (***"to hook"***) las terminales **278** y **276** del transistor de control **272** unas con otras, con un resistor **283** (mostrado en líneas de rayas en FIG. 8) en serie entre ellas y el Drenaje **284** del transistor EPROM **274**. El resistor limitaría la corriente en el Drenaje, pero el voltaje en los nodos marcados Control 1 y Control 2 estaría todavía en un voltaje máximo para un acoplamiento de voltaje mayor a la compuerta flotante.

La programación de esta celda EPROM acoplada a compuerta **270**, al igual que las celdas EPROM típicas, se hace aplicando un pulso de voltaje a

las terminales **276**, **278** del transistor de control **272**. Esto se hace con el fin de proporcionar una cantidad de electrones calientes a la compuerta flotante **280**. Es deseable que el voltaje en el Drenaje **284** esté cerca del voltaje de ruptura del circuito. El voltaje de ruptura es el voltaje al cual el transistor EPROM **274** comienza a conducir con la compuerta por debajo del voltaje umbral (compuerta a cero voltios). En una incorporación, el inventor ha programado el circuito EPROM con un voltaje de alrededor de 16 ±1 V, donde el circuito tiene un voltaje de ruptura de 15 voltios.

Como ya se anotó, el Control 2 **278** puede amarrarse al Drenaje **284** con un resistor **283** (que tiene una resistencia, por ejemplo, de 100 ohmios) con el fin de limitar el voltaje de ruptura. Adicionalmente, el tamaño físico de la longitud (compuerta) del canal – es decir, la longitud del canal bajo las compuertas del transistor EPROM **274** – puede manipularse para modificar el voltaje de ruptura. Por ejemplo, una longitud de compuerta más estrecha bajará el voltaje de ruptura. En una incorporación, el inventor ha usado una longitud de compuerta de 3.0μm a 3.5μm, en vez de 4μm para este propósito.

El tiempo requerido para programar es una función del voltaje de compuerta flotante, la cantidad de electrones calientes atraídos a la compuerta flotante, la variación de voltaje umbral deseada, la capacitancia total de la estructura de compuerta y el espesor de la capa de óxido de la compuerta (capa **254** en FIG. 7). El espesor de la capa de óxido de la compuerta determina el porcentaje de electrones calientes energéticos que son capaces de alcanzar la compuerta flotante **280**. En una incorporación, el voltaje de compuerta flotante está en el rango de 5 voltios a 12 voltios, aunque pueden utilizarse otros rangos de voltaje. El voltaje de compuerta flotante depende del voltaje en las terminales de control **276**, **278** del transistor de control **272**, y la relación de acoplamiento del sustrato de silicio y las capas de silicio policristalino (**252**, **256**, respectivamente, en FIG. 7). Aunque los electrones calientes deseados se proveerán con cualquier espesor de óxido de la compuerta, el espesor del óxido de la compuerta estará a veces fijado para una configuración dada de chip. Por

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ejemplo, en una incorporación de un chip de control de un cabezal de impresión, el espesor del óxido de la compuerta se fija en alrededor de 700 Å.

La cantidad de electrones calientes proporcionados durante la programación es más alta cuando la programación se hace cerca del voltaje de ruptura, y con una corriente más elevada. En una incorporación, el inventor ha programado con una corriente de 25 mA, aunque pueden emplearse también otras corrientes. Asimismo, el inventor ha contemplado una corriente de programación de 20 mA, por ejemplo, pero pueden emplearse también otras corrientes. Un rango para el voltaje umbral que el inventor ha utilizado va de 3 voltios a 7 voltios, pero pueden usarse igualmente otros rangos de voltaje umbral. Bajo los anteriores parámetros, el inventor ha descubierto que puede utilizarse un tiempo de programación de 10 milisegundos. No obstante, pueden usarse asimismo diferentes tiempos de programación, particularmente si los distintos parámetros ya mencionados se varían. Por ejemplo, el tiempo de programación puede variar desde menos de 100 μs a tanto como varios segundos (por ejemplo, 4 segundos).

La lectura de las celdas EPROM se hace detectando el voltaje umbral a través de la celda EPROM acoplada a compuerta **270** utilizando un sensor de celda (no mostrado) en alguna otra parte en el circuito. Detectar el voltaje umbral puede hacerse o bien ajustando el voltaje compuerta/drenaje y midiendo la corriente correspondiente, o bien ajustando la corriente y midiendo el voltaje. El inventor ha descubierto que la resistencia de activación (***"the on resistance"***) (R_{on}) de la celda EPROM varía por un factor de alrededor de 2 antes y después de la programación.

El inventor ha construido y probado este tipo de celda EPROM en un escenario de laboratorio. En la configuración de prueba, se construyó una celda modificada para monitorear el voltaje de compuerta flotante. Se aplicó un pulso de voltaje a la compuerta y drenaje para programar la celda EPROM a un voltaje umbral deseado. Para probar que la celda detecta el voltaje de compuerta, la compuerta de un segundo transistor de detección

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(no mostrado) se conectó a la compuerta flotante de la celda EPROM. Esto hace que el voltaje de la compuerta del transistor de detección sea el mismo que el voltaje de compuerta flotante. La resistencia de activación (R_{on}) del segundo transistor es proporcional al voltaje de la compuerta. Al monitorear la resistencia de activación del segundo transistor, el voltaje de compuerta flotante podría determinarse.

La celda EPROM acoplada a compuerta mostrada en FIG. 8 puede incorporarse en un conjunto de circuitos en el cual cada celda de identificación EPROM se asocia con un circuito de control separado, como el de FIG. 4, o los bits de identificación acoplados a compuerta pueden incorporarse en un arreglo de celdas de identificación que comparten el conjunto de circuitos. En FIG. 9 se ilustra una incorporación de una celda EPROM acoplada a compuerta, asociada con un conjunto de circuitos de control individual. Esta figura muestra una porción del conjunto de circuitos de la celda de identificación de FIG. 4, con la celda EPROM acoplada a compuerta **270** insertada en lugar del bit de identificación (**103** en FIG. 4). Tal configuración proporcionará una línea de control por celda, controlándose la operación de cada celda EPROM por un transistor de control individual. Esta clase de configuración tiene un tamaño más grande que el arreglo de conjunto de circuitos compartidos, pero es similar a algunos esquemas de control usados actualmente con fusibles.

Como se ilustra en FIG. 9, la línea de identificación **102** se conecta a las compuertas del transistor de control **272** y el drenaje del transistor EPROM **274**, y la fuente **286** del transistor EPROM se acopla al drenaje del interruptor de mando **106**, que tiene su fuente acoplada a un polo a tierra **110**. Una compuerta más estrecha **282a** puede proveerse en el transistor EPROM **274** para proporcionar un voltaje de ruptura más bajo. Esto permite que la celda EPROM acoplada a compuerta obtenga una cantidad adecuada de electrones calientes en el transistor EPROM sin exceder los voltajes de ruptura de otros transistores en el circuito. Como se discute anteriormente con respecto a FIG. 8, un resistor **283** (por ejemplo, alrededor de 100 ohmios) podría agregarse entre el drenaje **284** del transistor EPROM **274** y

la fuente **278** del transistor de control **272**, o un resistor **277** puede ponerse entre la fuente del transistor de control y el drenaje **276** del transistor de control. El método elegido dependería de las decisiones de distribución y la técnica utilizada para controlar la corriente de drenaje.

Con referencia nuevamente a FIG. 9, cuando el transistor **106** se activa, la fuente del transistor EPROM **274** está esencialmente a tierra (***"at ground"***), y la celda EPROM funciona como se describe para la celda en Fig 8. Un voltaje en la línea ID **102** se acopla a través del óxido de la compuerta del transistor de control **272** a la compuerta flotante (**280/282** en FIG. 8). Un voltaje elevado (16V) programará la EPROM. Un voltaje más bajo se usará para lectura detectando el voltaje umbral o la resistencia de activación. Si el transistor **106** está apagado, cualquier voltaje aplicado a la línea ID no tendrá una ruta a tierra, y la celda EPROM no se afectará.

En FIG. 10 se ilustra un diagrama esquemático parcial de un arreglo EPROM **300** que puede producirse usando una celda EPROM acoplada a compuerta, divulgada en esta solicitud. En esta configuración un arreglo de bits de identificación EPROM acoplados a compuerta comparte el conjunto de circuitos. En este arreglo, una pluralidad de celdas EPROM acopladas a compuerta **270** se dispone en filas y columnas. La línea de entrada de cada celda EPROM acoplada a compuerta se amarra al voltaje de entrada V_{in} (designado en **304**) a través de la línea de entrada **308**. La línea fuente **286** de cada transistor EPROM **274** se amarra al drenaje de un transistor de fila **310**. Los transistores de fila se amarran a través de sus fuentes **312** a los drenajes de transistores de columna **314**. Si se desea, un resistor limitante de corriente de drenaje (no mostrado) puede agregarse a la celda EPROM, como se describe más arriba con respecto a Fig 9. En lugar de un resistor individual para cada celda acoplada a compuerta, podría proveerse un solo resistor **322** (mostrado en líneas de rayas en FIG. 10) para alimentar la totalidad de los transistores en paralelo. Este resistor puede conectarse entre el voltaje V_{in} y el drenaje del transistor EPROM (**284** en FIG. 8), con una sola línea desde V_{in} al resistor, y líneas separadas **324** (mostradas en líneas de rayas en FIG. 10) que se extienden desde el resistor a los drenajes de

cada uno de los transistores EPROM en el arreglo. La conexión entre la fuente y el drenaje del transistor de control EPROM **272** se eliminaría entonces, y todas las conexiones del transistor de control-drenaje de la celda EPROM **270** se amarrarían directamente a la línea de entrada **308**.

Las líneas de filas, marcadas **316a** para Fila 1, **316b** para Fila 2, etc., conectan a las compuertas de todos los transistores selectores de fila **310** en una fila dada. Las fuentes **312** de todos los transistores de fila en una columna dada se conectan al drenaje del transistor de columna **314** para esa columna. Las compuertas **318** de cada transistor de columna se conectan a la fuente de voltaje (no mostrada) a través de líneas de columna (no mostradas). Las fuentes **320** de los transistores de columna se conectan a un voltaje común, tal como un polo a tierra. Los transistores de columna se marcan **314a** para Columna 1, **314b** para Columna 2, etc.

Los transistores de fila **310** y los transistores de columna **314** permiten la selección de las celdas EPROM acopladas a compuerta específicas, tanto para programación como para lectura. Los transistores de columna son transistores normales, y las interconexiones a estos transistores pueden fabricarse en la capa metálica 1 (**260** en FIG. 7). Algunas ventajas de este circuito consisten en que es más compacto que la implementación de celdas de identificación con un conjunto de circuitos separado, y que no requiere la capa metálica 2 y sus reglas de distribución asociada. Adicionalmente, el tamaño del arreglo EPROM acoplado a compuerta **300** no se limita por la configuración del conjunto de circuitos de control de la celda de encendido del cabezal de impresión (**80** en FIG. 3). Este arreglo puede ser tan grande o tan pequeño como se desee, sin importar el número de líneas de encendido asociadas con el circuito de control de la celda de encendido.

Para programar una celda **270** del arreglo **300**, se selecciona la celda aplicando un voltaje a una línea de fila (por ejemplo, **316a**) y una línea de columna (por ejemplo, a la compuerta del transistor de columna **314a**), y luego se aplica un pulso de voltaje relativamente alto V_{in} (por ejemplo, 16V). Para detectar una condición de la celda, se aplica de la misma manera

un pulso voltaje de entrada V_{in} más bajo (por ejemplo, 5V), y se monitorea la corriente. En este arreglo no hay voltaje alto a través del drenaje a la fuente del transistor EPROM, excepto cuando se programa. Ventajosamente, no hay problemas de acoplamiento de voltaje drenaje a compuerta porque el drenaje y la compuerta de los transistores EPROM se interconectan conjuntamente. Además, el acoplamiento compuerta a drenaje es ventajoso en la actualidad porque aumenta el acoplamiento del voltaje a la compuerta.

El inventor ha descubierto que el tamaño de los transistores selectores de fila **316** es significativo porque tienen que manejar la corriente de programación, tal como 20 mA, 25 mA, o mayor. Para este efecto, el inventor ha utilizado transistores selectores de fila que tienen un ancho de 150 µm. Será evidente que pueden usarse tamaños más pequeños para una corriente de programación más baja, y tamaños más grandes se necesitarán para una corriente más alta.

En operación, una señal de fila pone en marcha activa todos los transistores de control de fila **316** en esa fila. Una señal de columna activa un transistor de control de columna selectora **314**. A continuación se aplica un voltaje de entrada V_{in}, y únicamente la celda **270** con sus dos transistores de fila y columna activados tendrá el voltaje pleno a través de ella. Todas las demás celdas tendrán la fuente del transistor EPROM flotando. Es decir, la fuente del transistor EPROM no será inducida a algún voltaje fijo, sino flotará apenas tan sólo a los voltajes en las otras terminales. No habrá voltaje a través del transistor EPROM.

Puede configurarse un arreglo EPROM en la manera descrita anteriormente para uso en proporcionar bits ID de la pluma en una cabezal de impresión de chorro de tinta. En esta configuración, las señales de fila y columna pueden suministrarse por el registro de desplazamiento (***"the shift register"***) del circuito de control de la pluma. Es decir, más que inducir las líneas de fila y columna individualmente, los valores respectivos pueden desplazarse en un registro de desplazamiento, e inducirse desde las salidas del registro de desplazamiento. El registro de desplazamiento direcciona las

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selecciones de fila y columna del arreglo 2x10. Será evidente a los expertos en el arte del diseño de semiconductores que la configuración geométrica del conjunto de circuitos puede configurarse en una variedad de modos.

El inventor ha construido y programado un arreglo de 4 bits basado en el diseño anterior. Luego de programarlas, las celdas EPROM han conservado su carga durante más de un año.

La confiabilidad y longevidad de la celda EPROM acoplada a compuerta descrita en esta solicitud depende de un número de factores. Debido a que la estructura es diferente de la configuración típica de la celda EPROM, algunos aspectos del diseño resultante afectan su robustez. Por ejemplo, el mayor tamaño de la compuerta flotante (**280** en FIG. 8) puede permitir más área para corriente de fuga. Adicionalmente, el óxido de la compuerta (**254** en FIG. 7) no se procesa para una corriente de fuga mínima absoluta.

Adicionalmente, la planitud (***"the flatness"***) de las capas puede afectar su desempeño. Ligeras ondulaciones en las superficies de las capas y variaciones en el espesor de las diferentes capas pueden causar concentraciones de carga y fuga entre las capas. En un circuito de control de pluma, configurado con las capas del chip PROM mostrado en FIG. 7, por ejemplo, el espesor y la planitud de la capa de silicio policristalino **256** y las capas dieléctricas adyacentes **254** no son tan críticos para la operación del circuito PROM. Este factor afecta el nivel de control de calidad aplicado a la formación de estas capas. No obstante, en un circuito EPROM, estos factores tienen un mayor efecto.

Al mismo tiempo, existen otros factores que afectan los fusibles y que no afectan las EPROMs, o que no las afectan en la misma forma o en la misma medida. Como ya se anotó, los fusibles tienen un número de desventajas que, con frecuencia, son molestas. Se cree que las EPROMs serán en última instancia más confiables que los fusibles en la aplicación divulgada en esta solicitud. Donde las posibles limitaciones de la celda EPROM acoplada a compuerta, divulgada en esta solicitud, puedan tolerarse, esta configuración puede ser útil sin necesidad de aumentar el

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control de calidad. Esto es cierto de las plumas de chorro de tinta. El tiempo medio entre fallas (***"design life"***) de una pluma de chorro de tinta es usualmente de alrededor de 18 meses, principalmente porque los cartuchos de chorro de tinta se venden por lo general poco después de su fabricación, y porque entonces la pluma se desgasta. Por consiguiente, si las celdas EPROM pueden conservar confiablemente su carga durante ese período de tiempo, existe poca probabilidad de que el dispositivo no funcione como se prevé. No obstante, esta misma estructura puede usarse efectivamente en otras aplicaciones donde se desea una mayor confiabilidad ejerciendo un control mayor control sobre la planitud y el espesor de las capas.

La estructura EPROM acoplada a compuerta, divulgada en esta solicitud puede reemplazar fusibles en circuitos de control de una pluma de chorro de tinta, sin agregar capas de proceso y costos. Esta configuración proporciona celdas que son más grandes que las celdas EPROM tradicionales, pero más pequeñas que los fusibles. Las celdas de identificación acopladas a compuerta pueden utilizarse para almacenar una amplia variedad de información de identificación que indique características de información sobre la matriz del cabezal de impresión, u otra información. Por ejemplo, una impresora que emplee un cabezal de impresión con celdas de identificación EPROM puede usar la información de identificación para una amplia variedad de propósitos para optimizar la calidad de impresión o realizar otras funciones. Por ejemplo, celdas de identificación seleccionadas pueden almacenar información de identificación sobre la matriz del cabezal de impresión, o sobre el cartucho de tinta o pluma, en la cual se inserta la matriz del cabezal de impresión, tal como información que indique un nivel de detección de tinta agotada.

Las celdas de identificación pueden almacenar igualmente información de identificación que indique un valor de resistencia sensora térmica (TSR) para determinar la temperatura del cabezal de impresión. Celdas de identificación seleccionadas almacenan información de identificación que indica un número de exclusividad para identificar y responder adecuadamente al cabezal de impresión. Celdas de identificación

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pueden usarse para almacenar información de identificación que indique un peso de la gota de tinta para un cabezal de impresión. Una impresora puede relacionar los valores de peso de la gota almacenados en celdas de identificación seleccionadas y la información del nivel de detección de tinta agotada almacenada en otras celdas de identificación seleccionadas para determinar niveles actuales de detección de tinta agotada.

La impresora puede emplear asimismo información de identificación para fines de mercadeo, tales como mercadeo regional y mercadeo comercialización de fabricante de equipo original (OEM). Por ejemplo, celdas de identificación seleccionadas almacenan información de identificación que indique una región de mercadeo para el dispositivo de eyección de fluido. En una incorporación, celdas de identificación seleccionadas pueden almacenar información de identificación que indique el vendedor de un dispositivo de eyección de fluido OEM. Celdas de identificación seleccionadas pueden almacenar asimismo identificación que indique si una impresora OEM está desbloqueada. Por ejemplo, la impresora OEM puede responder a la información desbloqueada OEM para desbloquear una impresora OEM, de modo que la impresora OEM pueda aceptar cabezales de impresión OEM vendidos por una compañía dada o grupo de compañías y cabezales de impresión vendidos por compañías distintas de la compañía dada o grupo de compañías, tal como la compañía fabricante original actual.

Celdas de identificación seleccionadas almacenan información de identificación que indique el tipo de producto y la revisión del producto de un dispositivo de eyección de fluido. El tipo de producto y la revisión del producto pueden usarse por una impresora para verificar las características físicas sobre el cabezal de impresión. Características físicas de revisión del producto, tales como distancia entre columnas de boquillas, que pueden cambiar en productos futuros pueden almacenarse asimismo en celdas de identificación seleccionadas de un cabezal de impresión. En esta incorporación, la información de características físicas de la revisión del

producto puede usarse por la impresora para ajustar los cambios de características físicas entre revisiones del producto.

Celdas EPROM acopladas a compuerta, configuradas en esta forma, pueden utilizarse asimismo para muchos otros propósitos, aparte de los ya anotados. Debido a que la carga en la compuerta flotante del transistor EPROM (**282** en FIG. 8) es acumulativa, esta configuración puede usarse para almacenar cantidades acumulativas. Por ejemplo, en un cabezal de impresión de chorro de tinta, las celdas EPROM acopladas a compuerta pueden reprogramarse sucesivamente para rastrear el número de páginas impresas, o para otros propósitos. Puesto que la programación de celdas EPROM modifica el voltaje umbral de la celda EPROM **270**, la programación sucesiva de estas celdas puede usarse para controlar circuitos análogos, tales como crear un desfase de tiempo variable. Existe también la posibilidad de otras aplicaciones.

Hay que entender que los arreglos ya referenciados son ilustrativos de la aplicación de los principios de la presente invención. Será evidente a las personas de habilidad ordinaria en el arte que pueden introducirse numerosas modificaciones sin apartarse de los principios y conceptos de la invención como se exponen en las reivindicaciones.

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REIVINDICACIONES

Lo que se reivindica es:

1. Una celda EPROM en un circuito de control de un cabezal de impresión para una impresora de chorro de tinta, circuito de control que tiene un sustrato semiconductor, una y sólo una capa de silicio policristalino dispuesta encima del sustrato semiconductor y una capa conductora dispuesta encima de la capa de silicio policristalino, celda EPROM que comprende:

un transistor de control, con una compuerta flotante que comprende una porción de la capa de silicio policristalino;

un transistor EPROM, con una compuerta flotante que comprende una porción de la capa de silicio policristalino; y

una interconexión eléctrica, que comprende una porción de la capa conductora, interconectando la compuerta flotante del transistor de control y la compuerta flotante del transistor EPROM.

2. Una celda EPROM de acuerdo con la reivindicación 1, en donde el transistor de control comprende una primera terminal de control y una segunda terminal de control, y que comprende además una interconexión eléctrica entre las terminales de control primera y segunda.

3. Una celda EPROM de acuerdo con la reivindicación 2, en donde la interconexión eléctrica entre las terminales de control primera y segunda comprende una resistencia.

4. Una celda EPROM de acuerdo con la reivindicación 1, en donde el transistor de control comprende una primera terminal de control y una segunda terminal de control, y el transistor EPROM comprende un drenaje, y comprende además una interconexión eléctrica entre la segunda

terminal de control del transistor de control y el drenaje del transistor EPROM.

5. Una celda EPROM de acuerdo con la reivindicación 4, en donde la interconexión eléctrica entre la segunda terminal de control terminal del transistor de control y el drenaje del transistor EPROM transistor comprenden una resistencia.

6. Una celda EPROM de acuerdo con la reivindicación 1, en donde el transistor de control comprende una primera terminal de control y una segunda terminal de control, y el transistor EPROM comprende un drenaje, y comprende además una interconexión eléctrica entre las terminales de control primera y segunda del transistor de control y el drenaje del transistor EPROM.

7. Una celda EPROM de acuerdo con la reivindicación 6, en donde la interconexión eléctrica entre las terminales primera y segunda del transistor de control y el drenaje del transistor EPROM incluye una resistencia

8. Una celda EPROM de acuerdo con la reivindicación 1, en donde una carga de programación aplicada a la compuerta flotante del transistor EPROM es acumulativa, de modo que la celda EPROM puede cargarse sucesivamente para almacenar valores acumulativos.

9. Una celda EPROM de acuerdo con la reivindicación 1, en donde el transistor de control incluye una conexión de drenaje, y el transistor EPROM incluye una conexión fuente, y comprende además una línea de entrada, conectada a la conexión de drenaje del transistor de control, con lo cual pueden proporcionarse señales de programación al transistor EPROM.

10. Una celda EPROM de acuerdo con la reivindicación 9, que comprende además un transistor de mando, con un drenaje conectado a la fuente del transistor EPROM, asociándose una compuerta del transistor de mando con una línea de pre-carga, una línea selectora, y una línea de datos de un arreglo de celdas de encendido, con lo cual la programación y lectura de la celda EPROM pueden controlarse por señales enviadas a través de la línea de entrada y a través de la línea de pre-carga, la línea selectora y la línea de datos.

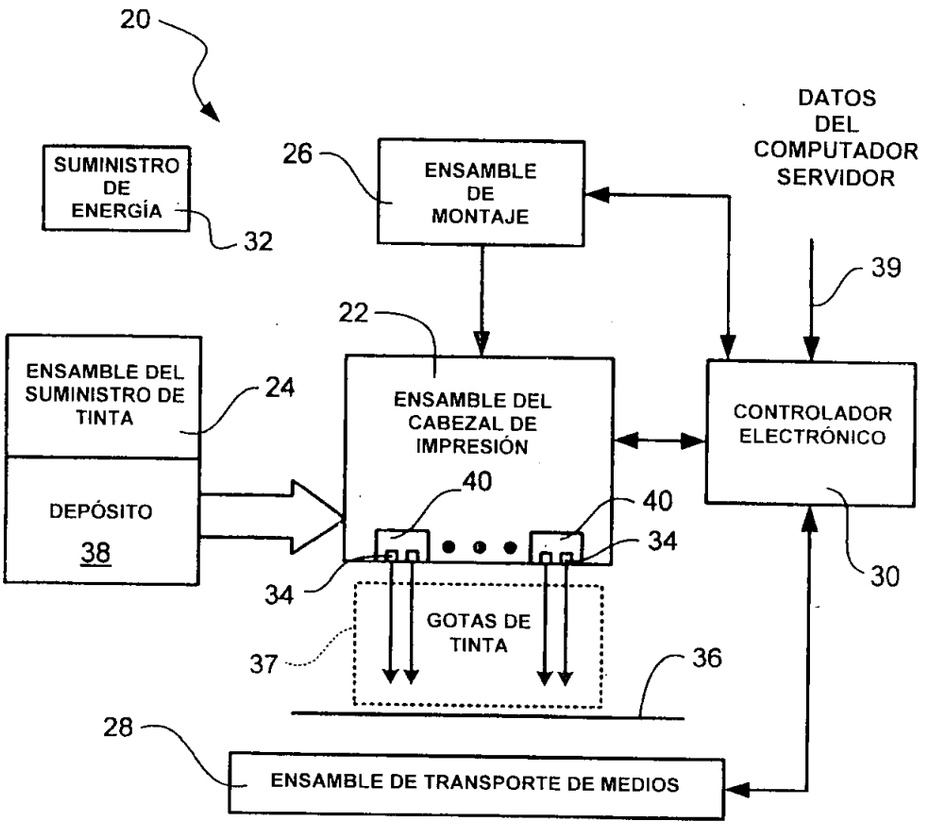
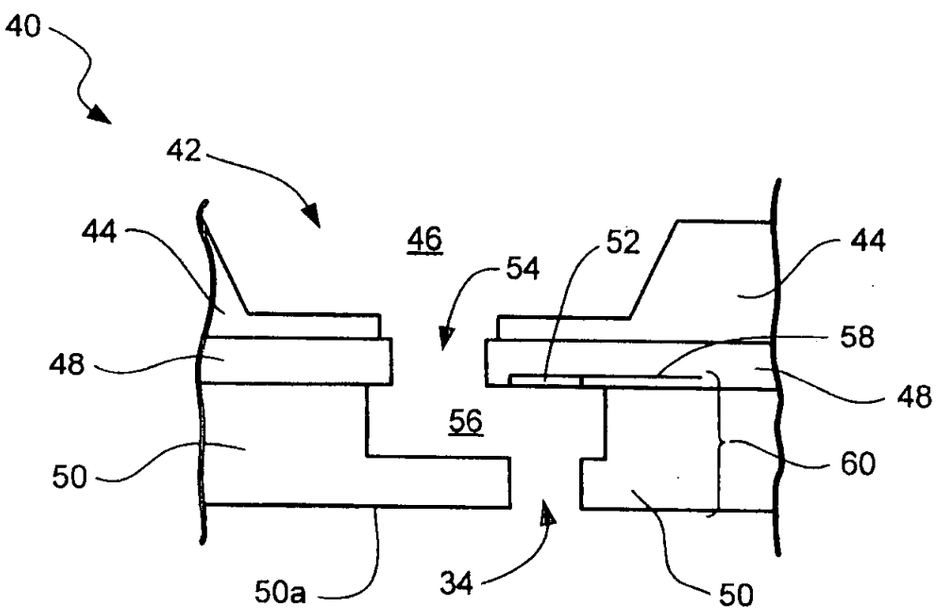

20
SUMINISTRO DE ENERGÍA
32
26
ENSAMBLE DE MONTAJE
DATOS DEL COMPUTADOR SERVIDOR
39
22
ENSAMBLE DEL SUMINISTRO DE TINTA
24
DEPÓSITO
38
ENSAMBLE DEL CABEZAL DE IMPRESIÓN
40
40
34
34
CONTROLADOR ELECTRÓNICO
30
GOTAS DE TINTA
37
36
28
ENSAMBLE DE TRANSPORTE DE MEDIOS

FIG. 1


40
42
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46
54
52
44
58
48
48
56
60
50
50a
34
50

FIG. 2

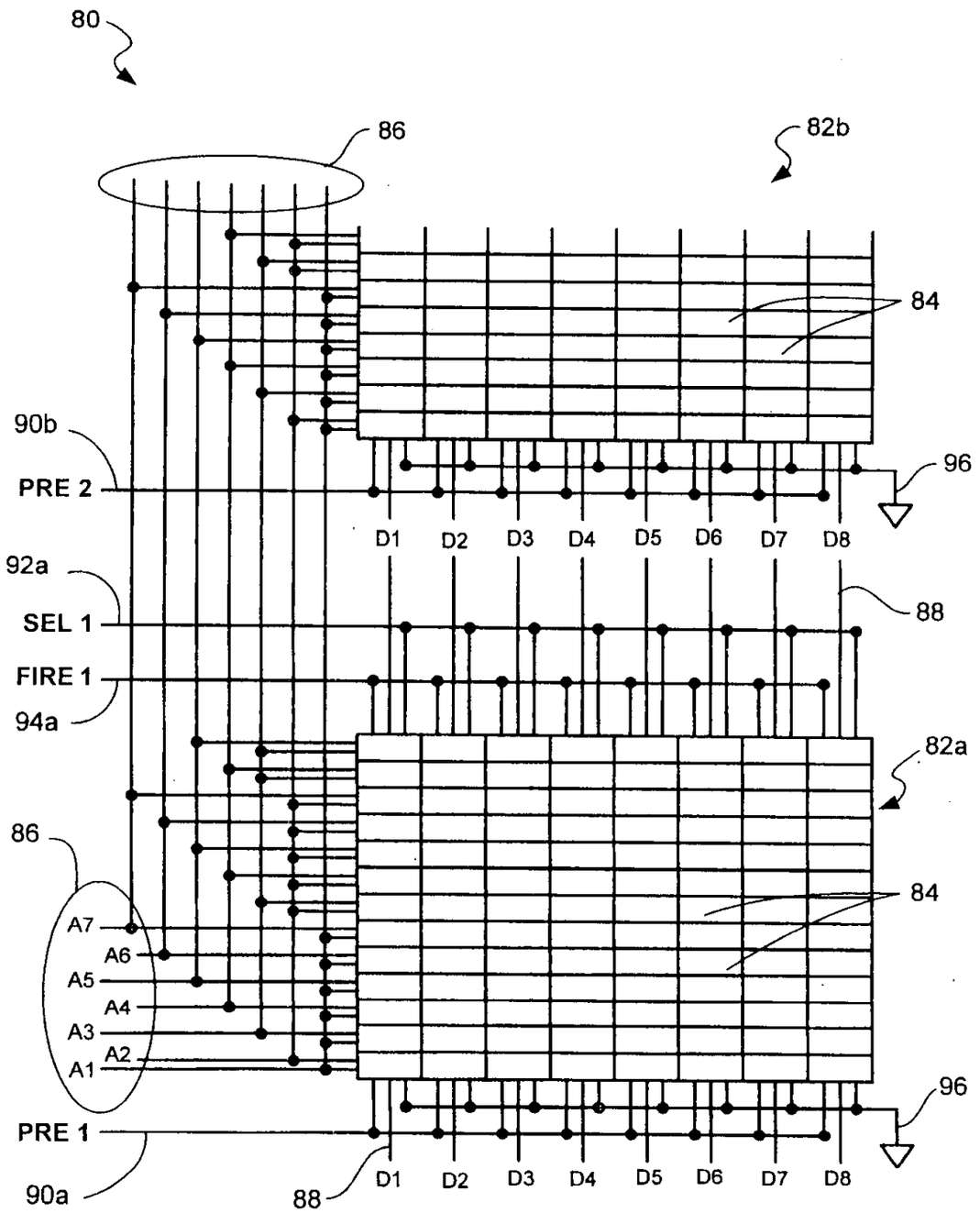
80
86
82b
84
90b
PRE 2
96
D1
D2
D3
D4
D5
D6
D7
D8
92a
SEL 1
88
FIRE 1
94a
82a
86
84
A7
A6
A5
A4
A3
A2
A1
96
PRE 1
90a
88
D1
D2
D3
D4
D5
D6
D7
D8

FIG. 3

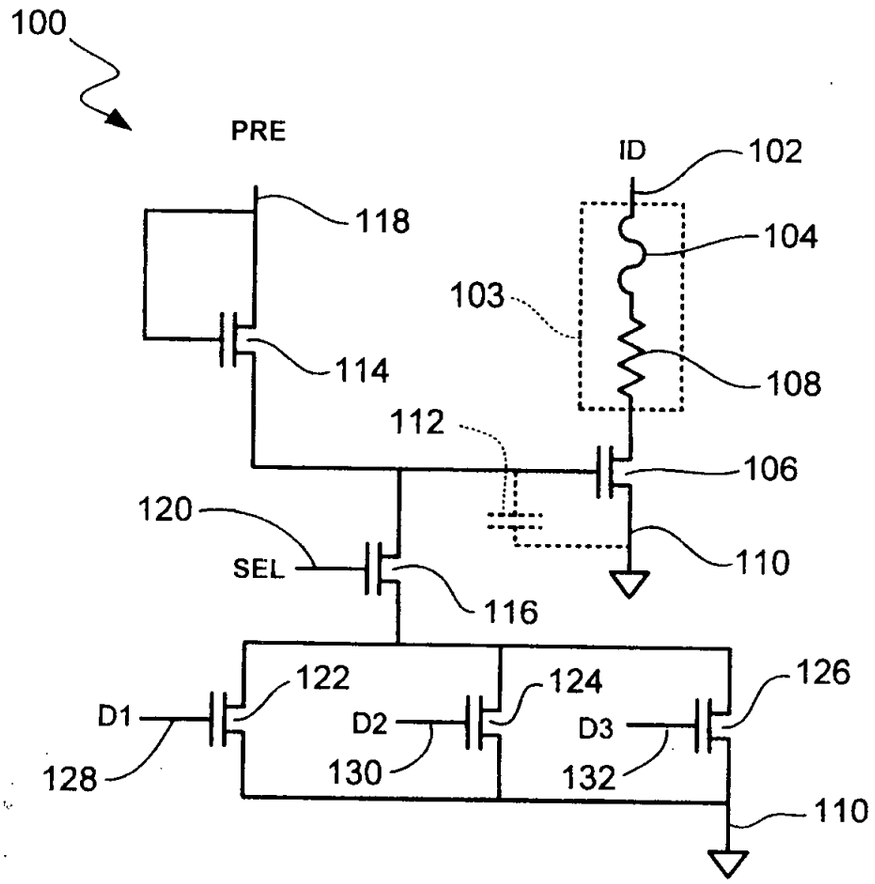
100
PRE
ID
102
118
104
103
114
108
112
106
120
SEL
110
116
122
124
126
D1
D2
D3
128
130
132
110

FIG. 4

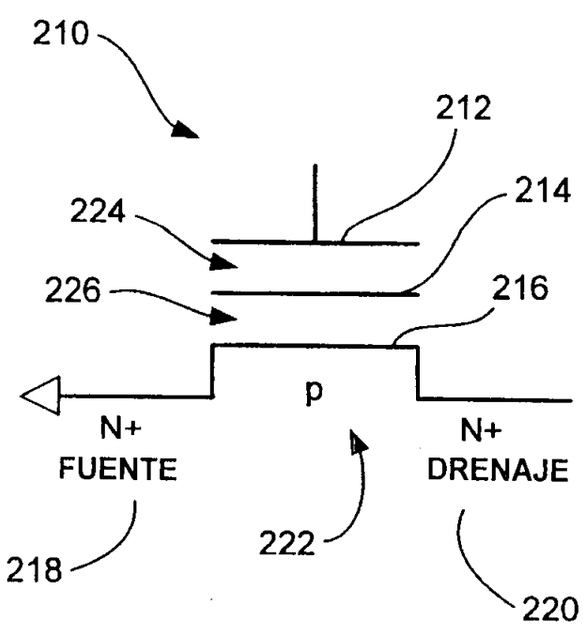
210
212
224
214
226
216
p
N+
FUENTE
N+
DRENAJE
218
222
220

FIG. 5

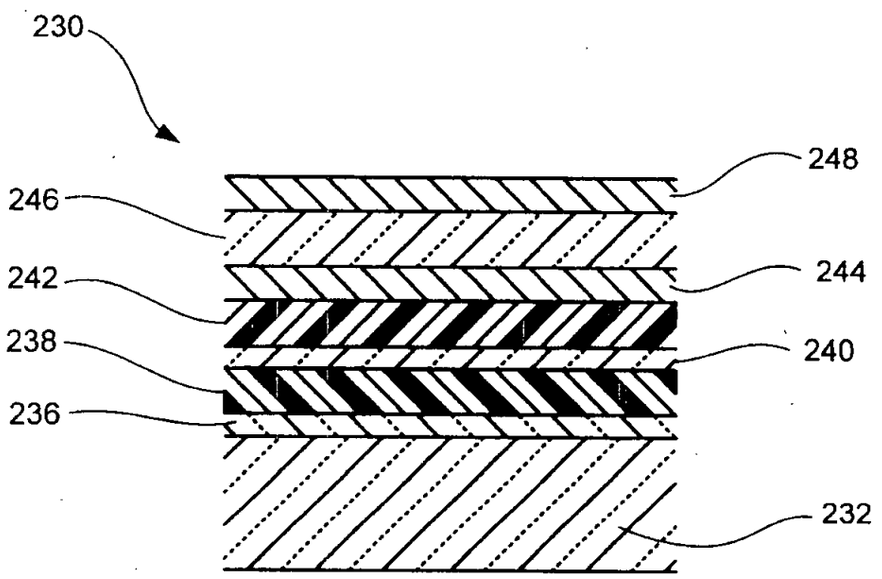
230
248
246
244
242
240
238
236
232

FIG. 6

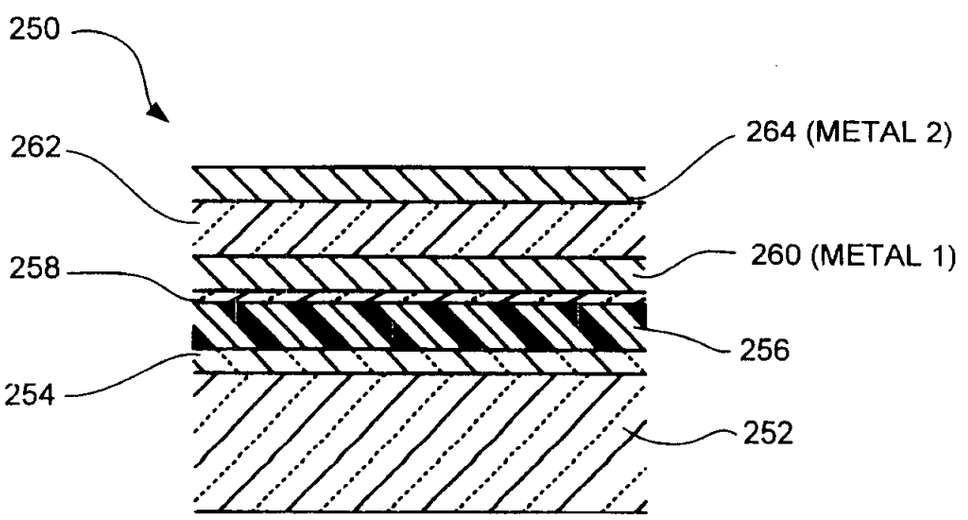
250
264 (METAL 2)
262
260 (METAL 1)
258
256
254
252

FIG. 7

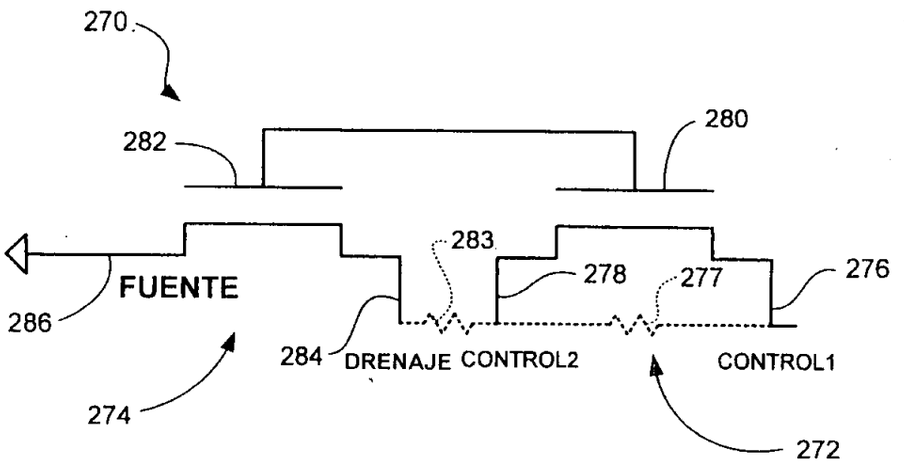
270
282
280
283
278
277
276
FUENTE
286
284
DRENAJE
CONTROL2
CONTROL1
274
272

FIG. 8

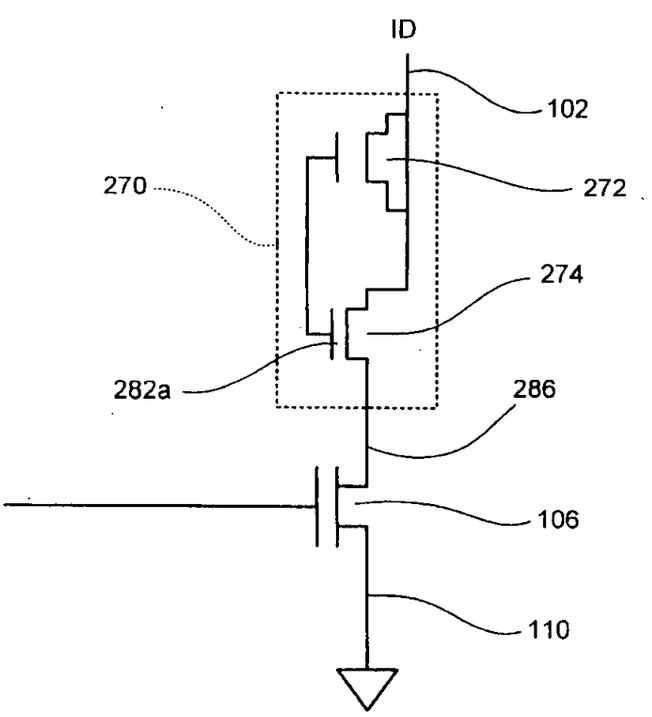
ID
102
270
272
274
282a
286
106
110

FIG. 9

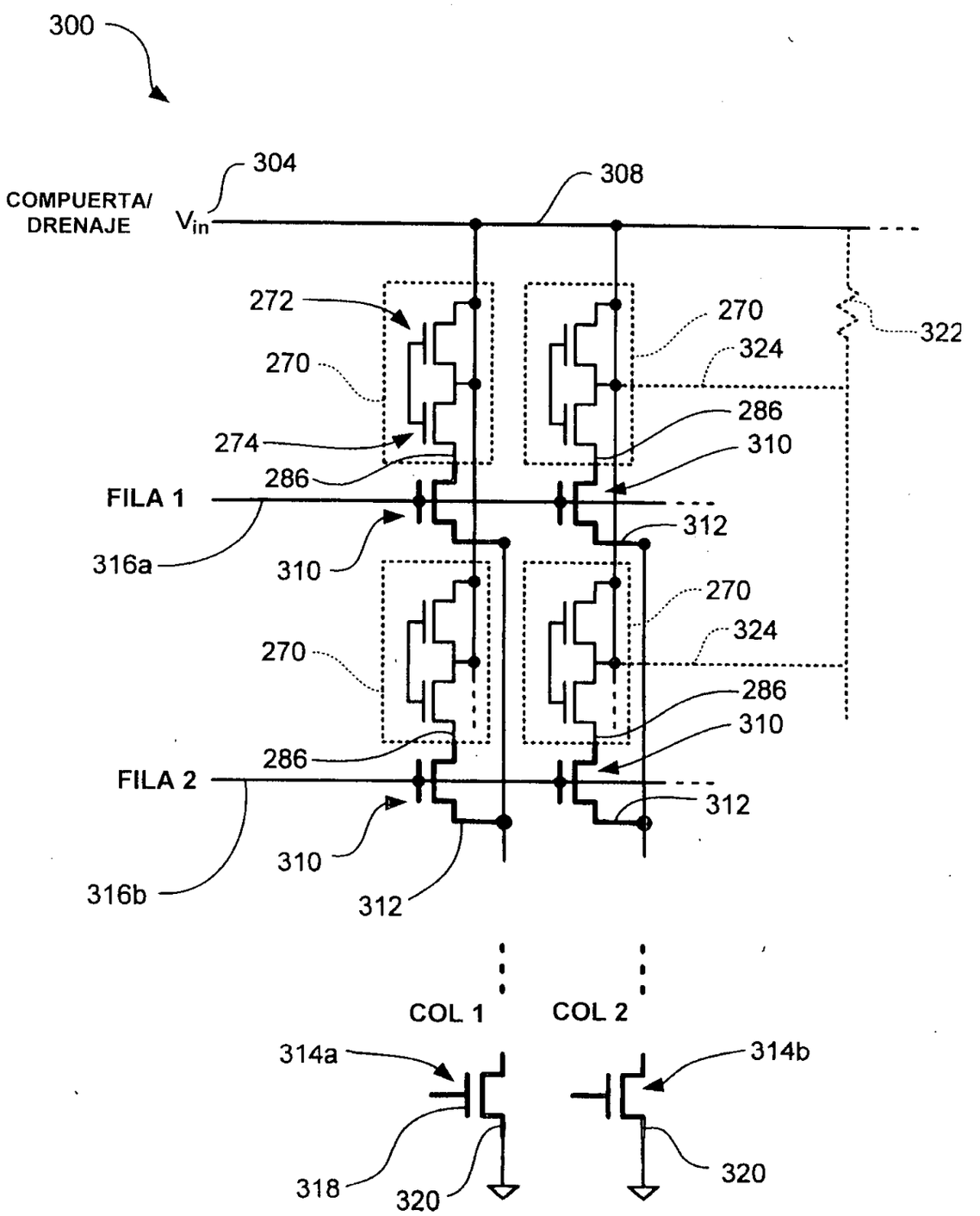
300
304
COMPUERTA/
DRENAJE
V_{in}
308
272
270
274
286
FILA 1
316a
310
312
322
324
FILA 2
316b
COL 1
COL 2
314a
314b
318
320

FIG. 10

WO 2007/120988
PCT/US2007/062644

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
AVAILABILITY OF THE PUBLICATION
OF THE INTERNATIONAL APPLICATION

To:

COULMAN, Donald, J.
Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400 Mail Stop 35
Fort Collins, Colorado 80527-2400
ETATS-UNIS D'AMERIQUE

Date of mailing (*day/month/year*)	
10 April 2008 (10.04.2008)	
Applicant's or agent's file reference 200600453-2	**IMPORTANT NOTICE**

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US2007/062644	23 February 2007 (23.02.2007)	23 February 2006 (23.02.2006)

Applicant
HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. et al

The applicant is hereby **notified** that the International Bureau:

☐ has **published** the above-indicated international application on under No. WO

☑ has **republished** the above-indicated international application on 10 April 2008 (10.04.2008) under No. WO 2007/120988
For an explanation as to the reason for this republication of the international application, reference is made to INID codes (15), (48) or (88) (*as the case may be*) on the front page of the published international application.

A copy of the international application is available for viewing and downloading on WIPO's website at the following address: http://www.wipo.int/pctdb (under "Query" enter the PCT or WO number).

The applicant may also request a paper copy of the published international application from the International Bureau by submitting a written request to PatentScope@wipo.int or to the address provided below.

The International Bureau of WIPO	Authorized officer

PATENT COOPERATION TREATY

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From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To:

HEWLETT-PACKARD COMPANY
Attn. Coulman, Donald J.
Intellectual Property Administration
P.O. Box 272400, Mail Stop 35
Fort Collins CO 80527-2400
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*	27/02/2008
Applicant's or agent's file reference: 200600453-2	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/US2007/062644	International filing date *(day/month/year)* 23/02/2007

Applicant

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

1. [X] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Roberta Andreatta

Form PCT/ISA/220 (October 2005)

(See notes on accompanying sheet)

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

PATENT COOPERATION TREATY

PCT

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
200600453-2		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2007/062644	23/02/2007	23/02/2006
Applicant		
HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

[X] the international application in the language in which it was filed

[ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title**,

[X] the text is approved as submitted by the applicant

[ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

[X] the text is approved as submitted by the applicant

[ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 8

[ ] as suggested by the applicant

[ ] as selected by this Authority, because the applicant failed to suggest a figure

[X] as selected by this Authority, because this figure better characterizes the invention

b. [ ] none of the figures is to be published with the abstract

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/062644

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/28 B41J2/05 G11C16/04
ADD. H01L21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L B41J G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 320 807 A (HYUNDAI ELECTRONICS IND [KR]) 1 July 1998 (1998-07-01) page 4, line 12 - page 8, line 11; figures 2,3	1-10
A	US 2005/099458 A1 (EDELEN JOHN G [US] ET AL) 12 May 2005 (2005-05-12) paragraphs [0002] - [0035]	1-10
X	US 6 324 097 B1 (CHEN CHUN-LIN [TW] ET AL) 27 November 2001 (2001-11-27)	1,8-10
A	column 3, line 1 - column 5, line 30; figures 2-9	2-7
A	US 6 222 764 B1 (KELLEY PATRICK J [US] ET AL) 24 April 2001 (2001-04-24) column 3, line 36 - column 5, line 27; figure 1	1-10

-/--

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2008	27/02/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Neumann, Andreas

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/062644

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/005543 A1 (DI PEDE LUIGI [CA] ET AL) 17 January 2002 (2002-01-17) paragraphs [0029] - [0036]; figure 1	1-10

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/062644

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2320807 A	01-07-1998	JP 10223784 A	21-08-1998
		US 5998830 A	07-12-1999
US 2005099458 A1	12-05-2005	AU 2004311068 A1	02-06-2005
		BR PI0416516 A	09-01-2007
		CN 1890101 A	03-01-2007
		EP 1691981 A2	23-08-2006
		US 2007216732 A1	20-09-2007
		US 2008007597 A1	10-01-2008
		WO 2005050702 A2	02-06-2005
US 6324097 B1	27-11-2001	US 2001049170 A1	06-12-2001
US 6222764 B1	24-04-2001	GB 2363679 A	02-01-2002
		JP 2001185632 A	06-07-2001
		KR 20010070297 A	25-07-2001
US 2002005543 A1	17-01-2002	NONE	

PATENT COOPERATION TREATY

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From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/062644	23.02.2007	23.02.2006

International Patent Classification (IPC) or both national classification and IPC
INV. H01L21/28 B41J2/05 G11C16/04
ADD. H01L21/8247

Applicant
HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	see form PCT/ISA/210	Neumann, Andreas Telephone No. +49 89 2399-6924

Form (PCT/ISA/237) (Cover Sheet) (April 2005)

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2007/062644

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2007/062644

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-10
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-10
Industrial applicability (IA)	Yes:	Claims	1-10
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (SEPARATE SHEET)

International application No.
PCT/US2007/062644

Re Item V

D1: GB-A-2 320 807 (HYUNDAI ELECTRONICS IND [KR]) 1 July 1998 (1998-07-01)
D2: US 2005/099458 A1 (EDELEN JOHN G [US] ET AL) 12 May 2005 (2005-05-12)
D3: US-B1-6 324 097 (CHEN CHUN-LIN ET AL) 27 November 2001 (2001-11-27)
D4: US-B1-6 222 764 (KELLEY PATRICK J [US] ET AL) 24 April 2001 (2001-04-24)
D5: US 2002/005543 A1 (DI PEDE LUIGI [CA] ET AL) 17 January 2002 (2002-01-17)

Articles 33(1) and 33(3) PCT

1. D1 (cf. fig.2B and associated text passages) discloses an EPROM cell on a semiconductor substrate 11 and comprising a single polysilicon layer (15A, 15B) and a conductive layer 18 above said polysilicon layer wherein the cell comprises a control transistor T1 having a floating gate 15A that comprises a portion of said polysilicon layer, an EPROM transistor T2 having a floating gate 15B that comprises a portion of said polysilicon layer, and an electrical interconnection comprising a portion of said conductive layer 18 that interconnects both floating gates 15A and 15B.

   The skilled person routinely, i.e. without the exercise of any inventive skill, uses EPROM cells such as the one of D1 in all circuits that require EPROM-type memory functionality. One of such routinely known uses concerns the control circuit of a printhead for an inkjet printer, as is illustrated for example by pars.2 and 17-20 of D2.

   The subject-matter of independent claim 1 is therefore not inventive over a combination of D1 with the skilled person's routine knowledge.

2. Claim 1 also lacks an inventive step over a combination of D3 with the skilled person's routine knowledge because D3 discloses in fig.9 and associated text passages a device very similar to the one of D1, wherein a single polysilicon layer is used for forming the floating gates 802 and 804. Therefore claim 1 lacks an inventive step for the same reason as indicated in item 1.

3. Claim 1 also lacks an inventive step over a combination of D4 with the skilled person's routine knowledge because D4 also discloses (see fig.1 and associated text passages) a single-polysilicon EPROM cell wherein the choice of providing

the interconnection 40 between the floating gates 26 and 34 is routinely done by means of a conductive layer overlying the polysilicon layer, as is illustrated by D1 and D3. Therefore claim 1 lacks an inventive step for a similar reason to the one indicated in item 1.

4. Claim 1 also lacks an inventive step over a combination of D5 with the skilled person's routine knowledge because D5 also discloses (see fig.1 and associated text passages) a single-polysilicon EPROM cell wherein the choice of providing the interconnection between the floating gates 12A and 12B is routinely done by means of a conductive layer overlying the polysilicon layer instead of by portions of the polysilicon layer itself, as is illustrated by D1 and D3. It is also noted that the possibility of connecting the two floating gates by portions of the single polysilicon layer is also contemplated in the present application (see p.16 ll.20-22). Therefore claim 1 lacks an inventive step for a similar reason to the one indicated in item 1.

5. The subject-matter of claims 2-10 is also considered not to be inventive in the sense of Article 33 PCT, see D1-D5 and the corresponding passages cited in the search report.

For the sake of completeness, the following is pointed out. Claims 2-7 require (resistive) connections between the source/drain regions of the control transistor as well as between the source/drain regions of the control transistor and the drain region of the EPROM transistor. It is clear that for example the source/drain regions 12A and 12C of the D1 control transistor T1 are connected by the channel 13A of said transistor, which implies that both regions are electrically connected through a resistance. There also clearly is a resistive path between said source/drain regions 12A/12C and the drain (either 12D or 12B) of the EPROM transistor T2 of D1. Therefore the additional features of claims 2-7 are disclosed in D1. The same argument also applies in view of the transistors and respective source/drain regions of the D4 (see fig.1) and D5 (see fig.1) devices.

Re Item VIII

Article 6 PCT

1. The additional feature of device claim 8 relates to a method of using the device without making the intended limitations clear in terms of device features, thereby leaving the category of the claim unclear.

2. The vague and imprecise statement in the description in lines 20-24 on page 4 implies that the subject-matter for which protection is sought may be different from that defined by the claims, thereby resulting in lack of clarity (Article 6 PCT) when used to interpret them.

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

Europäisches Patentamt
European Patent Office
Office européen des brevets

European Patent Office
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Fax +31 (0)70 340-3016

For any questions about this communication:
Tel.:+31 (0)70 340 45 00

Hewlett-Packard Development Company, L.P.
Hewlett-Packard Company,
Intellectual Property Administration
20555, S.H. 249
Houston, Texas 77070
ETATS-UNIS D'AMERIQUE

Date
16.04.08

Reference	Application No./Patent No.
	07778530.1 - 2203
Applicant/Proprietor	
Hewlett-Packard Development Company, L.P.	

The international search report, or the declaration under Article 17(2)(a) PCT, has been published under Article 21(3) and Rule 48 PCT on 10.04.08. That publication takes the place of the mention of publication of the European search report (Art. 153(6) EPC).

The request for examination must be filed within **six months** from the above date (Art. 153(6) in conjunction with R. 70(1) EPC). It is not deemed to have been filed until the examination fee has been paid (Art. 94(1) EPC). However, under Article 22 or 39 PCT in conjunction with Rule 159(1) EPC, the time limit for filing it does not expire before the end of the 31st month from the filing date (or earliest priority date). Payment of the designation fees must also be made within the above-mentioned period (R. 159(1) EPC). The same applies also for the extension fees.

If the request for examination is not filed in due time, and at least one designation fee is not paid, the European patent application shall be deemed to be withdrawn (Art. 94(2), R. 39(2)-(4) and R. 160(1) EPC).

For more details see the EPO brochure "How to get a European patent", Guide for applicants - Part 2, PCT procedure before the EPO - "Euro-PCT" (EPO PCT Guide).

Receiving Section

Europäisches Patentamt • European Patent Office • Office européen des brevets

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

To:
DONALD J. COULMAN
HEWLETT-PACKARD COMPANY
INTELLECTUAL PROPERTY ADMINISTRATION
P.O. BOX 272400 MAIL STOP 35
FORT COLLINS, COLORADO 80527-2400

Confirmation No: 1198

PCT

NOTIFICATION OF THE INTERNATIONAL APPLICATION NUMBER AND OF THE INTERNATIONAL FILING DATE

(PCT Rule 20.5(c))

Date of mailing *(day/month/year)*	10 Aug 2007
Applicant's or agent's file reference: 200600453-2	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/062644	23 Feb 2007	23 Feb 2006

Applicant: HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

Title of the invention: GATE-COUPLED EPROM CELL FOR PRINTHEAD

1. The applicant is hereby notified that the international application has been accorded the international application number and the international filing date indicated above.

2. The applicant is further notified that the record copy of the international application:

☒ was transmitted to the International Bureau on 10 Aug 2007

☐ has not yet been transmitted to the International Bureau for the reason indicated below and a copy of this notification has been sent to the International Bureau*:

☐ because the necessary national security clearance has not yet been obtained.

☐ because *(reason to be specified)*:

* The International Bureau monitors the transmittal of the record copy by the receiving Office and will notify the applicant (with Form PCT/IB/301) of its receipt. Should the record copy not have been received by the expiration of 14 months from the priority date, the International Bureau will notify the applicant (Rule 22.1(c)).

3. FOREIGN TRANSMITTAL LICENSE INFORMATION — Completed by: MW

☐ Additional license for foreign transmittal not required. This subject matter is covered by a license already granted or the equivalent U.S. national application. Refer to that license for information concerning its scope.

☐ License for foreign transmittal not required. 37 CFR 5.11(e)(1) or 37 CFR 5.11(e)(2). However, a license may be required for additional subject matter. See 37 CFR 5.15(b).

☒ Foreign transmittal license granted. 35 U.S.C. 184; 37 CFR 5.11 on 04 Aug 2007 (date):

☐ 37 CFR 5.15(a) ☒ 37 CFR 5.15(b)

Name and mailing address of the receiving Office	Authorized officer
Mail Stop PCT, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450	Misty Walker
Facsimile No. 571-273-3201	Telephone No. 703-308-9290 EX 122

Form PCT/RO/105 (July 1992)

WO 2007/120988
PCT/US2007/062644

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

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PCT

NOTIFICATION CONCERNING
AVAILABILITY OF THE PUBLICATION
OF THE INTERNATIONAL APPLICATION

To:

COULMAN, Donald, J.
Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400 Mail Stop 35
Fort Collins, Colorado 80527-2400
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 25 October 2007 (25.10.2007)	
Applicant's or agent's file reference 200600453-2	**IMPORTANT NOTICE**
International application No. PCT/US2007/062644	International filing date *(day/month/year)* 23 February 2007 (23.02.2007)
Priority date *(day/month/year)* 23 February 2006 (23.02.2006)	
Applicant HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. et al	

The applicant is hereby **notified** that the International Bureau:

☑ has **published** the above-indicated international application on 25 October 2007 (25.10.2007) under No. WO 2007/120988

☐ has **republished** the above-indicated international application on under No. WO
For an explanation as to the reason for this republication of the international application, reference is made to INID codes (15), (48) or (88) (*as the case may be*) on the front page of the published international application.

A copy of the international application is available for viewing and downloading on WIPO's website at the following address: http://www.wipo.int/pctdb (under "Query" enter the PCT or WO number).

The applicant may also request a paper copy of the published international application from the International Bureau by submitting a written request to PatentScope@wipo.int or to the address provided below.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Yoshiko Kuwahara

e-mail: pt07.pct@wipo.int

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From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
SUBMISSION OR TRANSMITTAL
OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

COULMAN, Donald, J.
Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400 Mail Stop 35
Fort Collins, Colorado 80527-2400
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 15 August 2007 (15.08.2007)	
Applicant's or agent's file reference 200600453-2	IMPORTANT NOTIFICATION
International application No. PCT/US2007/062644	International filing date *(day/month/year)* 23 February 2007 (23.02.2007)
International publication date *(day/month/year)* **Not yet published**	Priority date *(day/month/year)* 23 February 2006 (23.02.2006)
Applicant HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. et al	

1. By means of this Form, which replaces any previously issued notification concerning submission or transmittal of priority documents, the applicant is hereby notified of the date of receipt by the International Bureau of the priority document(s) relating to all earlier application(s) whose priority is claimed. Unless otherwise indicated by the letters "NR", in the right-hand column or by an asterisk appearing next to a date of receipt, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. *(If applicable)* The **letters "NR"** appearing in the right-hand column denote **a priority document which, on the date of mailing of this Form, had not yet been received by the International Bureau** under Rule 17.1(a) or (b). Where, under Rule 17.1(a), the priority document must be submitted by the applicant to the receiving Office or the International Bureau, but the applicant fails to submit the priority document within the applicable time limit under that Rule, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

3. *(If applicable)***An asterisk (*)** appearing next to a date of receipt, in the right-hand column, denotes **a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b)** (the priority document was received after the time limit prescribed in Rule 17.1(a) or the request to prepare and transmit the priority document was submitted to the receiving Office after the applicable time limit under Rule 17.1(b)). Even though the priority document was not furnished in compliance with Rule 17.1(a) or (b), the International Bureau will nevertheless transmit a copy of the document to the designated Offices, for their consideration. In case such a copy is not accepted by the designated Office as the priority document, Rule 17.1(c) provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
23 February 2006 (23.02.2006)	11/360,801	US	08 August 2007 (08.08.2007)

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Yoshiko Kuwahara
e-mail
Telephone No. +41 22 338 74 07

98

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING SUBMISSION OR TRANSMITTAL OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

COULMAN, Donald, J.
Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400 Mail Stop 35
Fort Collins, Colorado 80527-2400
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 15 August 2007 (15.08.2007)	
Applicant's or agent's file reference 200600453-2	IMPORTANT NOTIFICATION
International application No. PCT/US2007/062644	International filing date *(day/month/year)* 23 February 2007 (23.02.2007)
International publication date *(day/month/year)* **Not yet published**	Priority date *(day/month/year)* 23 February 2006 (23.02.2006)
Applicant HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. et al	

1. By means of this Form, which replaces any previously issued notification concerning submission or transmittal of priority documents, the applicant is hereby notified of the date of receipt by the International Bureau of the priority document(s) relating to all earlier application(s) whose priority is claimed. Unless otherwise indicated by the letters "NR", in the right-hand column or by an asterisk appearing next to a date of receipt, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. *(If applicable)* The **letters "NR"** appearing in the right-hand column denote **a priority document which, on the date of mailing of this Form, had not yet been received by the International Bureau** under Rule 17.1(a) or (b). Where, under Rule 17.1(a), the priority document must be submitted by the applicant to the receiving Office or the International Bureau, but the applicant fails to submit the priority document within the applicable time limit under that Rule, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

3. *(If applicable)***An asterisk (*)** appearing next to a date of receipt, in the right-hand column, denotes **a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b)** (the priority document was received after the time limit prescribed in Rule 17.1(a) or the request to prepare and transmit the priority document was submitted to the receiving Office after the applicable time limit under Rule 17.1(b)). Even though the priority document was not furnished in compliance with Rule 17.1(a) or (b), the International Bureau will nevertheless transmit a copy of the document to the designated Offices, for their consideration. In case such a copy is not accepted by the designated Office as the priority document, Rule 17.1(c) provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
23 February 2006 (23.02.2006)	11/360,801	US	08 August 2007 (08.08.2007)

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Yoshiko Kuwahara
e-mail
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99

PATENT COOPERATION TREATY

From the RECEIVING OFFICE

To:

DONALD J. COULMAN
HEWLETT-PACKARD COMPANY
INTELLECTUAL PROPERTY ADMINISTRATION
P.O. BOX 272400 MAIL STOP 35
FORT COLLINS, COLORADO 80527-2400

PCT

NOTIFICATION CONCERNING PAYMENT OF PRESCRIBED FEES

(PCT Rules 14, 15 and 16 and Administrative Instructions, Sections 102*bis*(c), 304, 323(b), 707(b) and 803)

Date of mailing *(day/month/year)*	10 Aug 2007
Applicant's or agent's file reference: 200600453-2	**PAYMENT DUE** see item 3 for time limits

International application No.	International filing date/Date of receipt *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/062644	23 Feb 2007	23 Feb 2006

Applicant: HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

1. The applicant is hereby notified that this receiving Office has received:

☒ **the payment** of all the prescribed fees, and ☐ **an overpayment**, which will be refunded in due course.

☐ **no or insufficient payment** of the prescribed fees and the applicant is hereby **invited to pay the balance due**, as summarized under item 2, within the time limit(s) indicated under item 3.

2. **Fees and payment calculation:**

3,442.00	–	3,442.00	=	0.00
Total fees payable		Amount paid		Balance

☐ The details of the calculation are given in the Annex.

3. **Time limit(s) for payment and amount(s) payable (Rules 14.1, 15.4 and 16.1(f)):**

☐ within ONE MONTH from the date of receipt of the international application (**for the transmittal fee** (if any), **the search fee** and **the international filing fee**). The amount payable for each fee is the amount applicable on the date of receipt of the international application.

☐ within 16 MONTHS from the priority date (only for the fee for priority document). The applicant's attention is drawn to the fact that the request made by the applicant under Rule 17.1(b) will be considered not to have been made unless the fee is paid within that time limit.

4. Additional observations *(if necessary)*:

☐ The search copy will not be transmitted to the International Searching Authority until the search fee is paid (therefore the start of the international search will be delayed) (Rule 23.1(a) and (b)).

Name and mailing address of the receiving Office	Authorized officer
Mail Stop PCT, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450	Misty Walker
Facsimile No. 571-273-3201	Telephone No. 703-308-9290 EX 122

Form PCT/RO/102 (January 2004)

100

ANNEX TO FORM PCT/RO/102
CALCULATION OF THE PRESCRIBED FEES

International application No.
PCT/US2007/062644

[T] Transmittal Fee

Prescribed amount:		300.00 [T]	
Amount paid:	–	300.00	[X] correct amount
Balance:	=	0.00	[ ] overpayment
			[ ] balance due

[S] Search Fee

Prescribed amount:		2,059.00 [S]	
Amount paid:	–	2,059.00	[X] correct amount
Balance:	=	0.00	[ ] overpayment
			[ ] balance due

[I] International Filing Fee

Fixed amount for first 30 sheets: 931.00 [i1]

11 (Number of sheets in excess of 30) x 12.00 (Fee per sheet) = 132.00 [i2]

Additional component: 400 x 0.00 (Fee per sheet) = 0.00 [i3]

Reduction where the international application is filed *(See PCT Applicant's Guide, Volume I, General Part, for details on the availability of this reduction)*:

using the PCT-EASY software:	–	0.00 [r]
or		
in electronic form where the text of the description, claims and abstract is not in character coded format:	–	0.00 [r]
or		
in electronic form where the text of the description, claims and abstract is in character coded format:	–	0.00 [r]
Sub-total:	=	1,063.00 [i1+i2+i3-r]

Prescribed total amount *(The amount to be entered at I is the sub-total entered at (i1+i2+i3-r), except where the applicant is (or all applicants are) entitled to a reduction of 75%, in which case the amount to be entered at I is 25% of the sub-total (i1+i2+i3-r); certain applicants from certain States are entitled to a reduction of 75% of the international filing fee; see Notes to the Fee Calculation Sheet as annexed to the Request Form, PCT/RO/101, for details)*:

	=	1,063.00 [I]	
Amount paid:	–	1,063.00	[X] correct amount
Balance:	=	0.00	[ ] overpayment
			[ ] balance due

[P] Fee for Priority Document

Prescribed amount:		20.00 [P]	
Amount paid:	–	20.00	[X] correct amount
Balance:	=	0.00	[ ] overpayment
			[ ] balance due

TRANSMITTAL LETTER TO THE UNITED STATES RECEIVING OFFICE

~~Express Mail mailing number~~: Filed Electronically	Date of Deposit: 23 February 2007
File reference no. 200600453-2	International Application no. (if known): Filed Herewith
Title of the invention: GATE COUPLED EPROM CELL FOR PRINTHEAD	
Earliest priority date claimed (Day/Month/Year): 23 February 2006	

__x__ This is a new International Application

SCREENING DISCLOSURE INFORMATION:

In order to assist in screening the accompanying international application for purposes of determining whether a license for foreign transmittal should and could be granted and for other purposes, the following information is supplied. (Check as many boxes as apply.):

_____ The invention disclosed was **not** made in the United States of America.

_____ There is no prior U.S. application relating to this invention.

__x__ The following prior U.S. application(s) contain subject matter which is related to the invention disclosed in the attached international application. *(Note: priority to these applications may or may not be claimed on the Request (form PCT/RO/101 and this listing does **not** constitute a claim for priority.)*

application no.	11/360,801	filed on	23 February 2006
application no.		filed on	
application no.		filed on	

_____ The present international application contains additional subject matter not found in the prior U.S. application(s) identified above. The additional subject matter is found on pages _____ and _____ **DOES NOT ALTER** ____ **MIGHT BE CONSIDERED TO ALTER** the general nature of the invention in a manner which would require the U.S. application to have been made available for inspection by the appropriate defense agencies under 35 U.S.C. 181 and 37 C.F.R. 5.15.

Itemized list of contents:

Sheets of Request form:	7	Check no:	Please charge deposit account 08-2025
Sheets of description (excluding sequence listing):	25	Return receipt postcard:	Enclosed
Sheets of claims:	2	Power of attorney:	Enclosed
Sheets of abstract:	1		
Sheets of drawings:	6	Certified copy of priority document (specify):	n/a
Sheets of sequence listing:	n/a		
Sequence listing diskette/CD	n/a	Other (specify):	PCT Easy/Safe Diskette
Tables related to sequence listing CD	n/a		

The person signing this form is:	_____ Applicant	Name of person signing: COULMAN, Donald J.
	__x__ Attorney/Agent (Reg. No.) 50,406	
	_____ Common Representative	Signature: Donald J. Coulman

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PCT REQUEST

Original (for **SUBMISSION**)

0	**For receiving Office use only**	
0-1	International Application No.	
0-2	International Filing Date	
0-3	Name of receiving Office and "PCT International Application"	

0-4	**Form PCT/RO/101 PCT Request**	
0-4-1	Prepared Using	PCT-SAFE [EASY mode] Version 3.51.015.190 MT/FOP 20061001/0.20.5.7
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	United States Patent and Trademark Office (USPTO) (RO/US)
0-7	**Applicant's or agent's file reference**	200600453-2
I	**Title of Invention**	GATE-COUPLED EPROM CELL FOR PRINTHEAD
II	**Applicant**	
II-1	This person is	applicant only
II-2	Applicant for	all designated States except US
II-4	Name	HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.
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II-7	State of residence	US
II-8	Telephone No.	+1 541 715 1694
II-9	Facsimile No.	+1 208 396 3958
II-10	e-mail	ipa.mail@hp.com

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PCT REQUEST

Original (for SUBMISSION)

III-1	**Applicant and/or Inventor**	
III-1-1	This person is	applicant and inventor
III-1-2	Applicant for	US only
III-1-4	Name (LAST, First)	BENJAMIN, Trudy L.
III-1-5	Address	18110 SE 34th Street Vancouver, Washington 98683 United States of America
III-1-6	State of nationality	US
III-1-7	State of residence	US
IV-1	**Agent or common representative; or address for correspondence**	
	The person identified below is hereby/ has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	agent
IV-1-1	Name (LAST, First)	COULMAN, Donald J.
IV-1-2	Address	Hewlett-Packard Company Intellectual Property Administration P.O. Box 272400 Mail Stop 35 Fort Collins, Colorado 80527-2400 United States of America
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IV-1-4	Facsimile No.	+1 208 396 3958
IV-1-5	e-mail	ipa.mail@hp.com
IV-1-8	Agent's registration No.	50,406
IV-2	**Additional agent(s)**	additional agent(s) with same address as first named agent
IV-2-1	Name(s)	FOR ADDITIONAL NAMES, Please See Attached General Power of Attorney
V	**DESIGNATIONS**	
V-1	**The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.**	
VI-1	**Priority claim of earlier national application**	
VI-1-1	Filing date	23 February 2006 (23.02.2006)
VI-1-2	Number	11/360,801
VI-1-3	Country	US

PCT REQUEST

Original (for **SUBMISSION**)

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VI-2	**Priority document request** The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s):	VI-1	
VII-1	**International Searching Authority Chosen**	European Patent Office (EPO) (ISA/EP)	
VIII	**Declarations**	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	1	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	1	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	1	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	-	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	-	

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VIII-1-1	Declaration: Identity of the inventor Declaration as to the identity of the inventor (Rules 4.17(i) and 51bis.1(a)(i))	in relation to this international application
	Name (LAST, First) Address	BENJAMIN, Trudy L. of 18110 SE 34th Street Vancouver, Washington 98683 United States of America is the inventor of the subject matter for which protection is sought by way of this international application

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VIII-2-1	**Declaration: Entitlement to apply for and be granted a patent** Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent (Rules 4.17(ii) and 51bis.1(a)(ii)), in a case where the declaration under Rule 4.17(iv) is not appropriate: Name (LAST, First)	in relation to this international application HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. is entitled to apply for and be granted a patent by virtue of the following:
VIII-2-1(iv)		an assignment from BENJAMIN, Trudy L. to HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P., dated 23 February 2006 (23.02.2006)

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VIII-3-1	**Declaration: Entitlement to claim priority** Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application specified below, where the applicant is not the applicant who filed the earlier application or where the applicant's name has changed since the filing of the earlier application (Rules 4.17(iii) and 51bis.1(a)(iii)) Name	in relation to this international application HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. is entitled to claim priority of earlier application No. 11/360,801 by virtue of the following:
VIII-3-1(iv)		an assignment from BENJAMIN, Trudy L. to HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P., dated 23 February 2006 (23.02.2006)

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PCT REQUEST

Original (for SUBMISSION)

IX	Check list	number of sheets	electronic file(s) attached
IX-1	Request (including declaration sheets)	7	✓
IX-2	Description	25	-
IX-3	Claims	2	-
IX-4	Abstract	1	✓
IX-5	Drawings	6	-
IX-7	TOTAL	41	
	Accompanying Items	paper document(s) attached	electronic file(s) attached
IX-8	Fee calculation sheet	✓	-
IX-11	Copy of general power of attorney	reference no. none	-
IX-17	PCT-SAFE physical media	-	✓
IX-19	**Figure of the drawings which should accompany the abstract**		
IX-20	**Language of filing of the international application**	English	
X-1	**Signature of applicant, agent or common representative**	Donald J. Coulman	
X-1-1	Name (LAST, First)	COULMAN, Donald J.	
X-1-2	Name of signatory		
X-1-3	Capacity		

FOR RECEIVING OFFICE USE ONLY

10-1	**Date of actual receipt of the purported international application**	
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/EP
10-6	**Transmittal of search copy delayed until search fee is paid**	

FOR INTERNATIONAL BUREAU USE ONLY

11-1	**Date of receipt of the record copy by the International Bureau**	

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PCT (ANNEX - FEE CALCULATION SHEET)

Original (for **SUBMISSION**)

(This sheet is not part of and does not count as a sheet of the international application)

0	**For receiving Office use only**			
0-1	International Application No.			
0-2	Date stamp of the receiving Office			
0-4	**Form PCT/ROM101 (Annex)** **PCT Fee Calculation Sheet**			
0-4-1	Prepared Using	PCT-SAFE [EASY mode] Version 3.51.015.190 MT/FOP 20061001/0.20.5.7		
0-9	**Applicant's or agent's file reference**	200600453-2		
2	**Applicant**	HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.		
12	**Calculation of prescribed fees**	fee amount/multiplier	Total amounts (USD)	
12-1	Transmittal fee T	⇨	300	
12-2-1	Search fee S	⇨	2059	
12-2-2	International search to be carried out by	EP		
12-3	International filing fee (first 30 sheets) I1	1086		
12-4	Remaining sheets	11		
12-5	Additional amount (X)	12		
12-6	Total additional amount I2	132		
12-7	I1 + I2 = I	1218		
12-12	EASY Filing reduction R	-78		
12-13	Total international filing fee (I-R) I	⇨	1140	
12-14	Fee for priority document Number of priority documents requested	1		
12-15	Fee per document (X)	20		
12-16	Total priority document fee: P	⇨	20	
12-17	**TOTAL FEES PAYABLE (T+S+I+P)**	⇨	3519	
12-19	**Mode of payment**	authorization to charge deposit account		
12-20	**Deposit account instructions** The receiving Office	United States Patent and Trademark Office (USPTO) (RO/US)		
12-20-1	Authorization to charge the total fees indicated above	✓		
12-20-2	Authorization to charge any deficiency or credit any overpayment in the total fees indicated above	✓		
12-20-3	Authorization to charge the fee for priority document	✓		
12-21	Deposit account No.	08-2025		
12-22	Date	09 February 2007 (09.02.2007)		
12-23	Name and signature	COULMAN, Donald J. Donald J.		

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13-2-6	Validation messages Declarations	Green? Manually inputted data. Please verify the contents of the information provided.
	Validation messages Declarations	Green? Manually inputted data. Please verify the contents of the information provided.
	Validation messages Declarations	Green? Manually inputted data. Please verify the contents of the information provided.
13-2-7	Validation messages Contents	Green? Figure of the drawings which should accompany the abstract not specified. Please verify.

An EPROM cell (270) in a printhead control circuit for an inkjet printer, having exactly one polysilicon layer (256) and a conductive layer (260) disposed above the polysilicon layer, includes a control transistor (272) and an EPROM transistor (274). The control and EPROM transistors each have floating gates (280, 282) comprising a portion of the polysilicon layer (256), and an electrical interconnection, comprising a portion of the conductive layer (260), interconnects the floating gate (280) of the control transistor (272) and the floating gate (282) of the EPROM transistor (274).

PCT

GENERAL POWER OF ATTORNEY

(for several international applications filed under the Patent Cooperation Treaty)

(PCT Rule 90.5)

The undersigned person(s) :

(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.
20555 S.H. 249
Houston, TX 77070
US

hereby appoint(s) the following person as: [X] agent [ ] common representative

Name and address

(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)

See attached page 2 for list of names. All appointed agents have the same addresses:

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to represent the undersigned before

[X] all the competent International Authorities

[ ] the International Searching Authority only

[ ] the International Preliminary Examining Authority only

in connection with any and all international applications filed by the undersigned with the following Office

United States Patent and Trademark Office as receiving Office

and to make or receive payments on behalf of the undersigned.

Signature(s) *(where there are several persons, each of them must sign; next to each signature, indicate the name of the person signing and the capacity in which the person signs, if such capacity is not obvious from reading this power):*

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.
by: HPQ HOLDINGS, LLC, its General partner

by: _____
Bloor Redding, Jr.
Assistant General Counsel, Intellectual Property
(Please see attached Statement of Authority to Sign)

Date: November 7 2006

Form PCT/Model of general power of attorney (for several international applications) (July 1992)

Attachment to PCT General Power of Attorney

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STATEMENT OF AUTHORITY TO SIGN
PCT GENERAL POWER OF ATTORNEY
(for several international applications filed under the Patent Cooperation Treaty)
(PCT Rule 90.5)

The undersigned, Bloor Redding, Jr., hereby certifies that he has been empowered to execute the accompanying PCT General Power of Attorney on behalf of HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

Please direct any questions you may have to the undersigned at the address and phone number below.

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

By: HPQ Holdings, LLC, its General Partner

By: _____
Bloor Redding, Jr.
Assistant General Counsel, Intellectual Property

Dated: November 7 2006

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400, m/s 35
Ft. Collins CO 80527-2400

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Attachment to PCT General Power of Attorney
Agents Authorized for Hewlett-Packard Development Company, L.P.
Shown with USPTO Registration Number

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POTTS, Jerry 27,091
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SCHUYLER, Marc 35,675
SIMMONS, Lane R. 37,721
STENSTROM, Dennis G. 28,910
STEVENS, Walter S. 33,098
STOKEY, Richard J. 40,383
STREETER, William J. 24,447
WADE, Matthew L. 42,206

WASSON, Robert D. 40,218
WINFIELD, Augustus W. 34,046
WISDOM, Gregg W. 40,231

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GATE-COUPLED EPROM CELL FOR PRINTHEAD

BACKGROUND

An inkjet printing system is a type of fluid ejection device, and includes a printhead, an ink supply, and an electronic controller that controls the printhead. The printhead ejects liquid ink drops through an array of orifices or nozzles disposed in a die by rapidly heating small volumes of ink located in vaporization chambers. The ink is heated with small electric heaters, such as thin film resistors or firing resistors. Heating the ink causes a portion of the liquid ink to vaporize and thereby eject a single drop through the nozzle toward a sheet of print medium, such as a sheet of paper, to print an image. The ink nozzles are typically arranged in one or more arrays in the printhead die, such that properly sequenced ejection of ink from the nozzles causes characters or other images to be printed as the printhead scans across the print medium.

To eject each drop of ink, the electronic controller that controls the printhead activates an electrical current from a power supply external to the printhead. The electrical current passes through a selected firing resistor to heat the ink in a corresponding selected vaporization chamber and eject the ink through a corresponding nozzle. Known drop generators include a firing resistor, a corresponding vaporization chamber, and a corresponding nozzle.

In inkjet printing systems it is desirable to have several characteristics of each print cartridge easily identifiable by a controller, and it is desirable to have such identification information supplied directly by the print cartridge. This "identification information" can provide information to the controller to adjust the operation of the printer and ensure correct operation. Additionally, as the different types of fluid ejection devices and their operating parameters increase,

there is a need to provide a greater amount of identification information without adding further interconnections to the flex tab circuit or increasing the size of the die to provide such identification information.

For these and other reasons, pen identification cells have been developed and integrated with the circuitry of inkjet printhead dies. In one configuration, the printhead circuitry is a negative-channel metal-oxide semiconductor (NMOS) circuit, and the identification cells are configured to be addressed individually. Each identification cell includes an identification bit that stores one bit of information.

The identification bits of the identification cells typically employ fuses and, though they are different from standard programmable read-only memory (PROM) chips, these bits are programmed and used in basically the same way. To program the chip, a relatively high current is selectively routed to certain fuses to cause them to burn out. Bits where fuses remain have a value of 1, while those where the fuses have been burned out provide a value of 0 in the binary logic of the circuit.

Programming and using ROM chips in this way has some drawbacks. If a chip is improperly programmed initially, there is no way to fix it, and the chip must be discarded. Additionally, fuses are relatively large, and can be unreliable. In inkjet printhead circuits, for example, fuses can damage the inkjet orifice layer during programming, and after a fuse burns out, metal debris from the fuse can be drawn into the ink and cause blockage in a pen, or result in poor quality printing.

In recent years, electronically programmable read-only memory (EPROM) devices have also been developed. Unlike PROM chips, EPROM chips do not include fuses. Like typical ROM chips, EPROMs include a conductive grid of columns and rows. The cell at each intersection has two gates that are separated from each other by a thin oxide layer that acts as a dielectric. One of the gates is called a floating gate and the other is called a control gate or input gate. The floating gate's only link to the row is through the control gate. A blank EPROM has all of the gates fully open, giving each cell a

value of 1. That is, the floating gate initially has no charge, which causes the threshold voltage to be low.

To change the value of the bit to 0, a programming voltage (e.g. 10 to 16 volts) is applied to the control gate and drain. This programming voltage draws excited electrons to the floating gate, thereby increasing the threshold voltage. The excited electrons are pushed through and trapped on the other side of the thin oxide layer, giving it a negative charge. These negatively charged electrons act as a barrier between the control gate and the floating gate. During use of the EPROM cell, a cell sensor monitors the threshold voltage of the cell. If the threshold voltage is low (below the threshold level), the cell has a value of 1. If the threshold voltage is high (above the threshold level), the cell has a value of zero.

Because EPROM cells have two gates at each intersection, an EPROM chip requires additional layers compared to a standard NMOS or PROM chip, including many such chips that are frequently used in inkjet printhead circuits. Consequently, while some of the drawbacks of fuses in NMOS circuits could be eliminated by the application of EPROM circuitry, the use of a typical EPROM cell either requires that the chip be provided with additional layers, which increases the cost and complexity of the chip, or that a separate EPROM chip be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Various features and advantages of the invention will be apparent from the detailed description which follows, taken in conjunction with the accompanying drawings, which together illustrate, by way of example, features of the invention, and wherein:

FIG. 1 is a block diagram of one embodiment of an ink jet printing system;

FIG. 2 is a diagram illustrating a portion of one embodiment of a printhead die;

FIG. 3 is a schematic diagram illustrating one embodiment of an ink jet printhead firing cell array;

FIG. 4 is a schematic diagram of one embodiment of an identification cell in one embodiment of a printhead die;

FIG. 5 is a schematic diagram of a typical EPROM transistor;

FIG. 6 is a cross-sectional view showing the circuitry layers in a typical EPROM chip;

FIG. 7 is a cross-sectional view showing the layers in one embodiment of an ink jet printhead die providing the circuitry shown in FIG. 3;

FIG. 8 is a schematic diagram of one embodiment of a gate-coupled EPROM cell that can be adapted for use as an identification bit in the printhead circuitry of FIG. 4;

FIG. 9 is a schematic diagram of one embodiment of an identification cell having a gate-coupled EPROM identification bit; and

FIG. 10 is a schematic diagram of an array of gate-coupled EPROM cells for a printhead circuit.

DETAILED DESCRIPTION

Reference will now be made to exemplary embodiments illustrated in the drawings, and specific language will be used herein to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended. Alterations and further modifications of the inventive features illustrated herein, and additional applications of the principles of the invention as illustrated herein, which would occur to one skilled in the relevant art and having possession of this disclosure, are to be considered within the scope of the invention.

Shown in FIG. 1 is a block diagram of one embodiment of an inkjet printing system 20. The inkjet printing system generally includes an inkjet printhead assembly 22, and a fluid supply assembly, such as the ink supply assembly 24. The inkjet printing system also includes a mounting assembly 26, a media transport assembly 28, and an electronic controller 30. A power supply 32 provides power to the various electrical components of the system.

In the embodiment shown in FIG. 1, the inkjet printhead assembly 22 includes at least one printhead or printhead die 40 that ejects drops of ink

through a plurality of orifices or nozzles 34 toward a print medium 36, so as to print onto the print medium. The print medium can be any type of suitable sheet material, such as paper, card stock, transparencies, Mylar®, fabric, and the like. Typically, the nozzles 34 are arranged in one or more columns or arrays such that properly sequenced ejection of ink from the nozzles causes characters, symbols, and/or other graphics or images to be printed upon print medium as the inkjet printhead assembly and print medium are moved relative to each other. The printhead 40 is one embodiment of a fluid ejection device. While the following description refers to the ejection of ink from the printhead assembly 22, it is to be understood that other liquids, fluids or flowable materials, including clear fluid, may be ejected from the printhead assembly.

The ink supply assembly 24 is one embodiment of a fluid supply assembly, and provides ink to the printhead assembly 22. The ink supply assembly includes a reservoir 38 for storing ink, which flows from the reservoir to the inkjet printhead assembly. The ink supply assembly and inkjet printhead assembly can form either a one-way ink delivery system or a recirculating ink delivery system. In a one-way ink delivery system, substantially all of the ink provided to the inkjet printhead assembly is consumed during printing. In a recirculating ink delivery system, only a portion of the ink provided to the printhead assembly is consumed during printing. In such a system, ink not consumed during printing is returned to the ink supply assembly.

In one embodiment of an inkjet printing system, the inkjet printhead assembly 22 and ink supply assembly 24 are housed together in an inkjet cartridge or pen. Alternatively, the ink supply assembly can be separate from the inkjet printhead assembly, and provide ink to the inkjet printhead assembly through an interface connection, such as a supply tube (not shown). In either embodiment, the reservoir 38 can be removed, replaced, and/or refilled.

The mounting assembly 26 positions the inkjet printhead assembly 22 relative to the media transport assembly 28, which positions the print medium 36 relative to the inkjet printhead assembly. A print zone 37 is thus defined adjacent to the nozzles 34 in an area between the inkjet printhead assembly and the print medium. The inkjet printhead assembly can be a scanning type

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printhead assembly, wherein the mounting assembly includes a carriage (not shown) for moving the inkjet printhead assembly relative to the media transport assembly to scan the print medium. Alternatively, the inkjet printhead assembly can be a non-scanning type printhead assembly, wherein the mounting assembly fixes the inkjet printhead assembly at a prescribed position relative to the media transport assembly 28.

The electronic controller or printer controller 30 typically includes a processor, firmware, and other electronics, or any combination thereof, for communicating with and controlling the inkjet printhead assembly 22, the mounting assembly 26, and the media transport assembly 28. The electronic controller receives data 39 from a host system, such as a computer, and usually includes memory (not shown) for temporarily storing the data. Typically, the data is sent to the inkjet printing system 20 along an electronic, infrared, optical, or other information transfer path. The data represents, for example, a document to be printed, and includes one or more print job commands and/or command parameters, thereby forming a print job for the inkjet printing system. The pattern of ejected ink drops is determined by the print job commands and/or command parameters.

The inkjet printhead assembly 22 can include one printhead 40, or it can be a wide-array or multi-head printhead assembly. The inkjet printhead assembly can include a carrier, which carries the printhead dies, provides electrical communication between the printhead dies and electronic controller 30, and provides fluidic communication between the printhead dies and the ink supply assembly 24.

Provided in FIG. 2 is a diagram illustrating a portion of one embodiment of a printhead die 40. The printhead die includes an array of printing or fluid ejecting elements 42. The printing elements are formed on a substrate 44, which has an ink feed slot 46 formed therein. The ink feed slot provides a supply of liquid ink to the printing elements, and is one embodiment of a fluid feed source. Other embodiments of fluid feed sources include but are not limited to corresponding individual ink feed holes feeding corresponding

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vaporization chambers and multiple shorter ink feed trenches that each feed corresponding groups of fluid ejecting elements.

A thin-film structure 48 is provided with an ink feed channel 54 formed therein. This channel communicates with the ink feed slot 46 formed in the substrate 44. An orifice layer 50 has a front face 50a and a nozzle opening 34 formed in the front face. The orifice layer also has a nozzle chamber or vaporization chamber 56 formed therein, which communicates with the nozzle opening and the ink feed channel of the thin-film structure. A firing resistor 52 is positioned within the vaporization chamber, and conductive leads 58 electrically couple this firing resistor to circuitry controlling the application of electrical current through selected firing resistors. As used herein, the term "drop generator" 60 includes the firing resistor 52, the nozzle chamber or vaporization chamber 56 and the nozzle opening 34.

During printing, ink flows from the ink feed slot 46 to the vaporization chamber 56 via the ink feed channel 54. The nozzle opening 34 is operatively associated with the firing resistor 52, such that droplets of ink within the vaporization chamber are ejected through the nozzle opening (e.g., substantially normal to the plane of the firing resistor) and toward the print medium 36 upon energizing of the firing resistor.

There are a variety of types of printhead dies. These include thermal printheads, piezoelectric printheads, electrostatic printheads, and any other type of fluid ejection device known in the art that can be integrated into a multi-layer structure. The substrate 44 can be formed, for example, of silicon, glass, ceramic, or a stable polymer, and the thin-film structure 48 can be formed to include one or more passivation or insulation layers of silicon dioxide, silicon carbide, silicon nitride, tantalum, polysilicon glass, or other suitable material. The thin-film structure also includes at least one conductive layer, which defines the firing resistor 52 and leads 58. The conductive layer can be made of, for example, aluminum, silver, gold, tantalum, tantalum-aluminum, or other metal or metal alloy. Firing cell circuitry, such as described in detail below, can be implemented in the substrate and thin-film layers.

The orifice layer 50 can be of a photoimageable epoxy resin, such as an epoxy referred to as SU8, marketed by Micro-Chem, of Newton, Massachusetts. Techniques for fabricating the orifice layer with SU8 or other polymers are well known to those of skill in the art. In one embodiment, the orifice layer is formed of two separate layers, referred to as a barrier layer (e.g., a dry film photo resist barrier layer) and a metal orifice layer (e.g., a nickel, copper, iron/nickel alloys, palladium, gold, or rhodium layer) formed over the barrier layer. Other suitable materials can also be employed to form the orifice layer.

Shown in FIG. 3 is a schematic diagram of a portion of one embodiment of an inkjet printhead firing cell circuit 80. The firing cell circuit includes a plurality of fire groups 82 (e.g. six fire groups), each fire group comprising an array of pre-charged firing cells 84. A first fire group 82a and a portion of a second fire group 82b are shown in FIG. 3. The pre-charged firing cells in each fire group are schematically arranged into 13 rows and eight columns. The number of pre-charged firing cells and their layout may vary as desired.

The eight columns of pre-charged firing cells 84 are electrically coupled to eight data lines 88, labeled D1-D8. Each of the firing cells in each column of pre-charged firing cells is electrically coupled to one of the data lines, and these data lines extend to the corresponding columns of pre-charged firing cells in fire group 82b and subsequent fire groups (not shown).

The rows of pre-charged firing cells 84 are electrically coupled to address lines 86, labeled A1-A7, that receive address signals. Each pre-charged firing cell in a row of pre-charged firing cells, referred to herein as a row subgroup or subgroup, is electrically coupled to the same pair of the address lines, this pair being unique for each row subgroup. The array of firing cells shown in the fire group 82 includes 13 row subgroups, but it will be apparent that the array can include any suitable number of subgroups. The address lines also extend to connect with row subgroups of fire group 82b and subsequent fire groups (not shown).

The pre-charge line 90a (labeled PRE 1) receives a pre-charge signal, and provides the pre-charge signal to all of the pre-charged firing cells 84 in the

first fire group 82a. Additional fire groups each have a separate pre-charge line, such as pre-charge line 90b (labeled PRE2) for fire group 82b.

A select line 92a (labeled SEL 1) receives a select signal and provides this select signal to all firing cells 84 in a corresponding fire group 82 and a fire line 94a (labeled FIRE 1) provides a fire signal to all pre-charged firing cells in the associated fire group. The fire line is electrically coupled to the firing resistors (52 in FIG. 2) of all pre-charged firing cells 84 in one fire group. Additional fire groups each have their own separate select and fire lines.

Additionally, all pre-charged firing cells 84 in the array 80 are electrically coupled to a reference line 96 that is tied to a reference voltage, such as ground. Given this structure, the pre-charged firing cells in a row subgroup of pre-charged firing cells are electrically coupled to the same address lines 86, pre-charge line 90, select line 92, fire line 94, and ground line 96.

The firing cells 84 cause the individual firing resistors (52 in FIG. 2) of the ink nozzles to selectively operate, so as to eject ink in the desired pattern. The fire groups are first precharged through the respective PRE lines 90. Address signals are provided on the address lines 86 to address one row subgroup in each of the fire groups 82, including one row subgroup in the pre-charged fire group. Data signals are provided on data lines 88 to provide data to all fire groups, including the addressed row subgroup in the pre-charged fire group. Next, a select signal is provided on the select line 92 of the pre-charged fire group to select the pre-charged fire group. The select signal defines a discharge time interval for discharging the node capacitance on each drive switch (not shown) in a pre-charged firing cell that is either not in the addressed row subgroup in the selected fire group or addressed in the selected fire group and receiving a high level data signal. The node capacitance does not discharge in pre-charged firing cells that are addressed in the selected fire group and receiving a low-level data signal. A high voltage level on the node capacitance turns the drive switch on (conducting).

After drive switches in the selected fire group 82 are set to conduct or not conduct, an energy pulse or voltage pulse is provided on the fire line 94 of the selected fire group. Pre-charged firing cells 84 that have conducting drive

switches conduct current through the firing resistor (52 in FIG. 2) to heat ink and eject ink from the corresponding drop generator (60 in FIG. 2). In operation, the plurality of fire groups 82 can be selected to fire in succession, or other sequences, and non-sequential selections may also be utilized. The address signals provided on the address lines 86 can be set to one row subgroup address during each cycle through the fire groups, and thereby cycle through the 13 row subgroup addresses in each fire group before repeating a row subgroup address. After the last row subgroup, address signals select the first row subgroup to begin the address cycle over again.

With fire groups 82 operated in succession, the select signal for one fire group is used as the pre-charge signal for the next fire group. The pre-charge signal for one fire group precedes the select signal and fire signal for the one fire group. After the pre-charge signal, data signals are multiplexed in time and stored in the addressed row subgroup of the one fire group by the select signal. The select signal for the selected fire group is also the pre-charge signal for the next fire group. After the select signal for the selected fire group is complete, the select signal for the next fire group is provided. Pre-charged firing cells 84 in the selected subgroup fire or heat ink based on the stored data signal as the fire signal, including an energy pulse, is provided to the selected fire group.

As noted above, it can be desirable to provide a greater amount of identification information in the printhead circuit, without adding further interconnections to the flex tab circuit or increasing the size of the die to provide such identification information. Accordingly, identification cells have been developed that can be included in the printhead circuitry, such as that shown in FIG. 3. Provided in FIG. 4 is a schematic diagram of one embodiment of an identification cell 100 that can be fabricated in the circuitry of one embodiment of a printhead die (40 in FIGS. 1 & 2). The printhead die can include a plurality of such identification cells electrically coupled to one identification line 102 which receives an identification signal and provides the identification signal to the identification cells.

The identification cell 100 includes a memory element or identification bit, indicated at 103. The memory element stores one bit of information. In one

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embodiment, depicted in FIG. 4, the memory element comprises a fuse, represented by fuse element 104 and fuse resistance 108. The identification cell includes a drive transistor or drive switch 106 electrically coupled to the memory element 103. The drive switch can be a FET (Field Effect Transistor) having a drain-source path that is electrically coupled at one end to one terminal of the memory element and at the other end to a reference 110, such as ground. The other terminal of the memory element is electrically coupled to the identification line 102. The identification line receives an identification signal and provides the identification signal to the memory element. The identification signal, including the program signal and the read signal, can be conducted through the memory element if the drive switch 106 is turned on (conducting). This allows for only specific identification cells on a single identification line to respond to read and programming signals on the identification line, while other identification cells on the same identification line do not respond to the read and programming signals.

The gate of the drive switch 106 forms a storage node capacitance 112, which functions as a memory to store charge pursuant to the sequential activation of the pre-charge transistor 114 and the select transistor 116. The drain-source path and gate of the pre-charge transistor are electrically coupled to the pre-charge line 118 that receives a pre-charge signal. The pre-charge line can be electrically connected to the pre-charge line 90 in FIG. 3.

The gate of the drive switch 106 is a control input that is electrically coupled to the drain-source path of the pre-charge transistor 114 and the drain-source path of the select transistor 116. The gate of the select transistor is electrically coupled to the select line 120 that receives a select signal. The select transistor can be electrically connected to the select line (92 in FIG. 3). The storage node capacitance 112 is shown in dashed lines, as it is part of the drive switch 106. Alternatively, a capacitor separate from the drive switch can be used to store charge.

The identification cell also includes a first transistor 122, a second transistor 124 and a third transistor 126 having drain-source paths that are electrically coupled in parallel. The parallel combination of these three

transistors is electrically coupled between the drain-source path of the select transistor 116 and the reference 110. The serial circuit including the select transistor coupled to the parallel combination of the first, second and third transistors is electrically coupled across the node capacitance 112 of the drive switch 106.

The gates of the first, second, and third transistors, 122, 124 and 126, are electrically coupled to three of the data lines of the associated fire group (82 in FIG. 3). The three data lines so connected can be any unique group of three of the eight data lines D1-D8 associated with the corresponding fire group. As shown in FIG. 4, the data lines can be those labeled DI-D3 in the fire group 82 in FIG. 3.

The pre-charge signal can be the pre-charge signal provided on pre-charge line 90a (labeled PRE 1) to the fire group 82, and the select signal can be the select signal provided on select line 92a (labeled SEL 1) to the fire group 82 in FIG. 3. To program the memory element 103, the identification cell 100 receives enabling signaling, including the pre-charge signal, select signal and data signals D1-D3 to turn on the drive switch 106. The identification line 102 provides the program signal in the identification signal to the memory element. The program signal provides a relatively high voltage (e.g. 16 volts) through the memory element to the conducting drive switch and reference 110. This high voltage changes the state of the memory element from a low resistive state to a high resistive state by burning out the fuse 104.

To read the state of the memory element 103, the identification cell 100 receives enabling signaling, including the pre-charge signal, select signal and data signals DI-D3 to turn on the drive switch 106. The identification line 102 provides the read signal in the identification signal to the memory element. The read signal provides a current through the memory element to the conducting drive switch 106 and reference 110. The voltage on the identification line can be detected to determine the resistive state of the memory element. In one embodiment, the memory element is determined to be in the high resistive state if the resistance is greater than about 1000 ohms (i.e. the fuse is burned out)

and in the low resistive state if the resistance is less than about 400 ohms (i.e. the fuse is intact).

Using the configuration of FIG. 4, each identification cell 100 can be individually enabled, and thereby can be programmed on an individual basis. Also, since the identification cells can be read individually, the combinations utilized to store data are greatly increased. For example, a single identification cell can be utilized in multiple combinations that each represents different information.

With three of eight data signals DI-D8 selecting each identification cell 100 in a plurality of identification cells, up to fifty six different identification cells can be selected by combinations of three of the eight data signals. Thus, with one pre-charge line, one select line, eight data lines, and one identification line the circuit can control fifty six identification bits, or about 5.1 identification cell bits per control line. Alternatively, each identification cell can be configured to respond to any suitable number of data signals, such as two or four or more data signals.

It should be noted that while Figure 4 discloses utilizing a single identification line 102 that is coupled to each of the identification cells 100, more than one identification line may be utilized, thus allowing a larger number of identification cells. Also, the number of identification cells that are provided may be more or less than 56 depending of factors such as the size of the die, the operating parameters of the fluid ejection device, or other considerations. Also, the number of identification cells that are encoded with information may be less than the total number of identification cells on the die.

While the identification cell configuration described above can be used in a variety of ways to store identification information on the printhead, fuses present some drawbacks noted earlier. The inventor has recognized that electronically programmable read-only memory, or EPROM, can be desirable to eliminate fuses in NMOS circuits, such as in ink jet printheads and other applications. EPROM cells do not include fuses, and provide a number of advantages over NMOS bits.

Shown in FIG. 5 is a schematic diagram of a typical EPROM cell or bit 210. An EPROM cell generally includes an input gate 212 (also called a control gate), a floating gate 214, and a semiconductor substrate 216 that includes a source 218 and a drain 220. As shown in FIG. 5, the substrate is provided with N+ doped regions adjacent to the source and drain, respectively, and a p doped region 222 therebetween. The control gate and floating gate are capacitively coupled together, with a dielectric material 224 between them, such that the control gate voltage is coupled to the floating gate. Another layer of dielectric material 226 is also disposed between the floating gate 214 and the semiconductor substrate 216.

A high voltage bias on the drain 220 generates energetic "hot" electrons. A positive voltage bias between the control gate 212 and the drain pulls some of these hot electrons onto the floating gate 214. As electrons are pulled onto the floating gate, the threshold voltage of the cell, that is, the voltage required to cause the gate/drain to conduct current, increases. If sufficient electrons are pulled onto the floating gate, those electrons will block current flow such that the threshold voltage will eventually increase to a level above a desired threshold voltage (e.g. the operating voltage of the circuit). This will cause the cell to block current at that voltage level, which changes the operating state of the cell from a 1 to a zero. After programming of the cell, a cell sensor (not shown) is used during normal operation to detect the state of the EPROM cell.

Because EPROM cells include two gates at each bit location, these chips require more layers than a PROM or NMOS chip as is typically used in an inkjet printhead circuit. Shown in FIG. 6 is a cross-sectional view of the layers in a typical EPROM chip 230. Disposed atop the semiconducting silicon substrate 232 is a gate oxide 236. Disposed atop the gate oxide layer is a layer of polysilicon material 238, in which the floating gate (14 in FIG. 5) is formed. When properly doped, this polysilicon material functions as a conductor. The gate oxide layer 236 functions as a dielectric layer (26 in FIG. 5) between the floating gate and the semiconductor substrate.

Disposed atop the floating gate layer is another layer 240 of gate oxide material, which provides another dielectric layer, atop which is another layer of

polysilicon 242, in which the control gate (12 in FIG. 5) is formed. Disposed atop the control gate layer are one or more metal layers 244, 248, separated by another dielectric layer 246. The metal layers provide row and column lines for the EPROM circuit, and also make the various electrical connections between the control gate, the drain, and other components of the circuit.

These circuit layers in a typical EPROM circuit are in contrast to the layers found in a typical inkjet printhead circuit. A cross-sectional view of the layers in an inkjet control chip 250, such as that providing the inkjet firing control circuit shown in FIG. 3, is given in FIG. 7. This chip includes a semiconductor substrate 252, atop which is an oxide layer 254 (such as silicon dioxide, SiO_2), followed by a polysilicon layer 256, a dielectric layer 258, then a Metal 1 layer 260 and Metal 2 layer 264, these metal layers being separated by a dielectric layer 262.

The two metal layers 260, 264 provide the conductors for the address lines, data lines, pre-charge, select, and fire lines, and other circuit connections. It will be apparent that this layer configuration lacks an additional polysilicon layer and gate dielectric that would be needed for creation of a standard EPROM cell. Prior attempts to implement EPROM's in this type of circuit have focused on adding additional process steps to add an extra floating gate and gate dielectric. Another option is to add a separate EPROM chip. Both of these options add complexity and cost

Advantageously, the inventor has developed a gate-coupled structure and method for providing EPROM functionality using the layers in this PROM chip, without adding process layers and cost. Shown in FIG. 8 is a schematic diagram of a gate-coupled EPROM bit 270 that can be created using the existing layers of the inkjet pen control chip shown in FIG. 7. The gate-coupled EPROM bit comprises two transistors having their floating gates tied together. The first transistor 272 is a control transistor, and the second transistor is the EPROM transistor 274. The control transistor includes two control connections or control terminals, the first terminal 276 being labeled Control1, and the second terminal 278 being labeled Control2.

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The floating gate 280 of the control transistor 272 is electrically coupled to the floating gate 282 of the EPROM transistor 274. The EPROM transistor includes a drain 284 and source 286, which can be connected to ground. The floating gate voltage is dependent upon the overlap capacitance of the source and drain of the control transistor 272, and whether the gate of the control transistor is on. The overlap and gate capacitance couple the voltage at Control1 and Control2 to the floating gate. The capacitance needs to be large enough to provide adequate coupling voltage to the floating gate. A standard EPROM uses the capacitance in the dielectric layer between the control gate and the floating gate to couple the voltage to the floating gate. In the gate-coupled device disclosed herein, the gate to drain overlap capacitance between Control1 276 couples the voltage at Control1 to the floating gate. The gate to source overlap capacitance at Control2 278 couples the voltage at Control2 to the floating gate. The goal is to find some capacitance structure to couple to the floating gate. In this configuration, the gate oxide layer (254 in FIG. 7) that provides the gate capacitance of a standard transistor is used in a reverse direction to provide this capacitance.

This gate-coupled structure is fully compatible with the printhead layer structure shown in FIG. 7, and only requires modification of the geometric layout of the various circuit layers. The floating gates 280, 282 of the control and EPROM transistors, as well as the coupling connection between them, can be fabricated in the polysilicon layer 256 of the printhead circuit. Further, these floating gate regions in the polysilicon layer can be electrically interconnected by the Metal1 layer 260. The gate/drain coupling is from the n+ drain region of the substrate 252 to the gate, through the gate oxide layer 254. The Metal1 layer 260 can be configured to connect the source of the control transistor 272 (Control2, 278) to the drain of the EPROM transistor 274 (Drain 284). One advantageous feature of this configuration is that there is both source and drain coupling to the floating gate. This provides additional capacitive coupling from the control node to the floating gate. In general, the more capacitive coupling the better.

Referring again to FIG. 8, the gates 276, 278 of the control transistor 272 can be tied together, or Control2 can be tied to the drain of the EPROM transistor 274. For some implementations, Control1, Control2 and Drain can be tied to separate voltages to get more efficient coupling. With Control2 278 and Drain 284 tied together, the voltage on Drain can limit the voltage on Control2, and the amount of voltage coupled to the floating gate 280.

In one embodiment, a space efficient layout can be obtained by tying the Drain 284 of the EPROM transistor 274 to the source (Control2) 278 of the control transistor 272. If a resistor is not needed to limit the drain current (e.g., limiting overheating by controlling pulse width instead, or relying on the resistance of the Select transistors (when implemented in arrays) to limit the current), Control1, Control2 and Drain can all be tied together. This configuration provides a high level of coupling in a small area, but also has higher sensitivity to excess drain current and overheating.

Alternatively, the drain 284 of the EPROM transistor 274 can be tied to the source (Control2) 278 of the control transistor 272, with a resistor 277 (shown in dashed lines in FIG. 8) between Control1 276 and Control2 278 to limit drain current. This configuration can be more robust with respect to drain current problems, though the voltage at the Control2-Drain node will be lower, and will provide less voltage to the floating gate.

Another approach is to hook the terminals 278 and 276 of the control transistor 272 together, with a resistor 283 (shown in dashed lines in FIG. 8) in series between them and the Drain 284 of the EPROM transistor 274. The resistor would limit current into the Drain, but the voltage at the nodes labeled Control1 and Control2 would still be at maximum voltage for greater voltage coupling to the floating gate.

Programming of this gate-coupled EPROM cell 270, like typical EPROM cells, is done by applying a voltage pulse to the terminals 276, 278 of the control transistor 272. This is done in order to provide a quantity of hot electrons to the floating gate 280. It is desirable that the voltage on the Drain 284 be close to the breakdown voltage of the circuit. The breakdown voltage is the voltage at which the EPROM transistor 274 begins to conduct with the gate below

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threshold voltage (gate at zero volts). In one embodiment, the inventor has programmed the EPROM circuit at a voltage of about 16 ±1 V where the circuit has a breakdown voltage of 15 Volts

As noted above, Control2 278 can be tied to the Drain 284 with a resistor 283 (having a resistance of, e.g., 100 ohm) in order to limit the breakdown voltage. Additionally, the physical size of the channel (gate) length – that is, the length of the channel under the gates of the EPROM transistor 274 – can be manipulated to modify the breakdown voltage. For example, a narrower gate length will lower the breakdown voltage. In one embodiment, the inventor has used a gate length of from 3.0μm to 3.5μm, instead of 4μm for this purpose.

The time required for programming is a function of the floating gate voltage, the quantity of hot electrons drawn to the floating gate, the threshold voltage change desired, the total gate structure capacitance, and the thickness of the gate oxide (layer 254 in FIG. 7). The gate oxide thickness determines the percentage of energetic hot electrons that are able to reach the floating gate 280. In one embodiment, the floating gate voltage is in the range of 5 volts to 12 volts, though other voltage ranges can be used. The floating gate voltage depends upon the voltage on the control terminals 276, 278 of the control transistor 272, and the coupling ratio of the silicon substrate and polysilicon layers (252, 256, respectively, in FIG. 7). While the desired hot electrons will be provided with any gate oxide thickness, the thickness of the gate oxide will sometimes be fixed for a given chip configuration. For example, in one embodiment of a printhead control chip, the thickness of the gate oxide is fixed at about 700 Å.

The quantity of hot electrons provided during programming is higher when programming is done at close to the breakdown voltage, and with higher current. In one embodiment, the inventor has programmed with a 25 mA current, though other currents can also be used. The inventor has also contemplated a 20 mA programming current, for example, and other currents can also be used. A range for the threshold voltage that the inventor has used is from 3 volts to 7 volts, but other threshold voltage ranges can also be used.

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Under the above parameters, the inventor has found that a 10 millisecond programming time can be used. However, different programming times can also be used, particularly if the various parameters mentioned above are varied. For example, the programming time can range from less than 100 μs to as much as several seconds (e.g. 4 seconds).

Reading of the EPROM cells is done by detecting the threshold voltage across the gate-coupled EPROM cell 270 using a cell sensor (not shown) elsewhere in the circuit. Detecting the threshold voltage can be done either by setting the gate/drain voltage and measuring the corresponding current, or by setting the current and measuring the voltage. The inventor has found that the on resistance (R_{on}) of the EPROM cell changes by a factor of about 2 before and after programming.

The inventor has built and tested this type of EPROM cell in a laboratory setting. In the test setup, a modified cell was built to monitor the floating gate voltage. A voltage pulse was applied to the gate and drain to program the EPROM cell to a desired threshold voltage. To test the cell to sense the gate voltage, the gate of a second sense transistor (not shown) was connected to the floating gate of the EPROM cell. This causes the gate voltage of the sense transistor to be the same as the floating gate voltage. The on resistance (R_{on}) of the second transistor is proportional to the gate voltage. By monitoring the on resistance of the second transistor, the floating gate voltage could be determined.

The gate-coupled EPROM cell shown in FIG. 8 can be incorporated into circuitry in which each EPROM identification cell is associated with a separate control circuit, like that of FIG. 4, or the gate-coupled identification bits can be incorporated into an array of identification cells that share control circuitry. Shown in FIG. 9 is one embodiment of a gate-coupled EPROM cell associated with individual control circuitry. This figure shows a portion of the circuitry of the identification cell of FIG. 4, with the gate-coupled EPROM cell 270 inserted in place of the identification bit (103 in FIG. 4). Such a configuration will provide one control line per cell, with the operation of each EPROM cell being controlled by an individual control transistor. This sort of configuration has a larger

physical size than the shared-circuitry arrangement, but is similar to some control schemes currently used with fuses.

As shown in FIG. 9, the identification line 102 is connected to the gates of the control transistor 272 and the drain of the EPROM transistor 274, and the source 286 of the EPROM transistor is coupled to the drain of the drive switch 106, which has its source coupled to ground 110. A narrower gate 282a can be provided on the EPROM transistor 274 to provide lower breakdown voltage. This allows the gate-coupled EPROM cell to obtain an adequate quantity of hot electrons at the EPROM transistor without exceeding the breakdown voltages of other transistors on the circuit. As discussed above with respect to FIG. 8, a resistor 283 (e.g. about 100 ohms) could be added between the drain 284 of the EPROM transistor 274 and the source 278 of the control transistor 272, or a resistor 277 can be placed between the source of the control transistor and the drain 276 of the control transistor. The method chosen would depend upon layout decisions and technique used to control drain current.

Referring back to FIG. 9, when the transistor 106 is turned on, the source of the EPROM transistor 274 is essentially at ground, and the EPROM cell functions as described for the cell in Fig 8. A voltage on the ID line 102 couples thru the gate oxide of the control transistor 272 to the floating gate (280/282 in FIG. 8). A high voltage (16V) will program the EPROM. A lower voltage will be used to read by detecting the threshold voltage or the on resistance. If the transistor 106 is off, any voltage applied to the ID line will not have a path to ground, and the EPROM cell will not be affected

Shown in FIG. 10 is a partial schematic diagram of an EPROM array 300 that can be produced using the gate-coupled EPROM cell disclosed herein. In this configuration an array of gate-coupled EPROM identification bits share control circuitry. In this array, a plurality of gate-coupled EPROM cells 270 are arranged in rows and columns. The input line of each gate-coupled EPROM cell is tied to the input voltage V_{In} (designated at 304) through input line 308. The source line 286 of each EPROM transistor 274 is tied to the drain of a row transistor 310. The row transistors are tied through their sources 312 to the drains of column transistors 314. If desired, a drain current limiting resistor (not

shown) can be added to the EPROM cell, as described above with respect to Fig 9. Rather than an individual resistor for each gate-coupled cell, a single resistor 322 (shown in dashed lines in FIG. 10) could be provided to feed all of the transistors in parallel. This resistor can be connected between the voltage Vin and the drain of the EPROM transistor (284 in FIG. 8), with a single line from Vin to the resistor, and separate lines 324 (shown in dashed lines in FIG. 10) extending from the resistor to the drains of each of the EPROM transistors in the array. The connection between the source and drain of the EPROM control transistor 272 would then be removed, and all of the control transistor-drain connections of the EPROM cell 270 would be tied directly to the input line 308.

The row lines, labeled 316a for Row 1, 316b for Row 2, etc., connect to the gates of all row select transistors 310 in a given row. The sources 312 of all row transistors in a given column are connected to the drain of the column transistor 314 for that column. The gates 318 of each column transistor are connected to a voltage source (not shown) through column lines (not shown). The sources 320 of the column transistors are connected to a common voltage, such as ground. The column transistors are labeled 314a for Column 1, 314b for Column 2, and so on.

The row transistors 310 and column transistors 314 allow selection of the specific gate-coupled EPROM cells, both for programming and reading. The column transistors are normal transistors, and the interconnects to these transistors can be fabricated in the Metal 1 layer (260 in FIG. 7). Some advantages of this circuit are that it is more compact than implementation of identification cells with separate control circuitry, and it doesn't require the Metal2 layer and its associated layout rules. Additionally, the size of the gate-coupled EPROM array 300 is not limited by the configuration of the printhead firing cell control circuitry (80 in FIG. 3). This array can be as large or as small as desired, regardless of the number of data lines associated with the firing cell control circuit.

To program a cell 270 of the array 300, the cell is selected by applying a voltage to one row line (e.g. 316a) and one column line (e.g. to the gate of

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column transistor 314a), and then a pulse of relatively high voltage V_{in} (e.g. 16V) is applied. To sense the condition of the cell, a lower input voltage V_{in} pulse (e.g. 5V) is applied in the same way, and the current is monitored. In this array, there is no high voltage across the drain to the source of the EPROM transistor except when programming. Advantageously, there are no drain to gate voltage coupling issues because the drain and gate of the EPROM transistors switch together. In addition, gate to drain coupling is actually advantageous because it increases the voltage coupling to the gate.

The inventor has found that the size of the row select transistors 316 is significant because they must handle the programming current, such as 20 mA, 25 mA, or higher. For this purpose, the inventor has used row select transistors having a width of 150 μm. It will be apparent that smaller sizes can be used for lower programming current, and larger sizes will be needed for higher current.

In operation, a row signal turns on all row control transistors 316 in that row. A column signal turns on a selected column control transistor 314. An input voltage V_{in} is then applied, and only the cell 270 with both its row and column transistor turned on will have the full voltage across it. All other cells will have the source of the EPROM transistor floating. That is, the source of the EPROM transistor will not be driven to any fixed voltage, but will just float to the voltages on the other terminals. There will be no voltage across the EPROM transistor.

An EPROM array can be configured in the manner described above for use in providing pen ID bits in an inkjet printhead. In this configuration, the row and column signals can be supplied by the shift register of the pen control circuit. That is, rather than drive the row and column lines individually, the respective values can be shifted into a shift register, and driven from the shift register outputs. The shift register addresses the row and column selects of the 2x10 array. It will be apparent to those skilled in the art of semiconductor design that the geometric configuration of the circuitry can be configured in a variety of ways.

The inventor has built and programmed a 4-bit array based on the above design. After programming, the EPROM cells have held their charge for over a year.

The reliability and longevity of the gate-coupled EPROM cell described herein depends upon a number of factors. Because the structure is different than the typical EPROM cell configuration, some aspects of the resultant design affect its robustness. For example, the larger size of the floating gate (280 in FIG. 8) can allow more area for leakage current. Additionally, the gate oxide (254 in FIG. 7) is not processed for absolute minimum leakage current.

Additionally, the flatness of the layers can affect their performance. Slight undulations in layer surfaces and variations in the thickness of the different layers can cause charge concentrations and leakage between the layers. In a pen control circuit configured with the layers of the PROM chip shown in FIG. 7, for example, the thickness and flatness of the polysilicon layer 256 and adjacent dielectric layer 254 are not as critical for operation of the PROM circuit. This factor affects the level of quality control applied to formation of these layers. However, in an EPROM circuit, these factors have a greater effect.

At the same time, there are other factors that affect fuses that do not affect EPROMS, or that do not affect them in the same way or to the same extent. As noted above, fuses have a number of drawbacks that are frequently bothersome. It is believed that EPROMs will ultimately be more reliable than fuses in the application disclosed herein. Where the possible limitations of the gate-coupled EPROM cell disclosed herein can be tolerated, this configuration can be useful without the need to increase quality control. This is true of inkjet pens. The design life for an inkjet pen is usually about 18 months, primarily because inkjet cartridges are usually sold soon after manufacture, and because the pen then gets used up. Consequently, if the EPROM cells can reliably hold their charge for that time period, there is little likelihood that the device will not work as intended. However, this same structure can be effectively used in other applications where greater reliability is desired by exerting greater control over the flatness and thickness of the layers.

The gate-coupled EPROM structure disclosed herein can replace fuses in inkjet pen control circuits without adding process layers and cost. This configuration provides cells that are larger than traditional EPROM cells, but smaller than fuses.

The gate-coupled identification cells can be used to store a wide variety of identification information indicating features of or other information about the printhead die. For example, a printer employing a printhead having EPROM identification cells can use the identification information for a wide variety of purposes to optimize printing quality or perform other functions. For example, selected identification cells can store identification information about the printhead die, or about the inkjet cartridge or pen in which the printhead die is inserted, such as information indicating an out of ink detection level.

The identification cells can also store identification information indicating a thermal sense resistance (TSR) value to determine the temperature of the printhead. Selected identification cells can store identification information indicating a printhead uniqueness number to identify and properly respond to the printhead. Identification cells can be used to store identification information indicating an ink drop weight for a printhead. A printer can account for the drop weight values stored in selected identification cells and the out of ink detection level information stored in other selected identification cells to determine actual out of ink detection levels.

The printer can also use identification information for marketing purposes, such as regional marketing and original equipment manufacturer (OEM) marketing. For example, selected identification cells store identification information indicating a marketing region for the fluid ejection device. In one embodiment, selected identification cells can store identification information indicating the seller of an OEM fluid ejection device. Selected identification cells can also store identification indicating whether an OEM printer is unlocked. For example, the OEM printer can respond to the OEM unlocked information to unlock an OEM printer, such that the OEM printer can accept OEM printheads sold by a given company or group of companies and printheads sold by

companies other than the given company or group of companies, such as the actual original manufacturer company.

Selected identification cells store identification information indicating the product type and product revision of a fluid ejection device. The product type and product revision can be used by a printer to ascertain physical characteristics about a printhead. Product revision physical characteristics, such as spacing between nozzle columns, that may change in future products can also be stored in selected identification cells of a printhead. In this embodiment, the product revision physical characteristic information can be used by the printer to adjust for the physical characteristic changes between product revisions.

Gate-coupled EPROM cells configured this way can also be used for many other purposes in addition to those noted above. Because the charge on the floating gate of the EPROM transistor (282 in FIG. 8) is cumulative, this configuration can be used to store cumulative quantities. For example, in an inkjet printhead, the gate-coupled EPROM cells can be successively reprogrammed to track the number of pages printed out, or for other purposes. Since programming of EPROM cells modifes the threshold voltage of the EPROM cell 270, successive programming of these cells can be used to control analog circuits, such as to create a variable time delay. Other applications are also possible.

It is to be understood that the above-referenced arrangements are illustrative of the application of the principles of the present invention. It will be apparent to those of ordinary skill in the art that numerous modifications can be made without departing from the principles and concepts of the invention as set forth in the claims.

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CLAIMS

What is claimed is:

1. An EPROM cell in a printhead control circuit for an inkjet printer, the control circuit having a semiconductor substrate, one and only one polysilicon layer disposed above the semiconductor substrate, and a conductive layer disposed above the polysilicon layer, the EPROM cell comprising:

a control transistor, having a floating gate comprising a portion of the polysilicon layer;

an EPROM transistor, having a floating gate comprising a portion of the polysilicon layer; and

an electrical interconnection, comprising a portion of the conductive layer, interconnecting the floating gate of the control transistor and the floating gate of the EPROM transistor.

2. An EPROM cell in accordance with claim 1, wherein the control transistor comprises a first control terminal and a second control terminal, and further comprising an electrical interconnection between the first and second control terminals.

3. An EPROM cell in accordance with claim 2, wherein the electrical interconnection between the first and second control terminals comprises a resistance.

4. An EPROM cell in accordance with claim 1, wherein the control transistor comprises a first control terminal and a second control terminal, and the EPROM transistor comprises a drain, and further comprising an electrical interconnection between the second control terminal of the control transistor and the drain of the EPROM transistor.

5. An EPROM cell in accordance with claim 4, wherein the electrical interconnection between the second control terminal of the control transistor and the drain of the EPROM transistor comprises a resistance.

6. An EPROM cell in accordance with claim 1, wherein the control transistor comprises a first control terminal and a second control terminal, and the EPROM transistor comprises a drain, and further comprising an electrical interconnection between the first and second control terminals of the control transistor and the drain of the EPROM transistor.

7. An EPROM cell in accordance with claim 6, wherein the electrical interconnection between the first and second control terminals of the control transistor and the drain of the EPROM transistor includes a resistance

8. An EPROM cell in accordance with claim 1, wherein a programming charge applied to the floating gate of the EPROM transistor is cumulative, such that the EPROM cell can be successively charged to store cumulative values.

9. An EPROM cell in accordance with claim 1, wherein the control transistor includes a drain connection, and the EPROM transistor includes a source connection, and further comprising an input line, connected to the drain connection of the control transistor, whereby programming signals can be provided to the EPROM transistor.

10. An EPROM cell in accordance with claim 9, further comprising a drive transistor, having a drain connected to the source of the EPROM transistor, a gate of the drive transistor being associated with a precharge line, a select line, and a data line of an array of firing cells, whereby programming and reading of the EPROM cell can be controlled by signals sent through the input line and through the precharge line, the select line, and the data line.

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GATE-COUPLED EPROM CELL FOR PRINTHEAD

ABSTRACT OF THE DISCLOSURE

An EPROM cell (270) in a printhead control circuit for an inkjet printer, having exactly one polysilicon layer (256) and a conductive layer (260) disposed above the polysilicon layer, includes a control transistor (272) and an EPROM transistor (274). The control and EPROM transistors each have floating gates (280, 282) comprising a portion of the polysilicon layer (256), and an electrical interconnection, comprising a portion of the conductive layer (260), interconnects the floating gate (280) of the control transistor (272) and the floating gate (282) of the EPROM transistor (274).

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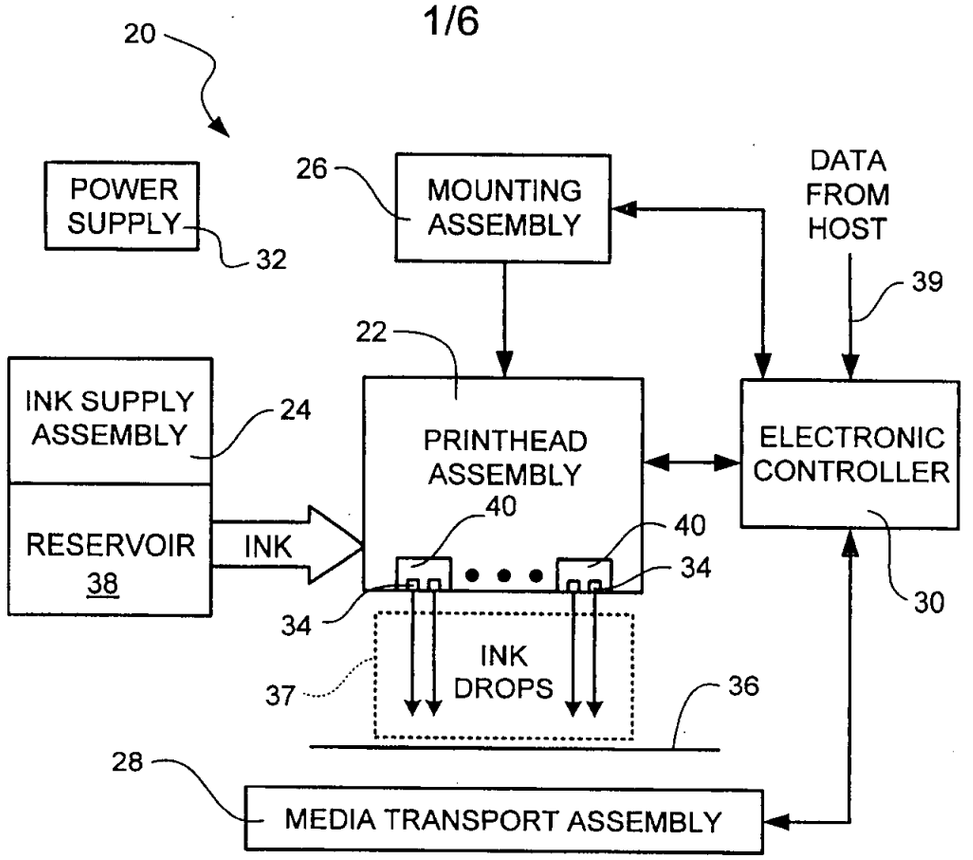


FIG. 1

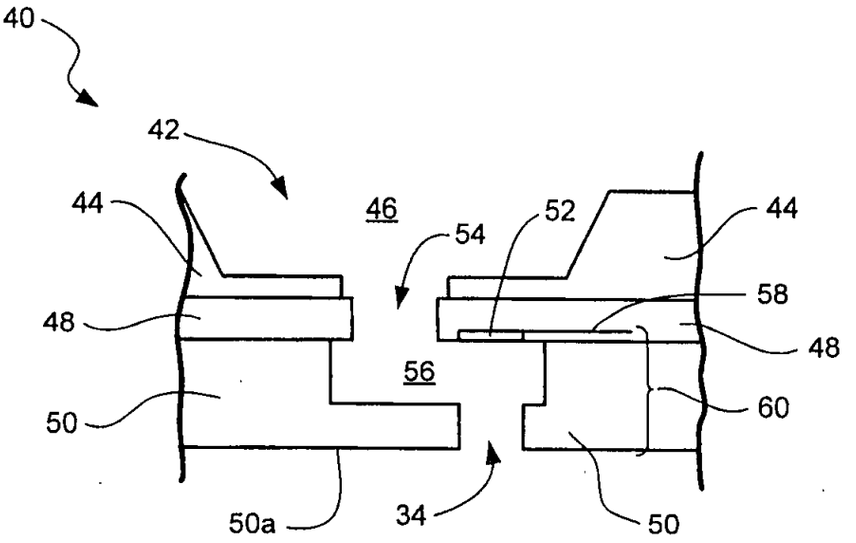
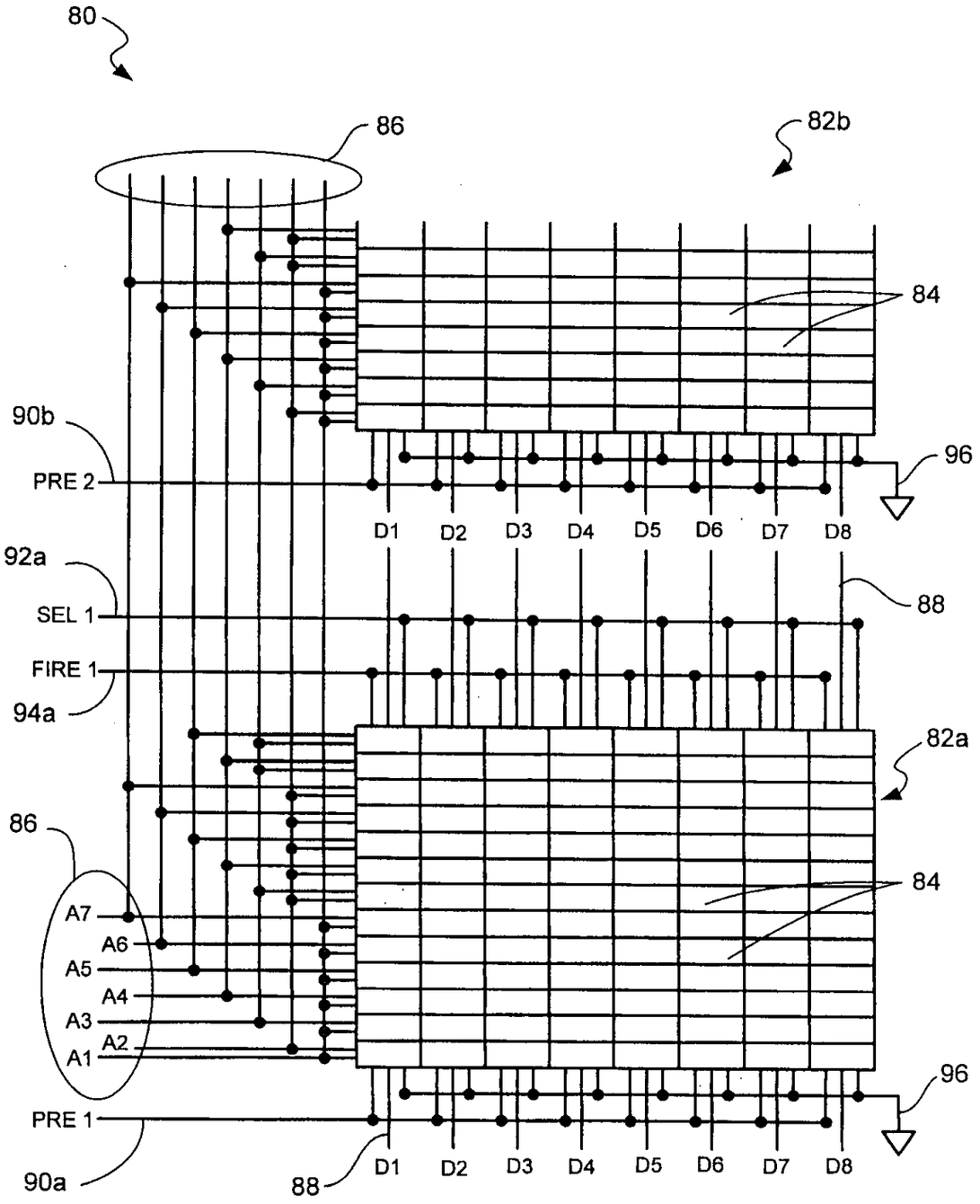


FIG. 2


80
86
82b
84
90b
PRE 2
96
D1
D2
D3
D4
D5
D6
D7
D8
92a
SEL 1
88
FIRE 1
94a
82a
86
84
A7
A6
A5
A4
A3
A2
A1
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PRE 1
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88
D1
D2
D3
D4
D5
D6
D7
D8

FIG. 3

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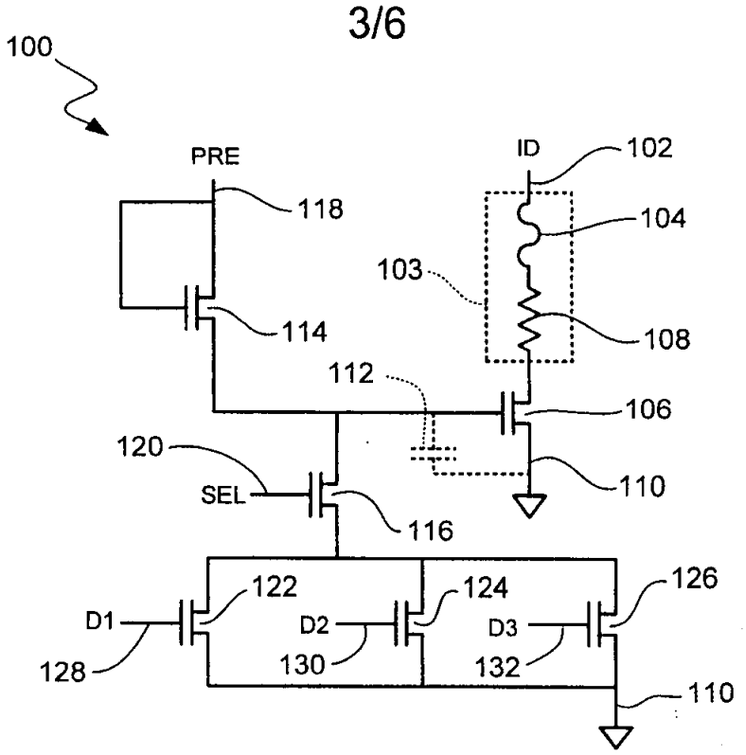

FIG. 4

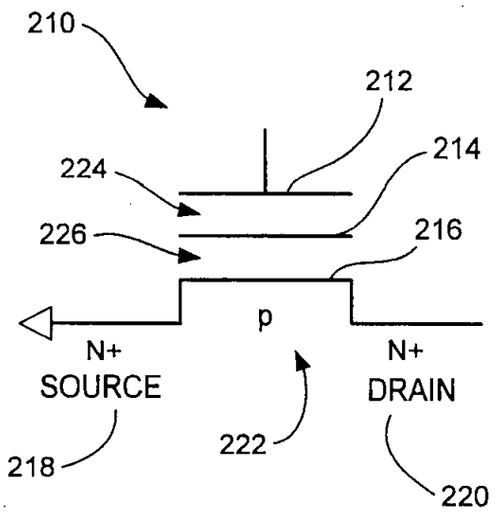

FIG. 5

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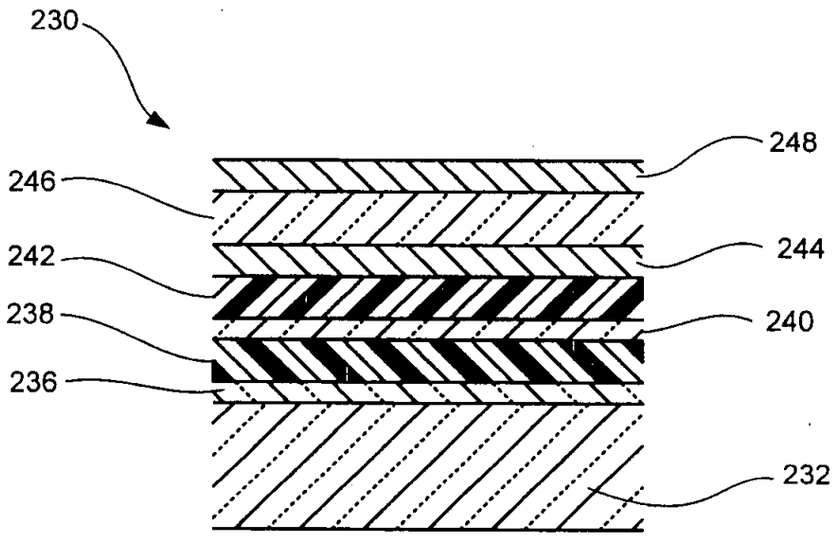

FIG. 6

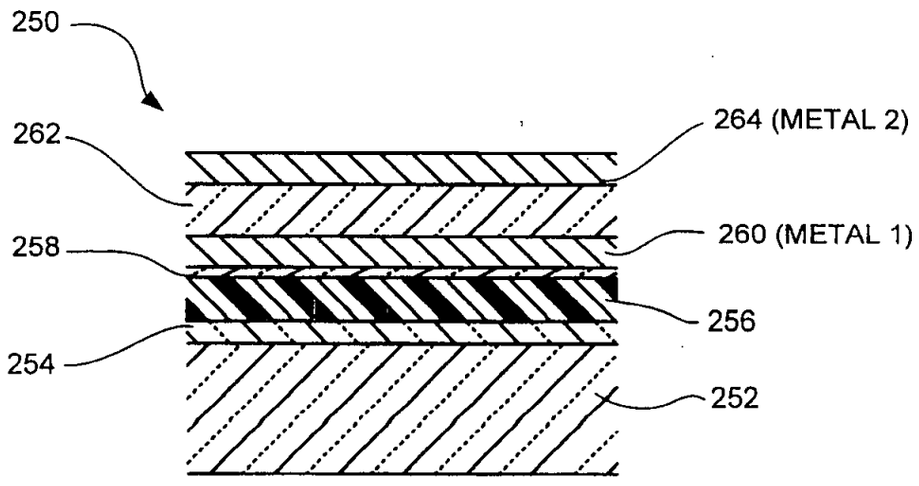

FIG. 7

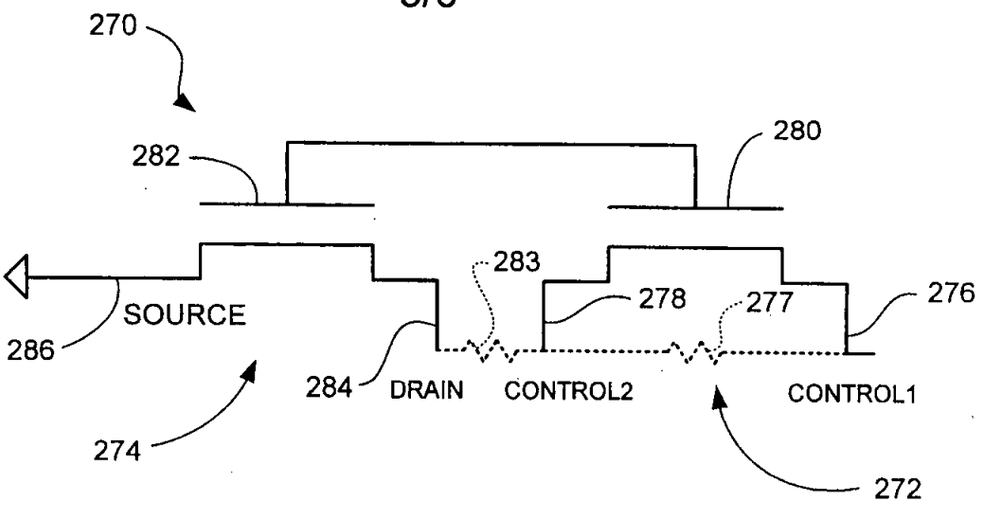
270
282
280
283
278
277
276
SOURCE
286
284
DRAIN
CONTROL2
CONTROL1
274
272

FIG. 8

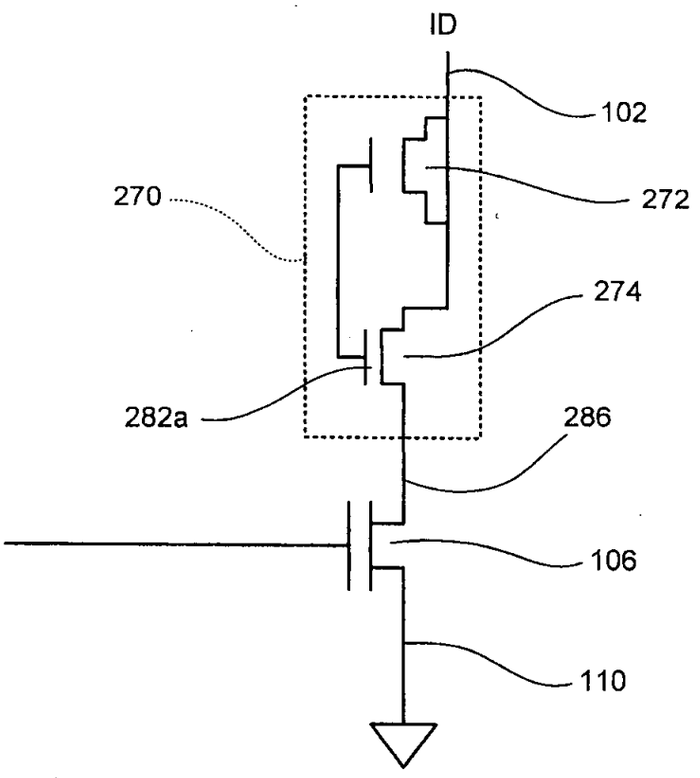
ID
102
270
272
274
282a
286
106
110

FIG. 9

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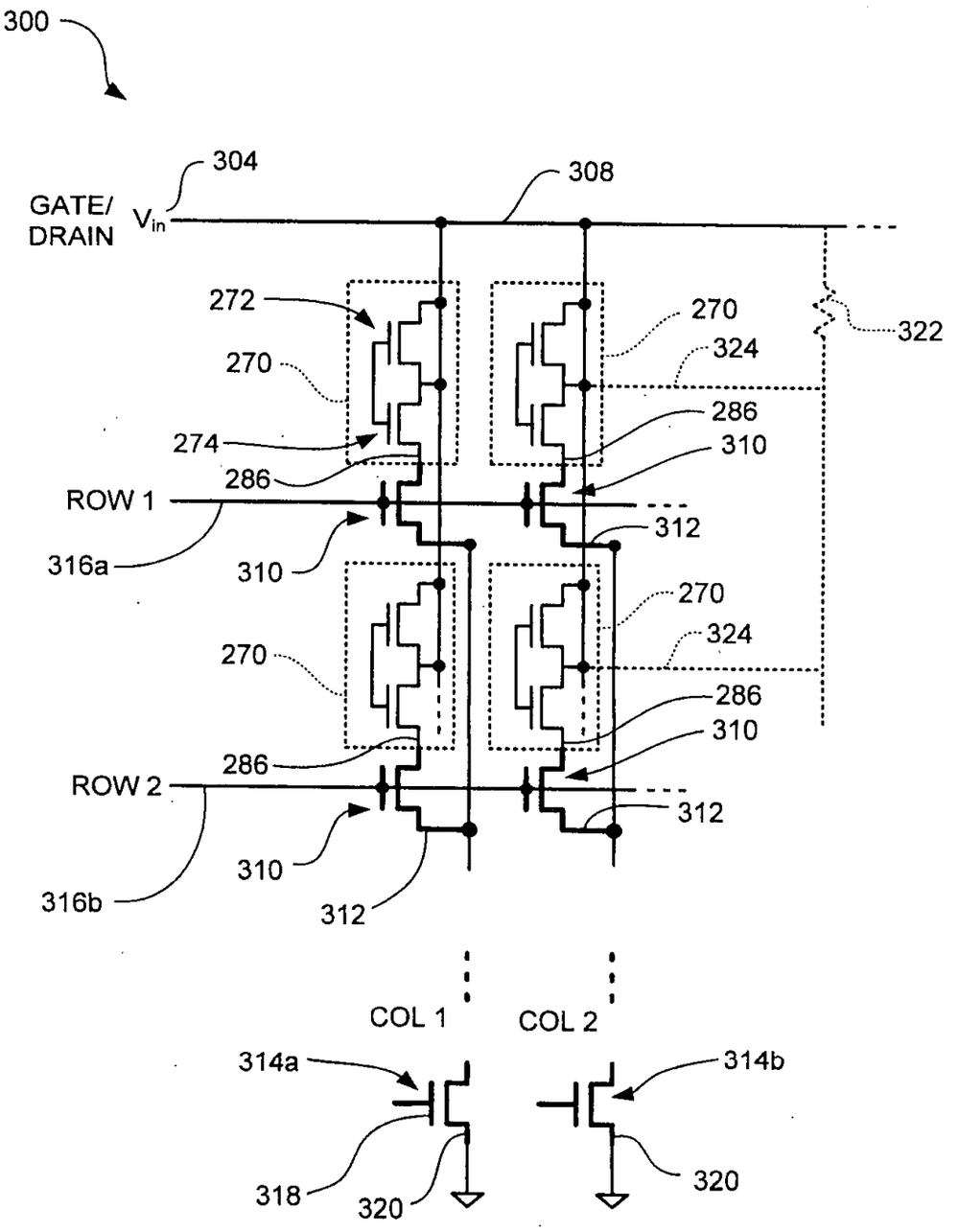
300
304
308
GATE/
DRAIN
V_{in}
272
270
274
286
310
322
324
ROW 1
316a
312
ROW 2
316b
COL 1
COL 2
314a
314b
318
320

FIG. 10

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PATENT APPLICATION

ATTORNEY DOCKET NO. 200600453-1

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GATE-COUPLED EPROM CELL FOR PRINTHEAD

Filing date: _____ Application No.: _____

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Trudy Benjamin Date Assignment Signed: 2/23/2006
Inventor's Signature (Seal)

Inventor's Typed Name: Trudy Benjamin Date Application Signed: 2/23/2006

State of Washington)
) ss.:
County of)

Before me this ____ day of _____, personally appeared Trudy Benjamin who is personally known or proved to me on the basis of satisfactory evidence to be the person who acknowledged the foregoing instrument of assignment to be his/her free act and deed.

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Notary Public
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ATTORNEY DOCKET NO. 200600453-1

150

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GATE-COUPLED EPROM CELL FOR PRINTHEAD

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			YES: ___ NO: ___
			YES: ___ NO: ___

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APPLICATION NUMBER	FILING DATE

U. S. Priority Claim

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APPLICATION NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

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Direct Telephone Calls to:

James McDaniel

(858) 655-4157

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Full Name of Inventor: Trudy Benjamin Citizenship: US

Residence: Portland, Oregon

Post Office Address: 18110 SE 34th St., Vancouver, WA 98683-8906

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
11/360,801	02/23/2006	2811	1000	200600453-1	6	20	3

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FILING RECEIPT

OC000000018352207

Date Mailed: 03/23/2006

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Power of Attorney: The patent practitioners associated with Customer Number **022879**.

Domestic Priority data as claimed by applicant

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US11/360,801

Projected Publication Date: 08/23/2007

Non-Publication Request: No

Early Publication Request: No

Title

Gate-coupled EPROM cell for printhead

Preliminary Class

257

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NUMBER OF PAGES: 2

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DOCKET NUMBER: 200600453-1

ASSIGNOR:
BENJAMIN, TRUDY

DOC DATE: 02/23/2006

ASSIGNEE:
HEWLETT-PACKARD DEVELOPMENT
COMPANY, L.P.
20555 SH 249
HOUSTON, TEXAS 77070

SERIAL NUMBER: 11360801
PATENT NUMBER:
TITLE: GATE-COUPLED EPROM CELL FOR PRINTHEAD

FILING DATE: 02/23/2006
ISSUE DATE:

JEFFREY OLSEN, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

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113261 U.S.PTO
11/360801
022306

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Rev 12/04 (Redesgn)

US007365387B2

(12) **United States Patent**
Benjamin

(10) **Patent No.: US 7,365,387 B2**
(45) **Date of Patent: Apr. 29, 2008**

(54) **GATE-COUPLED EPROM CELL FOR PRINTHEAD**

(75) Inventor: **Trudy Benjamin**, Portland, OR (US)

(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/360,801**

(22) Filed: **Feb. 23, 2006**

(65) **Prior Publication Data**

US 2007/0194371 A1 Aug. 23, 2007

(51) **Int. Cl.**
H01L 29/788 (2006.01)

(52) **U.S. Cl.** **257/320**; 257/317; 438/252; 438/211; 438/201; 327/143; 327/347

(58) **Field of Classification Search** 257/317, 257/320; 438/266, 201, 211, 252; 327/112, 327/143; 347/14, 57; 365/114
See application file for complete search history.

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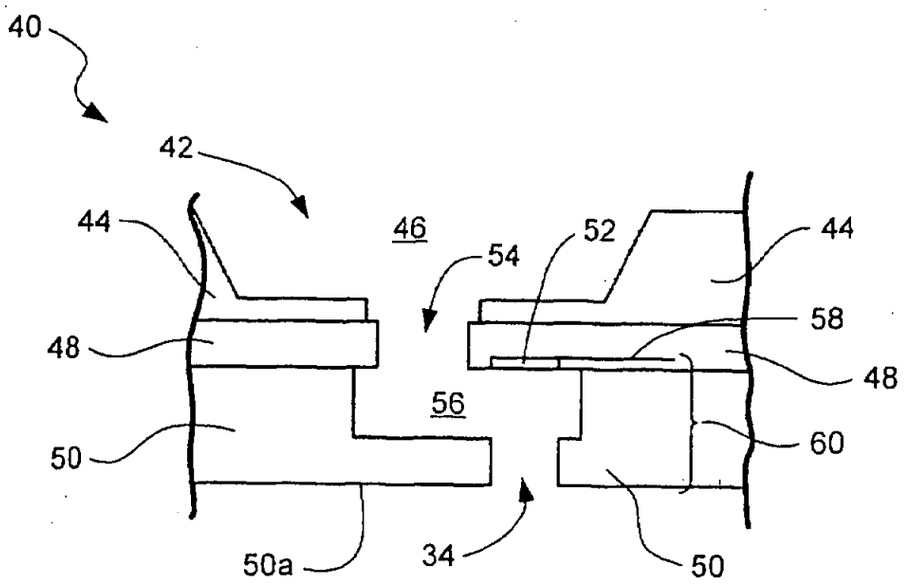
(Continued)

Primary Examiner—Jerome Jackson
Assistant Examiner—Jami M Valentine

(57) **ABSTRACT**

An EPROM cell in a printhead control circuit for an inkjet printer, having exactly one polysilicon layer and a conductive layer disposed above the polysilicon layer, includes a control transistor and an EPROM transistor. The control and EPROM transistors each have floating gates comprising a portion of the polysilicon layer, and an electrical interconnection, comprising a portion of the conductive layer, interconnects the floating gate of the control transistor and the floating gate of the EPROM transistor.

20 Claims, 6 Drawing Sheets



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U.S.P.T.O. Office Action for U.S. Appl. No. 11/263,337, mailed Aug. 9, 2007 (5pp).
Claims as currently presented in U.S. Appl. No. 11/263,337 (4pp).

* cited by examiner

AS: 102-96

159

Brigard & Castro
BOGOTA - COLOMBIA

PODER

Yo (nosotros) **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**

domiciliado(s) en Hewlett-Packard Company, Intellectual Property Administration, 20555 S.H. 249, Houston, TX 77070, Estados Unidos de América

Nombro(amos) a: **JUAN PABLO CADENA SARMIENTO** y/o **CARLOS H. PALACIO EASTMAN** y/o **MARTIN E. TORRES CARDOZO**, de Bogotá, Colombia, apoderados verdaderos y legales con poder especial, amplio y suficiente, para recabar de las oficinas y autoridades colombianas administrativas, judiciales y de policía, en cualquier instancia o recurso, la obtención de patentes de invención, diseños industriales, modelos de utilidad y contratos sobre los mismos, obtención de certificados de obtentor de variedades vegetales, así como sus prórrogas, renovaciones, anotaciones de traspaso, cambios de nombre y/o domicilio y/o dirección; intervenir como demandante o como demandado en cualquier instancia y recurso ante cualquier juez, corporación, funcionario público o autoridad en acciones judiciales, administrativas y de policía tales como: oposiciones, acciones de caducidad, cancelación y nulidad; acciones reivindicatorias, acciones de competencia desleal; demandas penales; acciones de indemnización de perjuicios, reclamos y observaciones a solicitudes de patentes, diseños industriales, modelos de utilidad, en el ejercicio de medidas cautelares y en otras acciones o medidas similares.

A este efecto, lo(s) faculto(amos) para elevar solicitudes, formular descripciones, enmiendas, protestas, declaraciones, oposiciones, cancelaciones, nulidades, apelaciones y reclamos; pagar impuestos, cuotas y gravámenes prescritos por la ley; renunciar o desistir a derechos concedidos o en curso de concesión; recibir toda clase de documentos y valores, dando el descargo respectivo, y, en general, para dar ante dichas autoridades todos los pasos necesarios al efecto indicado y tomar todas las medidas que creyeren conducentes al resguardo de mis (nuestros intereses), con todas las demás facultades legales necesarias.

Este poder comprende la facultad de ratificar o confirmar en mi (nuestro) nombre lo actuado así como la facultad de desistir, transigir, comprometer, y la de sustituirlo en todo o en parte y revocar sustituciones. Asimismo nombro(amos) a: **JUAN PABLO CADENA SARMIENTO** y/o **CARLOS H. PALACIO EASTMAN** y/o **MARTIN E. TORRES CARDOZO**, domiciliado(s) en la Carrera 7 No. 71-21, Torre B, Piso 4, mis (nuestros) apoderados en Colombia, con facultades para recibir notificaciones y designar apoderados judiciales o extrajudiciales.

Otorgado y firmado en

hoy de de 200_

Firma

Nombre
Cargo

POWER OF ATTORNEY

I (We) **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**

domiciled in Hewlett-Packard Company, Intellectual Property Administration, 20555 S.H. 249, Houston, TX 77070, United States of America

Hereby appoints **JUAN PABLO CADENA SARMIENTO** and/or **CARLOS H. PALACIO EASTMAN** and/or **MARTIN E. TORRES CARDOZO**, of Bogotá, Colombia, my (our) true and lawful attorneys with special, ample and sufficient power to obtain from the Colombian administrative, judicial and police offices and authorities, in any instance, privileges of patents of invention, industrial designs and utility models; and contracts related thereto, as well as extensions, renewals and recordal of assignments and changes of name, domicile and address related to the above; to act as plaintiff or defendant in any instance or recourse, and before any judge, corporation, public official or authority in judicial, administrative and police actions, such as: oppositions, caducity, cancellation and nullity actions; criminal proceedings, actions for payment of damages: claims or observations on patent applications, models, industrial designs and utility models; in the exercise of preventive measures and in other actions or similar proceedings.

To that effect they hereby empowered to file applications, formulate descriptions, amendments, protests, declarations, oppositions, cancellations, nullities, appeals and claims; to pay taxes, quotas and assessments prescribed by law, renounce or waive the rights granted or in the process of granting; to receive all kinds of documents and valuables, giving the respective release of receipt, and, in general, to take before said authorities the necessary steps to such effect, and any measures that they may deem pertinent to the safeguard of my (our) interest(s) with all the other necessary legal powers.

This power includes the faculty to ratify or confirm desist, settle and compromise on my (our) behalf, and to substitute this power in whole or in part and to revoke substitutions. At the same time I (We) hereby appoint **JUAN PABLO CADENA SARMIENTO** and/or **CARLOS H. PALACIO EASTMAN** and/or **MARTIN E. TORRES CARDOZO**, domiciled in Carrera 7 No. 71-21, Torre B, Piso 4, my (our) attorney(s) in fact, with powers to receive notifications and to designate judicial and extrajudicial attorneys.

Granted and signed in

This 1st day of March 2007

Name: Guy J. Kelley
Title: Assistant General Counsel

COMO NOTARIO CUARENTA Y SEIS ENCARGADO DEL CIRCULO DE BOGOTA, HAGO CONSTAR QUE ESTA COPIA FOTOSTATICA CONCUERDE CON EL ORIGINAL QUE HE TENIDO A LA VISTA
BOGOTA D.C. REPUBLICA DE COLOMBIA
6 MAR. 2007
ROSA FALLA LANSECA
NOTARIO CUARENTA Y SEIS ENCARGADO

160

APOSTILLE
(Convention de La Haye du 5 October 1961)

1. Country: United States of America
   This public document
2. has been signed by MICHAEL KRAFT
3. acting in the capacity of Notary Public, State of Colorado
4. bears the seal/stamp of the MICHAEL KRAFT, Notary Public, State of Colorado

CERTIFIED

5. at Denver, Colorado 6. this 7th day of March, 2007
7. By MIKE COFFMAN, Secretary of State, State of Colorado
8. Certificate Number 132656.
9. (OFFICIAL SEAL) 10. Signature:

Mike Coffman

COMO NOTARIO CUARENTA Y SEIS ENCARGADO DEL CIRCULO DE BOGOTA, HAGO CONSTAR QUE ESTA COPIA FOTOSTATICA COINCIDE CON EL ORIGINAL QUE HE TENIDO A LA VISTA
BOGOTA D.C. REPUBLICA DE COLOMBIA
16 MAR. 2007
ROSA FALLA LAISECA
NOTARIO CUARENTA Y SEIS ENCARGADO

Acknowledgement of Power of Attorney

State of Colorado
County of Larimer

The foregoing instrument was acknowledged before me this 1st day of March, 2007 by Guy J. Kelley, Assistant General Counsel of Hewlett Packard Development Company, L.P. a Houston, Texas corporation, on behalf of the corporation.

MICHAEL KRAFT NOTARY PUBLIC STATE OF COLORADO

Michael Kraft
My commission expires: Dec 15, 2007

COMO NOTARIO CUARENTA Y SEIS ENCARGADO DEL CIRCULO DE BOGOTA, HAGO CONSTAR QUE ESTA COPIA FOTOSTATICA COINCIDE CON EL ORIGINAL QUE HE TENIDO A LA VISTA BOGOTA D.C. REPUBLICA DE COLOMBIA
16 MAR. 2007
ROSA FALLA LAISECA
NOTARIO CUARENTA Y SEIS ENCARGADO

162

TRADUCCION AL ESPAÑOL del Documento de Poder otorgado por **Hewlett-Packard Development Company, L.P.** con domicilio en Hewlett-Packard Company, Intellectual Property Administration, 20555 S.H. 249, Houston, TX 77070, Estados Unidos de América.

ESTADO DE COLORADO
1876

APOSTILLA
(Convención de La Haya del 5 de Octubre de 1961)

1. PAÍS: **ESTADOS UNIDOS DE AMERICA**

   ESTE DOCUMENTO PÚBLICO

2. HA SIDO FIRMADO POR **MICHAEL KRAFT**

3. ACTUANDO EN CAPACIDAD DE **NOTARIO PUBLICO, ESTADO DE COLORADO**

4. LLEVA EL SELLO/TIMBRE DE **MICHAEL KRAFT, NOTARIO PUBLICO, ESTADO DE COLORADO**

CERTIFICADO

5. EN DENVER, COLORADO 6. EL 7 DE MARZO DE 2007

7. POR MIKE COFFMAN, SECRETARIO DE ESTADO, ESTADO DE COLORADO

8. CERTIFICADO NO. 132656.

9. SELLO OFICIAL 10. FIRMA

(FIRMA)

COMO NOTARIO CUARENTA Y SEIS ENCARGADO DEL CIRCULO DE BOGOTA, HAGO CONSTAR QUE ESTA COPIA FOTOSTATICA COINCIDE CON ORIGINAL QUE HE TENIDO A LA VISTA
D.C. REPUBLICA DE COLOMBIA
16 MAR. 2007
ROSA FALLA LAISECA
NOTARIO CUARENTA Y SEIS ENCARGADO

163

Reconocimiento de Poder de Abogado

Estado de Colorado
Condado de Larimer

El instrumento saliente fue reconocido ante mi este 1er día de Marzo, 2007 por Guy J. Kelley,.Consejero General Asistente de Hewlett-Packard Development Company, L.P., una corporación de Houston, Texas, en representación de la corporación.

Hay un sello que dice:

MICHAEL KRAFT
NOTARIO PUBLICO
ESTADO DE COLORADO

_____(firma)_____
Michael Kraft
Mi comisión vence: Dic. 15, 2007

COMO NOTARIO CUARENTA Y SEIS ENCARGADO DEL CIRCULO DE BOGOTA, HAGO CONSTAR QUE ESTA COPIA FOTOSTATICA COINCIDE CON EL ORIGINAL QUE HE TENIDO A LA VISTA
D.C. REPUBLICA DE COLOMBIA
16 MAR. 2007
ROSA FALLA LAISECA
NOTARIO CUARENTA Y SEIS ENCARGADO

164

REPUBLICA DE COLOMBIA
SUPERINTENDENCIA DE INDUSTRIA Y COMERCIO

Bogotá,
2020

Doctor(a)
CADENA SARMIENTO JUAN PABLO

REFERENCIA	Radicación No.	8 87789
	Solicitud internacional	PCT/US2007/062644
	Fecha inicio fase nacional	23/09/2008
	Trámite	11
	Evento	378
	Actuación	430
	Oficio No.	0539

Como resultado del examen de forma, realizado con fundamento en el artículo 38 de la Decisión 486 de la Comisión de la Comunidad Andina, artículo 27 del Tratado de Cooperación en Materia de Patentes (PCT), regla 51 bis del Reglamento y Circular Única de la Superintendencia de Industria y Comercio, se le comunica que:

1. En la documentación allegada no se evidencia la existencia y representación de la sociedad solicitante, por lo tanto debe allegar el documento que así lo acredite.

En cumplimiento de lo dispuesto por el artículo 39 de la Decisión 486, se le requiere para que dentro del término de dos meses siguientes a la fecha de notificación del presente oficio, complete los requisitos anteriormente enunciados. En caso de no dar cumplimiento al presente requerimiento, la solicitud se considerará abandonada y perderá su prelación.

Notifíquese el presente oficio conforme a lo dispuesto en el numeral 5.2, literal e), del capítulo quinto del título primero de la Circular Unica No.10 de 2001.

ALIX CARMENZA CESPEDES DE VERGEL
Jefe de la división de Nuevas Creaciones

El anterior requerimiento fue notificado por fijación en lista de fecha 23 ENE. 2009
jfernand

BRIGARD& CASTRO
PROPIEDAD INTELECTUAL

CARRERA 7 # 71 – 21 TORRE B – PISO 4
BOGOTÁ – COLOMBIA
TEL: (571) 744 22 00
FAX: (571) 742 22 00 – 321 40 45
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165

AS: 108.191

Señora Jefe
DIVISION DE NUEVAS CREACIONES
SUPERINTENDENCIA DE INDUSTRIA Y COMERCIO
E. S. D.

RESPUESTA A OFICIO 0539 DE 23 ENERO 2009

REF: Expediente No. 08 087789 – Solicitud de Patente Entrada en Fase Nacional Corresp. a la Solicitud Internacional PCT/US2007/062644
a favor de **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**
Titulada: CELDA EPROM ACOPLADA A COMPUERTA PARA CABEZAL DE IMPRESIÓN

JUAN PABLO CADENA SARMIENTO, vecino de Bogotá, portador de la tarjeta profesional No. 57492, obrando como apoderado de la sociedad **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**, según lo acredita el documento de poder presentado en esa División, para dar cumplimiento al requerimiento notificado por fijación en lista el 23 de enero de 2009, de acuerdo con los Artículos 38 y 39 de la Decisión 486 de la Comisión de la Comunidad Andina, Artículo 27 del Tratado de Cooperación en Materia de Patentes (PCT), regla 51 bis del Reglamento y Circular Única de la SIC, me permito allegar los siguientes documentos:

1. Fotocopia autenticada del certificado que acredita la Existencia y Representación Legal de **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**, debidamente apostillado y traducido al castellano.

2. Cesión del derecho a la Patente otorgado por el inventor al solicitante, debidamente apostillado para su mejor referencia, dado que las declaraciones que acreditan la cesión fueron presentadas con nuestro memorial petitorio del 22 de agosto de 2008.

3. Extracto para publicación y Tarjeta de Archivo Temático.

De la señora Jefe atentamente,

JUAN PABLO CADENA SARMIENTO
C.C. No. 80.410.337 de Usaquén
Cra. 7 No.71-21, Torre B, Piso 4

Bogotá, 18 de marzo de 2009
MXB/aac

[redacted]

166

SUPERINTENDENCIA DE INDUSTRIA Y COMERCIO

Industria y Comercio
SUPERINTENDENCIA

DIVISION DE NUEVAS CREACIONES

TARJETA ARCHIVO TEMÁTICO

PATENTE DE INVENCION _X_ PCT _X_ MODELO DE UTILIDAD ____ DISEÑO INDUSTRIAL ____

(21) N° de solicitud: 08 087789 (22) Fecha de solicitud: 22-08-2008

(51) Clasificación Internacional:

(71) Solicitante(s) **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**

(72) Inventor(es) Trudy L. BENJAMIN

(74) Agente: JUAN PABLO CADENA SARMIENTO

(30) Prioridad	(31) No. Prioridad	(32) Fecha	(33) País
	11/360,801	23-02-2006	US

FIGURA CARACTERISTICA
6 x 6 cm

(85) Fecha inicio fase nacional: 23-09-2008
(86) Datos relativos a la presentación de la solic. PCT
Fecha de presentación de la solicitud: 23-02-2007
No. de solicitud: PCT/US2007/062644

(87) Publicación internacional:
Fecha: 25-10-2007
No. Publicación: WO 2007/120988 A2

(54) Titulo: **CELDA EPROM ACOPLADA A COMPUERTA PARA CABEZAL DE IMPRESIÓN**

(57) Extracto:

Una celda EPROM **(270)** en un circuito de control de un cabezal de impresión para una impresora de chorro de tinta, que tiene exactamente una capa de silicio policristalino **(256)** y una capa conductora **(260)** dispuesta encima de la capa de silicio policristalino, incluye un transistor de control **(272)** y un transistor EPROM **(274)**.

CONTINUA AL RESPALDO ...

108191

The State of Texas

Corporations Section
P.O. Box 13697
Austin, Texas 78711-3697

Phone: 512-463-5555
Fax: 512-463-5709
Dial 7-1-1 For Relay Services
www.sos.state.tx.us

Hope Andrade
Secretary of State

Re: Original Documents

Dear Sir or Madam:

The attached certificate is an original certificate issued by the Secretary of State. Original certificates issued by the Secretary of State are electronically generated. Consequently, such original certificates are in black and white without gold or raised seals, and they bear the electronic signature of the named Secretary of State.

If you have any questions regarding this matter, please call me at 512-463-5578.

Very Truly Yours,

Victoria Castillo

Victoria Castillo
Certifying Team
Office of the Texas Secretary of State

En la Notaría Cuarenta de este Círculo se cotejó la presente fotocopia que coincide con el original que se ha tenido a la vista.
18 MAR. 2009
NOTARIO CUARENTA
Bogotá, D.C., Colombia
Agustín Castillo Zárate

F 169

orations Section
Box 13697
ustin, Texas 78711-3697

Hope Andrade
Secretary of State

Office of the Secretary of State

APOSTILLE
(Convention de La Haye du 5 Octobre 1961)

1.	**Country:** **This Public document**	**United States of America**
2.	**has been signed by**	**Hope Andrade**
3.	**acting in the capacity of**	**Secretary of State**
4.	**bears the seal/stamp of**	**State of Texas**

CERTIFIED

5. **at Austin, Texas**
6. **on March 6, 2009**
7. **by the Director, Business & Public Filings Division**
8. **Certificate No. C00007269**

9. **Seal**

10. **Signature:**

Lorna Wardorf

Director, Business & Public Filings Division

En la Notaría Cuarenta de este Círculo se cotejó la presente fotocopia que coincide con el original que se ha tenido a la vista.
19 MAR. 2009
NOTARIO CUARENTA
Bogotá, D.C., Colombia
Agustín Castillo Zárate

6170

Corporations Section
P.O.Box 13697
Austin, Texas 78711-3697

Hope Andrade
Secretary of State

Office of the Secretary of State

Certificate of Fact

The undersigned, as Secretary of State of Texas, does hereby certify that the document, Certificate Of Limited Partnership for Hewlett-Packard Development Company, L.P. (file number 11287610), a Domestic Limited Partnership (LP), was filed in this office on September 25, 1998.

It is further certified that the entity status in Texas is in existence.

In testimony whereof, I have hereunto signed my name officially and caused to be impressed hereon the Seal of State at my office in Austin, Texas on March 06, 2009.

En la Notaría Cuarenta de este Círculo se cotejó la presente fotocopia que coincide con el original que se ha tenido a la vista.
18 MAR. 2009
NOTARIO CUARENTA
Bogotá, D.C., Colombia
Agustín Castillo Zárate

Hope Andrade
Secretary of State

Phone: (512) 463-5555
Prepared by: Victoria Castillo

Come visit us on the internet at http://www.sos.state.tx.us/
Fax: (512) 463-5709
TID: 10264

Dial: 7-1-1 for Relay Services
Document: 248888340003

• TRADUCCION AL ESPAÑOL del Documento de Certificado de Existencia y Representación Legal de **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.**

[Sello]

Sección de Corporaciones
P.O. Box 13697
Austin, Texas 78711-3697

Tel: 512-463-5555
Fax: 512-463-5709
Marque 7-1-1 Para servicios de Relevo
WWW.sos.state.tx.us

Hope Andrade
Secretario de Estado

Re: Documentos Originales

Estimado señor o señora:

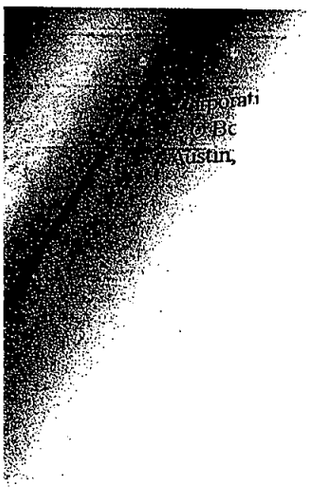
El certificado anexo es un certificado original emitido por el Secretario de Estado. Los certificados originales emitidos por el Secretario de Estado se generan electrónicamente. En consecuencia, dichos certificados originales están a blanco y negro sin sellos dorados o en alto relieve, y llevan la firma electrónica del Secretario de Estado asignado.

Si tienen alguna pregunta con respecto a este asunto, se pueden por favor comunicar conmigo al 512-463-5578.

Atentamente,

Firma

Victoria Castillo
Equipo de Certificaciones
Oficina del Secretario de Estado de Texas



[Sello]

Hope Andrade
Secretario de Estado

Oficina del Secretario de Estado

APOSTILLA
(Convención de La Haya del 5 de octubre de 1961)

1. País: Estados Unidos de América
   Este documento público
2. ha sido firmado por Hope Andrade
3. actuando en capacidad de Secretario del Estado
4. lleva el sello/timbre del Estado de Texas

Certificado

5. en Austin, Texas
6. el 6 de marzo de 2009
7. por el Director, División de Negocios y Presentaciones Públicas
8. Certificado No. COOOO7269
9. Sello/Timbre
10. Firma:

Lorna Wardorf

[Sello]

Director, División de Negocios y Presentaciones Públicas

Visítenos en intemet athttp://www.sos.state.tx.us/

Tel: (512) 463-5555
Preparado por: Victoria Castillo

Fax: (512)463-5709
IID: 10245

Marque: 7-1-1 para Servicios de Relevos
Documento: 248888340003

[redacted]ión de Corporaciones
P.O.Box 13697
Austm, Texas 78711-3697

Hope Andrade
Secretario de Estado

1873

[Sello]

Oficina del Secretario de Estado

Certificado de Hecho

El abajo firmante, como Secretario de Estado por medio del presente certifica que el documento, Certificado de la Sociedad Limitada para HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P..(expediente número 11287610), una Sociedad Doméstica Limitada (LP), fue presentada en esta oficina el 25 de septiembre de 1998.

En testimonio de lo cual, he fijado mi firma oficialmente e impreso el sello del Estado de mi oficina en Austin, Texas el día 6 de marzo de 2009

Firma
Hope Andrade
Secretario de Estado

AS: 108191 174

11

APOSTILLE

(Convention de La Haye du 5 octobre 1961)

Country: *United States of America*

This public document
has been signed by T. Lawrence

acting in the capacity of Certifying Officer

bears the seal/stamp of U.S. Patent and Trademark Office

Certified

at Washington, D.C.

the seventh of October, 2008

by *Assistant Authentication Officer, United States Department of State*

No. 09000684-6

Seal/Stamp:

10. Signature:

Patrick O. Hatchett

A 7149365

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

October 03, 2008

THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF A DOCUMENT RECORDED ON FEBRUARY 23, 2006.

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

T. LAWRENCE
Certifying Officer

PTO-1595
2

03-03-2006

ET

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

Attorney Docket No. 200600453-1

103189171

ne of conveying party(ies).
idy Benjamin

l address of receiving party(ies):

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.
20555 SH 249
Houston, TX 77070

113261 U.S.PTO
11/360801
022306

ıal name(s) of conveying party(ies) attached ___Yes _X_ No

Additional name(s) & address(es) attached? ___Yes _X_ No

ure of Conveyance:

_X_ Assignment ___ Merger ___ Change of Name

___Security Agreement ___ Other

ion Date(s): Feb. 23, 2006

lication number(s) or patent number(s):

document is being filed together with a new application, execution date of the application is: 02/23/2006

ent Application No.(s) B. Patent No.(s)

ation No.: Date Filed:

nation No.: Additional numbers attached? **NO**

ne and address of party to whom correspondence cerning document should be mailed:

ords Manager
llectual Property Administration
WLETT-PACKARD COMPANY
. Box 272400
t Collins, Colorado 80527-2400

6. Total number of applications and patents involved:____

7. Total Fee (37 CFR 3.41): $40.00

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_X_ Authorization to be charged to deposit account.

8. Deposit Account Number: **08-2025**

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When recorded please return to:

HEWLETT-PACKARD COMPANY
Intellectual Property Administrator
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200600453-1

ASSIGNMENT OF PATENT APPLICATION

I/We, the undersigned (each) have agreed and hereby agree to assign to HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas, (hereinafter HPDC), in furtherance of my/our obligations to the Hewlett-Packard Company and its subsidiaries and affiliates, and do hereby assign and transfer to HPDC, its successors and assigns, the entire right, title and interest, including the right of priority, in, to and under an application for Letters Patent of the United States entitled:

GATE-COUPLED EPROM CELL FOR PRINTHEAD

Filing date: _____ Application No.: _____

and the invention(s) and improvement(s) set forth therein, and any and all continuations, continuations-in-part (C-I-P's), divisionals, and renewals of and substitutes for said application for said Letters Patent, and any and all Letters Patent of the United States and of countries foreign thereto which may be granted thereon or therefor; and any reissues, or reexaminations, or extensions of said Letters Patent.

I/we additionally authorize HPDC to file applications in my/our name for Letters Patent in any country, to be held and enjoyed by HPDC, its successors, assigns, nominees or legal representatives, to the full end of the term or terms for which said Letters Patent respectively may be granted, reissued or extended, as fully and entirely as the same would have been held and enjoyed by me/us had this assignment, and transfer not been made;

AND I/we hereby covenant that I/we have full right to convey the entire interest herein assigned, and that I/we have not executed and will not execute any agreement in conflict herewith, and I/we further covenant and agree that I/we will, each time a request is made, and without undue delay, execute and deliver all such papers as may be necessary or desirable to perfect the title to said invention(s) or improvement(s), said application and said Letters Patent, to HPDC, its successors, assigns, nominees or legal representatives, and I/we agree to communicate to HPDC, or to its nominee, all known facts respecting said invention(s) or improvement(s), said application and said Letters Patent, to testify in any legal proceedings, to sign all lawful papers, to execute all disclaimers and divisionals, continuations, C-I-P's; reissue and foreign applications, to make all rightful oaths and declarations, and generally to do everything possible to aid HPDC, its successors, assigns, nominees and legal representatives to obtain and enforce, for its or their own benefit, proper patent protection for said invention(s) or improvement(s) in any and all countries provided the expenses which may be incurred by me/us in lending such cooperation and assistance are paid by HPDC;

AND I/we hereby authorize and request the Commissioner of Patents and Trademarks of the United States and any official of any country or countries foreign to the United States whose duty it is to issue patents on applications as aforesaid, to issue to HPDC, as assignee of the entire right, title and interest, any and all Letters Patent for said invention(s) or improvement(s), including any and all Letters Patent of the United States which may be issued and granted on or as a result of the application aforesaid, in accordance with the terms of this assignment.

I/we further authorize and direct the attorneys of record to insert the serial number and filing date of said application now identified by the attorney docket number and title set forth above as soon as the same shall have been made known to them by the United States Patent and Trademark Office.

IN WITNESS WHEREOF, I/we hereunto set my/our hand(s) and seal(s):

Trudy Benjamin _____ Date Assignment Signed: 2/23/2006
Inventor's Signature (Seal)

Inventor's Typed Name: Trudy Benjamin Date Application Signed: 2/23/2006

State of Washington)
) ss.:
County of)

Before me this ____ day of _____, personally appeared Trudy Benjamin who is personally known or proved to me on the basis of satisfactory evidence to be the person who acknowledged the foregoing instrument of assignment to be his/her free act and deed.

_____
Notary Public
My commission expires:

REPUBLICA DE COLOMBIA
SUPERINTENDENCIA DE INDUSTRIA Y COMERCIO

Folio 178

:020
)ogotá D.C.,

)octor(a)
:ADENA SARMIENTO JUAN PABLO
ıpoderado(a) y/o Representante de
IEWLETT PACKARD DEVELOPMENT COMPANY, L.P.

:EFERENCIA	Radicación No.	08 87789
	Solicitud internacional	PCT/US2007/062644
	Fecha inicio fase nacional	23/09/2008
	Trámite	11
	Evento	378
	Actuación	416
	Oficio No.	8948
	Folios	1

:eniendo en cuenta que la solicitud de privilegio de patente que se tramita bajo el :xpediente indicado en la referencia, reúne los requisitos de forma establecidos en .a Decisión 486 de la Comisión de la Comunidad Andina, el Tratado de Cooperación en ıateria de Patentes (PCT), el Reglamento y la Circular Única de la Superintendencia le Industria y Comercio, se envía el extracto de la solicitud a la Oficina de :omunicaciones para efecto de su publicación en la Gaceta de Propiedad Industrial.

:úmplase
)ado en Bogotá DC, 07 OCT. 2009

ALIX CARMENZA CESPEDES DE VERGEL
Jefe de la división de Nuevas Creaciones

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