URL	TITLE	ABSTRACT	AUTHORS	PUBLICATION
http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6756618&contentType=Conference+Publications	Interfacial delamination analysis at chip/underfill interface and investigation of its effect on flip-chip's reliability	Flip-chip packaging on organic substrate has been used widely as a promising package technology for the next generation of electronic devices. However, due to its numerous interfaces (i.e. die/passivation, passivation/underfill, underfill/solder mask, and solder mask/circuit board), it is more susceptible to a variety of complexworking and testing environments, delamination can easily take place in some critical sites, which is one of the greatest threats to its reliability. In this paper, delamination initiation and propagation behaviors of horizontal and vertical chip/underfill interfaces under temperature cycling tests are analyzed respectively by using cohesive zone model (CZM). The results indicate that delamination will occur first along the horizontal interface between chip and underfill and even when it propagates about 0.13mm, delamination still have not taken place at vertical interface. What's more, variance of phase angle with testing time and crack length is investigated. It turns out that when the crack is short, shearing stress dominates the contribution to causing the interfacial delamination, however, when the crack becomes long, the peeling stress gradually turns to be in the same range or even higher than that of shearing stress. Compared with interfacial delamination in vertical direction, the horizontal one induces a bigger threat to the reliability of flip-chip package because once it propagates to the solder joints, the fatigue life of solder would be reduced rapidly. The effect of interfacial delamination on fatigue life of solders is also implemented in this paper. It is found that plastic strain has been more than doubled in one temperature cycle when interfacial delamination is induced. Fatigue life is estimated by using modified Coffin-Mansin equation. It is found that induced interfacial delamination can decrease the solder's life by about 93.5%. Furthermore, the imperfection of underfill layers and some voids in the corners of the so- der joints caused by the contamination of the flux residues in the corners of the solder joints are also taken into account. And the incremental inelastic strain caused by the voids is compared with that induced by interfacial delamination. It is found that interfacial delamination can lead to much higher plastic strain, that is to say, compared with process-induced defects, delamination has a much greater impact on solder's fatigue life and the whole package's reliability.	Xiang Gao; Fei Wang; Sheng Liu	2013 14th International Conference on Electronic Packaging Technology

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=7028369&contentType=Conference+Publications	Thermo-compression bonding assembly process and reliability studies of Cu pillar bump on Cu/Low-K Chip	The cracking of the brittle ultra low-k dielectrics on advanced node silicon devices is a great concern for assembly processes. It is attributed mainly to various combinations of the Chip-Package-Interaction (CPI) effect. This challenge is further amplified by the adoption of Cu pillars to replace conventional solder bump flip chip interconnects as device bump pitch shrinks and the demand for higher I/O counts per area soars. The high modulus Cu pillar transfers more thermo-mechanical stress to the low k layer and increases the risk of dielectric cracks. The adoption of Cu pillars as interconnects is inevitable because Cu pillars offer better electrical performance than solder, and better a capability of forming finer pitch joints than the solder bump reflow process [1, 2]. It is therefore important to understand the CPI challenges of Cu pillar on low k chip and device to overcome them. This paper reports our studies on the process development challenges when employing TCB-NCP processes on large size (18×18mm) low k chips which were processed by using GLOBALFOUNDRIES' 28nm technology node. Discussions include methods to minimize bond forces for large bonding areas and key underfill (NCP) BOM property selections to mitigate large die size and high bump counts induced by cold joints and low k stress are explored. Thermo-mechanical modeling and simulation to compare TCB-NCP vs. conventional C4 reflow + capillary underfill process on low k layer stress to assist in package BOM selection is also studied and reported.	K. Y. Au; F. X Che; Jie Li Aw; Jong-Kai Lin; Bjoern Boehme; Frank Kuechenmeister	2014 IEEE 16th Electronics Packaging Technology Conference (EPTC)

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=4417068&contentType=Conference+Publications	The Effect of Ni Thickness on Mechanical Strength of Pb-free BGA Spheres on Selectively Plated Ni/Au Finish	As the world is changing to Pb-free solder per EU ROHS Directive, the higher reflow temperature requirement for Pb- free solder has demanded better substrate metal trace to solder mask adhesion to prevent delamination problem. Hence, selective Ni/Au plating process becomes more appealing in the fabrication of substrates to support Pb-free Semiconductor BGA product packaging. However, the set back of selective plating substrate is weaker Pb-free solder joint that leads to higher brittle fracture rate induced by shocking/knocking activities during assembly, test and shipping. In this work, Tape BGA (TBGA) substrates with 3 different Ni thicknesses (range from 2 to 10 mum) were built and attached with Sn3.8Ag0.7Cu Pb-free spheres. Mechanical tests were performed on 2 different levels to examine the strength of the solder joint. On solder joint level, cold ball pull (CBP) and ball shear were used to evaluate the adhesion strength of individual solder joint at Time Zero, after 6 times multiple reflow, and after 168 hours of high temperature storage. The brittle fracture failure rate from this test is believed to have correlation to the missing ball rate in the field. On package level, the tray drop test and packing drop test were conducted to provide a close resemblance to real handling and shipping conditions. Cross-sectioning and SEM investigation were carried out to obtain information on the morphology of intermetallic layer as well as solder mask opening profile. Based on this study, it is determined that the thickness of the Ni needs to be over a certain value (~5.5 mum for Tape BGA) to achieve optimum mechanical strength. By increasing the Ni thickness, the mechanical strength of the thicker Ni solder joint is expected to increase by at least 15% as shown in CBP result, with 3 to 4 times higher resistance against brittle fracture during handling and shipping as demonstrated by tray and packing drop-till-fail test result using center pedestal support trays.	Eu Poh Leng; Min Ding; Joah Rayos; Ibrahim Ahmad; Azman Jalar; Cui Cheng Qiang	2007 32nd IEEE/CPMT International Electronic Manufacturing Technology Symposium

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=8046109&contentType=Early+Access+Articles	Optimum Chip-Tape Adhesion for Reliable Pickup Process	An efficient UV-irradiation process plays an important role for a successful pickup of very thin (<d = 100 μm) Si chips, such as for integrated circuits, power semiconductors, or microelectromechanical systems devices. Before the UV-irradiation process, a dicing tape is laminated on the back of the wafer to hold it tightly (high adhesion strength), which enables rapid and smooth dicing of the wafer into separate Si chips. In the second stage, the adhesive layer is irradiated with UV light through the front side of the backing substrate, which decreases the adhesion strength to the level where the diced chips are picked up easily for further die-bonding processes. However, various malfunctions during the UV-irradiation process can lead to a different and occasionally insufficient UV dose. Consequently, the adhesion is not sufficiently reduced, which could later lead to pickup problems at the die-attach equipment during assembly. In this paper, we present the consequences of an insufficient UV dose on adhesion behavior and pickup efficiency. Using calculated adhesive energy, pickup simulation was done, and accumulated stress in the chips was evaluated at different UV doses. At lower UV doses, the adhesive energy showed rate-dependent behavior, while at higher UV doses, such a behavior was not shown. The accumulated stress within chips showed a linear correlation to adhesive energy, where at lower UV doses, the strength of the silicon chip was exceeded. In the practical process, with an increased pickup rate, higher energy is needed to delaminate the chip. With higher energy needed, accumulated stress in the chip is increased and could lead to the breaking of the chip.	Marko Omazic; Daniel Tscharnuter; Gernot Oreski; Michael Pinczolits; Nika Nikac; Andreas Rappmund; Matko Erceg; Gerald Pinter	IEEE Transactions on Components, Packaging and Manufacturing Technology
http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=7486835&contentType=Conference+Publications	Low temperature bonding using microscale Cu particles coated with thin Sn layers at 200 °C	Sn-Cu intermetallic compounds (IMCs) consisted joints were achieved by a low temperature solid-state bonding using microscale Cu particles coated with thin Sn layers for high temperature die attach application. The bonding process was conducted at 200 °C for 30 min under an applied pressure of 10 MPa using a thermo-compression bonding system. The formic acid atmosphere was used for reducing the oxide layer on the Sn coating and the Cu substrate during the bonding process. After bonding, the joint showed a microstructure fully comprising Cu-Sn intermetallic compounds matrix with a dispersion of pure Cu particles, and a shear strength equivalent to that of conventional Pb-5Sn solder could be achieved. The results demonstrate that low temperature solid-state bonding using microscale Cu particles coated with thin Sn layers has the potential to fulfill the requirement of die attach application.	Xiangdong Liu; Siliang He; Hiroshi Nishikawa	2016 International Conference on Electronics Packaging (ICEP)

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=7028275&contentType=Conference+Publications	Development of fluxless bonding using deposited Gold-indium multi-layer composite for heterogeneous silicon micro-cooler stacking	In this paper, Gold-indium fluxless eutectic bonding at short process time has been successfully developed for stacking multi-layers and heterogeneous structure of silicon micro-cooler. This paper introduces gold-indium eutectic bonding process which uses deposited thin and multilayer composites directly onto the silicon surfaces which to be bonded. The parameters DOE (design of experiment) study was carried out to develop thermal compression bonding process conditions as tabulated in Table 1. These eutectic bonds are examined using shear test, Scanning Electron Microscope (SEM) and Energy Dispersive X-ray Spectroscopy (EDX). This shear test results is compared with eutectic AuSn which is best known as hard solders, good fatigue-resistance and mechanical properties. Nearly void-free bonds are achieved and confirmed by cross-sectional SEM and X-ray scanning. A pre-clean process steps is required to ensure sufficient wetting and good adhesion for this fluxless process. Furthermore, a thermal cycling test and Scanning Acoustic Microscope (SAM) analysis will be carried out to evaluate the failure mode, reliability of solder joint and the bonded structure.	B. L. Lau; Yong Han; H. Y. Zhang; L. Zhang; X. W. Zhang	2014 IEEE 16th Electronics Packaging Technology Conference (EPTC)

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=7159864&contentType=Conference+Publications	A fracture mechanics based parametric study with dimensional variables of the Cu-Cu direct thermo-Compression bonded interface using FEA	Through-silicon via (TSV) technology with micro joint has been highlighted to overcome the limitations of I/O density and system performance enhancement of the conventional flip chip packages. However, the conventional joining methods, represented by the solder joint, cause many reliability problems, such as: intermetallic compound (IMC), thermal expansion coefficient (CTE) mismatch, creep and thermal fatigue problems. As an alternative, copper-to-copper direct bonding (CuDB) has been considered, especially located between a chip and an interposer as a substitute for the micro bump. CuDB enables reduction in fabrication process steps, and obtaining higher interconnect density and enhanced thermal conductivity. However, the CuDB interface has potential reliability risk since the bonding is typically performed at high temperature with a constant downward force in an inert atmosphere. Several papers have reported small voids between the interfaces that can lead crack propagation and delamination. The defect can result in fracture failure of an entire package during its fabrications and operation. This work is a quantitative parametric study about crack propagation at the CuDB interface using finite element methods (FEM). A pre-crack is assigned at the interface of the CuDB to reflect a small void which can be formed during the thermal compressive bonding process. Initial crack length and location, Cu bump diameter and pitch, and TSV diameter and pitch are varied to determine their impact on the crack propagation of the CuDB. As a computational domain, a unit cell including the outermost C4 solder ball, which is under the maximum warpage, is chosen. The unit cell consists of an intermediate layer, two silicon tiers, and a Cu microbump connected to a TSV with total 20 um width and 108 um height. The strain energy release rate (ERR) around the crack tip is calculated for a quantitative assessment. The results are verified with the J-integral method. As results, this stud- provides design recommendations that can minimize interfacial failure of the CuDB and modeling method, which can be used for efficient prediction of its failure possibility.	Ah-Young Park; Satish C. Chaparala; Seung Bae Park	2015 IEEE 65th Electronic Components and Technology Conference (ECTC)

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6698593&contentType=Conference+Publications	New approach for assessment of dielectric layer adhesion strength, demonstrated on eWLB FO-WLP interfaces	In our research, stud pull and shear tests are employed to obtain a quantitative measure of thin film adhesion between mold compound fan-out area and dielectric films in embedded wafer level ball array (eWLB) ICs. This package design uses thin dielectric films as stress buffers to reduce the stress between the second level connections and both the silicon passivation layer and mold compound surfaces. The interface strength or adhesion is typically a difficult physical property to quantify, and in most cases it is not specified by the material manufacturer. Due to the discrepancy of material properties between the different interlayers, adhesion failure is a reliability problem. Therefore, characterizing the influence of different dielectric formulations and process conditions on the interfaces strength is fundamental for a robust package and process. In order to assess these two tests, a set of factors is changed and its impact on film adhesion verified. In the end, the selected methods have been successfully used in the field and showed to be a valuable process instrument for both product development and process monitoring.	Jorge Teixeira; Raquel Pinto; Abel Janeiro; Paulo Cardoso; Mário Ribeiro	2013 Eurpoean Microelectronics Packaging Conference (EMPC)
http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6939653&contentType=Journals+%26+Magazines	Delamination Characteristics in Wide REBCO Coated Conductor Tapes Under Transverse Loading	Superior characteristics and great potential of coated conductor (CC) tapes are some of the promises in pursuit of energy efficient application in electrical field. However, in electric device applications, the coefficient of thermal expansion (CTE) mismatch of each constituent layer, screening current, excessive radial tensile stresses during operation, and other coil fabrication related reasons might cause delamination damage in CC tapes. It was reported that the delamination among its constituent layers resulted to the degradation of its electromechanical properties on coil application. Therefore, the investigation on its delamination behavior is necessary for device application design. In this study, using the anvil test method, the delamination behaviors in 12-mm-wide Cu stabilized and brass laminated GdBa₂Cu₃Oy CC tapes with stainless steel substrate were investigated. The mechanical delamination strength of the CC tapes for differently assembled upper anvil and CC tape configurations about widthwise direction was investigated by using a 4 mm × 8 mm size upper anvil. Mechanical delamination strength of the CC tape was not enhanced by the addition of brass laminate and showed no significant difference depending on the superconducting side or the substrate side. Furthermore, both CC tapes exhibited similar delamination mechanisms and sites but showed different fracture morphologies.	Alking Gorospe; Marlon J. Dedicatoria; Hyung-Seop Shin	IEEE Transactions on Applied Superconductivity

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6135776&contentType=Journals+%26+Magazines	Microtwin Structure and Its Influence on the Mechanical Properties of REBCO Coated Conductors	The elastic properties of REBCO tape (i.e., REBa₂Cu₃ O_{7-d}, RE = Y, Sm and Gd) have been investigated by means of diffraction techniques using synchrotron radiation. Total local strain A_{hkl}^l, which consists of thermal strain A_{hkl}^T and lattice strain A_{hkl}, was analyzed using a microscopic structure model, with two types of microtwin configuration along the tensile axis, i.e., with the [100] or [110] crystal axis oriented parallel to the longitudinal direction of the tape. Experimental results were: (a) slope dA_{h00}^l/dA is larger than dA_{0k0}^l/dA (where A is the external tensile strain), which is attributed to the elastic modulus E_a along the a-axis being smaller than E_b along the b-axis; (b) both dA_{h00}^l/dA and dA_{0k0}^l/dA are smaller than unity, but dA₁₁₀^l/dA is almost unity depending on the configuration of microtwin; (c) the thermal strain for different planes is different as A_{h00}^T ≠ A_{0k0}^T due to the elastic behavior of the superconducting layer being modified because it is constrained by the substrate and the outer metallic layer; and (d) a large Poisson ratio is attributed to this constraint state. It is suggested that the microtwin structure is critical to understand and model this unusual stress/strain behavior.	Kozo Osamura; Shutaro Machiya; Yoshinori Tsuchiya; Hiroshi Suzuki; Takahisa Shobu; Masugu Sato; Shojiro Ochiai	IEEE Transactions on Applied Superconductivity

DATE	TYPE	DOI	ISBN
2013	Conference publication	10.1109/ICEPT.2013.6756618	New-2005_Electronic_978-1-4799-0498-3

2014	Conference publication	10.1109/EPTC.2014.7028369	New-2005_Electronic_978-1-4799-6994-4

2007	Conference publication	10.1109/IEMT.2007.4417068	New-2005_CD-ROM_978-1-4244-1336-2

2017	Early access article	10.1109/TCPMT.2017.2744603	
2016	Conference publication	10.1109/ICEP.2016.7486835	New-2005_CD-ROM_978-4-9040-9016-9

2014	Conference publication	10.1109/EPTC.2014.7028275	New-2005_Electronic_978-1-4799-6994-4

2015	Conference publication	10.1109/ECTC.2015.7159864	New-2005_Electronic_978-1-4799-8609-5

2013	Conference publication	New-2005_Electronic_978-2-9527-4671-7
2015	Journal article	10.1109/TASC.2014.2366074

2012	Journal article	10.1109/TASC.2011.2178847