

Search query (2): [SP]: 1. a decision tree scoring hardware system comprising: a plurality of decision tree processors to access a common feature vector and to execute one or more decision trees with respect to the common feature vector. 2. the decision tree scoring hardware system of claim 1, wherein a first one of the plurality of decision tree processors further execute a first one of the decision trees with respect to the common feature vector concurrently with execution of a second one of the decision tree with respect to the common feature vector by a second one of the decision tree processors. 3. the decision tree scoring hardware system of claim 1, further comprising a decision tree cluster comprising a subset of the plurality of decision tree processors and feature storage to store the common feature vector, the feature storage accessible by the subset of the plurality of decision tree processors within the decision tree cluster. 4. the decision tree scoring hardware system of claim 1, further comprising: a first decision tree cluster comprising: a first subset of the plurality of decision tree processors and a first feature storage, accessible by the first subset of the plurality of decision tree processors, to store the common feature vector and a second decision tree cluster comprising: a second subset of the plurality of decision tree processors and a second feature storage, accessible by the first subset of the plurality of decision tree processors, to store the common feature vector. 5. the decision tree scoring hardware system of claim 1, further comprising a plurality of decision tree clusters, ones of the decision tree clusters comprising subsets of the decision tree processors, the subsets of the decision tree processors output scores based on outcomes of execution of the one or more decision trees, a first one of the decision tree clusters to accept first scores from a first subset of the decision tree processors within the first one of the decision tree clusters, accept at least second score data from a second one of the plurality of decision tree clusters, process the first scores and the at least second score data to produce combined score data. 6. the decision tree scoring hardware system of claim 5, wherein the first one of the decision tree clusters further processes the first scores and the second score data by one of: appending the first scores, or a sum of the first scores, to the second score data to produce the combined score data or summing the first scores with the second score data to produce the combined score data. 7. the decision tree scoring hardware system of claim 1, wherein ones of the decision tree processors output scores based on outcomes of execution of the one or more decision trees, the decision tree scoring hardware system further comprising: a score aggregation network to collect the scores output by the decision tree processors. 8. the decision tree scoring hardware system of claim 1, further comprising one or more of: a plurality of decision tree clusters comprising subsets of decision tree processors, wherein a first one of the plurality of decision tree cluster is to receive the common set of features from a second one of the decision tree clusters and to propagate the common set of features to a third one of the decision tree clusters and a feature network coupled to the decision tree processors to provide the common set of features to the decision tree processors. 9. the decision tree scoring hardware system of claim 1, further comprising a plurality of multi-threaded decision tree processors that concurrently executes a plurality of decision trees in multi-threaded processes. 10. a method comprising: providing a common feature vector to a plurality of decision tree processors implemented within an on-chip decision tree scoring system and executing, by the plurality of decision tree processors, a plurality of decision trees, by reference to the common feature vector. 11. the method of claim 10, further comprising concurrently executing, by the plurality of decision tree processors, the plurality of decision trees by reference to the common feature vector. 12. the method of claim 10, further comprising: outputting, into a score aggregation network, scores for ones of the plurality of decision trees based on outcomes of executing the plurality of decision trees. 13. the method of claim 10, wherein the common feature vector is stored on a feature storage, the method further comprising concurrently: loading another feature vector into the feature storage and executing, by at least one of the decision tree processors, at least one of the plurality of decision trees, the executing including reading one or more features of the common feature vector from the feature storage. 14. the method of claim 10, further comprising propagating the common feature vector throughout a plurality of decision tree clusters, the propagating including receiving the common feature vector from first neighboring decision tree clusters, and passing, by ones of the plurality of decision tree clusters, the feature vector to second neighboring decision tree clusters. 15. a decision tree-walking system comprising: feature storage that stores a common feature vector and a plurality of decision tree processors that accesses the common feature vector from the feature storage and executes a plurality of decision trees by comparing threshold values of the decision trees to feature values within the common feature vector. 16. the decision tree-walking system of claim 15, wherein the plurality of decision tree processors concurrently execute the plurality of decision trees. 17. the decision tree-walking system of claim 15, further comprising: another feature storage that stores the common feature vector and another plurality of decision tree processors that accesses the common feature vector from the other feature storage and executes another plurality of decision trees by comparing other threshold values of the other plurality of decision trees to the feature values within the common feature vectors. 18. the decision tree-walking system of claim 15, wherein the plurality of decision tree processors is a first plurality of decision tree processors, the on-chip decision tree-walking system further comprising a plurality of decision tree clusters, a first one of the decision tree clusters including the first plurality of decision tree processors, the first one the plurality of decision tree clusters: receives first score data output by the first plurality of decision tree processors receives second score data from one or more first neighboring decision tree clusters processes the first score data with the second score data to produce third score data and passes the third score data to one or more second neighboring decision tree clusters. 19. the decision tree-walking system of claim 15, concurrently writing another common feature vector to the feature storage with the access of the feature vector by the plurality of decision tree processors. 20. the decision tree-walking system of claim 15, wherein the feature storage and the plurality of decision tree processors are first feature storage and a first plurality of decision tree processors included in a first programmable logic device, first application-specific integrated circuit, or first on-chip processor with an enhanced instruction set, the plurality of decision trees are a first plurality of decision trees, and the decision tree-walking system further includes: a second programmable logic device, second application-specific integrated circuit, or second on-chip processor with an enhanced instruction set that includes: second feature storage to store the common feature vector and a second plurality of decision tree processors that accesses the common feature vector from the second feature storage and executes a second plurality of decision trees by comparing second threshold values of the second decision trees to the feature values within the common feature vector the second programmable logic device, second application-specific integrated circuit, or second on-chip processor with an enhanced instruction set: receives first score data from the first programmable logic device, first application-specific integrated circuit, or first on-chip processor with an enhanced instruction set, the first score data resulting from execution of the first plurality of decision trees and processes the first score data with second score data resulting from execution of the first plurality of decision trees to produce combined score data for the common feature vector.

Results: 6

Search history

Search pn=W02015142595 (Results 1)

1:

Search [SP]: 1. a decision tree scoring hardware system comprising: a plurality of decision tree processors to access a common feature vector and to execute one or more decision trees with respect to the common feature vector. 2. the decision tree scoring hardware system of claim 1, wherein a first one of the plurality of decision tree processors further execute a first one of the decision trees with respect to the common feature vector concurrently with execution of a second one of the decision tree with respect to the common feature vector by a second one of the decision tree processors. 3. the decision tree scoring hardware system of claim 1, further comprising a decision tree cluster comprising a subset of the plurality of decision tree processors and feature storage to store the common feature vector, the feature storage accessible by the subset of the plurality of decision tree processors within the decision tree cluster. 4. the decision tree scoring hardware system of claim 1, further comprising: a first decision tree cluster comprising: a first subset of the plurality of decision tree processors and a first feature storage, accessible by the first subset of the plurality of decision tree processors, to store the common feature vector and a second decision tree cluster comprising: a second subset of the plurality of decision tree processors and a second feature storage, accessible by the first subset of the plurality of decision tree processors, to store the common feature vector. 5. the decision tree scoring hardware system of claim 1, further comprising a plurality of decision tree clusters, ones of the decision tree clusters comprising subsets of the decision tree processors, the subsets of the decision tree processors output scores based on outcomes of execution of the one or more decision trees, a first one of the decision tree clusters to accept first scores from a first subset of the decision tree processors within the first one of the decision tree clusters, accept at least second score data from a second one of the plurality of decision tree clusters, process the first scores and the at least second score data to produce combined score data. 6. the decision tree scoring hardware system of claim 5, wherein the first one of the decision tree clusters further processes the first scores and the second score data by one of: appending the first scores, or a sum of the first scores, to the second score data to produce the combined score data or summing the first scores with the second score data to produce the combined score data. 7. the decision tree scoring hardware system of claim 1, wherein ones of the decision tree processors output scores based on outcomes of execution of the one or more decision trees, the decision tree scoring hardware system further comprising: a score aggregation network to collect the scores output by the decision tree processors. 8. the decision tree scoring hardware system of claim 1, further comprising one or more of: a plurality of decision tree clusters comprising subsets of decision tree processors, wherein a first one of the plurality of decision tree cluster is to receive the common set of features from a second one of the decision tree clusters and to propagate the common set of features to a third one of the decision tree clusters and a feature network coupled to the decision tree processors to provide the common set of features to the decision tree processors. 9. the decision tree scoring hardware system of claim 1, further comprising a plurality of multi-threaded decision tree processors that concurrently executes a plurality of decision trees in multi-threaded processes. 10. a method comprising: providing a common feature vector to a plurality of decision tree processors implemented within an on-chip decision tree scoring system and executing, by the plurality of decision tree processors, a plurality of decision trees, by reference to the common feature vector. 11. the method of claim 10, further comprising concurrently executing, by the plurality of decision tree processors, the plurality of decision trees by reference to the common feature vector. 12. the method of claim 10, further comprising: outputting, into a score aggregation network, scores for ones of the plurality of decision trees based on outcomes of executing the plurality of decision trees. 13. the method of claim 10, wherein the common feature vector is stored on a feature storage, the method further comprising concurrently: loading another feature vector into the feature storage and executing, by at least one of the

decision tree processors, at least one of the plurality of decision trees, the executing including reading one or more features of the common feature vector from the feature storage. 14. the method of claim 10, further comprising propagating the common feature vector throughout a plurality of decision tree clusters, the propagating including receiving the common feature vector from first neighboring decision tree clusters, and passing, by ones of the plurality of decision tree clusters, the feature vector to second neighboring decision tree clusters. 15. a decision tree-walking system comprising: feature storage that stores a common feature vector and a plurality of decision tree processors that accesses the common feature vector from the feature storage and executes a plurality of decision trees by comparing threshold values of the decision trees to feature values within the common feature vector. 16. the decision tree-walking system of claim 15, wherein the plurality of decision tree processors concurrently execute the plurality of decision trees. 17. the decision tree-walking system of claim 15, further comprising: another feature storage that stores the common feature vector and another plurality of decision tree processors that accesses the common feature vector from the other feature storage and executes another plurality of decision trees by comparing other threshold values of the other plurality of decision trees to the feature values within the common feature vectors. 18. the decision tree-walking system of claim 15, wherein the plurality of decision tree processors is a first plurality of decision tree processors, the on-chip decision tree-walking system further comprising a plurality of decision tree clusters, a first one of the decision tree clusters including the first plurality of decision tree processors, the first one the plurality of decision tree clusters: receives first score data output by the first plurality of decision tree processors receives second score data from one or more first neighboring decision tree clusters processes the first score data with the second score data to produce third score data and passes the third score data to one or more second neighboring decision tree clusters. 19. the decision tree-walking system of claim 15, concurrently writing another common feature vector to the feature storage with the access of the feature vector by the plurality of decision tree processors. 20. the decision tree-walking system of claim 15, wherein the feature storage and the plurality of decision tree processors are first feature storage and a first plurality of decision tree processors included in a first programmable logic device, first application-specific integrated circuit, or first on-chip processor with an enhanced instruction set, the plurality of decision trees are a first plurality of decision trees, and the decision tree-walking system further includes: a second programmable logic device, second application-specific integrated circuit, or second on-chip processor with an enhanced instruction set that includes: second feature storage to store the common feature vector and a second plurality of decision tree processors that accesses the common feature vector from the second feature storage and executes a second plurality of decision trees by comparing second threshold values of the second decision trees to the feature values within the common feature vector the second programmable logic device, second application-specific integrated circuit, or second on-chip processor with an enhanced instruction set: receives first score data from the first programmable logic device, first application-specific integrated circuit, or first on-chip processor with an enhanced instruction set, the first score data resulting from execution of the first plurality of decision trees and processes the first score data with second score data resulting from execution of the first plurality of decision trees to produce combined score data for the common feature vector. (Results 6)

Title: MESH CONNECTED COMPUTER

Abstract: Source: US6212628B [EN] An apparatus for processing data has a Single-Instruction-Multiple-Data (SIMD) architecture, and a number of features that improve performance and programmability. The apparatus includes a rectangular array of processing elements and a controller. In one aspect, each of the processing elements includes one or more addressable storage means and other elements arranged in a pipelined architecture. The controller includes means for receiving a high level instruction, and converting each instruction into a sequence of one or more processing element microinstructions for simultaneously controlling each stage of the processing element pipeline. In doing so, the controller detects and resolves a number of resource conflicts, and automatically generates instructions for registering image operands that are skewed with respect to one another in the processing element array. In another aspect, a programmer references images via pointers to image descriptors that include the actual addresses of various bits of multi-bit data. Other features facilitate and speed up the movement of data into and out of the apparatus. "Hit" detection and histogram logic are also included.

Classifications:

International (IPC 8-9): G06F9/30 G06F9/302 G06F9/318 G06F9/34 G06F9/38 G06T1/00 G06T1/20 (Advanced/Invention); G06F9/302 (Advanced/Non-invention);

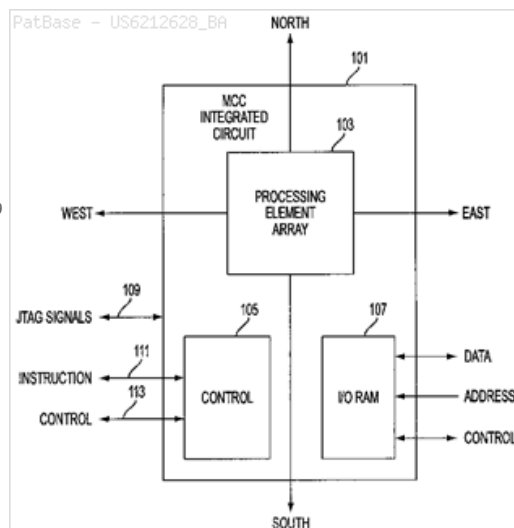
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International (IPC 1-7): G06F12/00 G06F9/318 G06F9/34 G06F9/38 G06T1/00 G06T1/20

CPC: G06F9/3885 G06F9/30025 G06F9/3013 G06F9/30014 G06F9/30036 G06F9/30145 G06F9/30167 G06F9/30181 G06F9/30189 G06F9/34 G06F9/3824 G06T1/20

European: G06F9/30A1A1 G06F9/30A1P G06F9/30T G06F9/30T4T G06F9/30X G06F9/34 G06F9/38D G06F9/38S G06T1/20

US: 711/202 712/14 712/16 712/224 712/226 712/E09.017 712/E09.028 712/E09.035 712/E09.038 712/E09.046 712/E09.069 712/E9.017 712/E9.028 712/E9.035 712/E9.038 712/E9.046 712/E9.069 712/E9.17 712/E9.28 712/E9.35 712/E9.38 712/E9.46 712/E9.69



Family:

Publication number	Publication date	Application number	Application date
AU199936366 A1	19991101	AU19990036366	19990409
CO4880829 A1	20000131	CO19990021049	19990409
EP1068592 A2	20010117	EP19990918447	19990409
TW428152 B	20010401	TW19990105653	19990409
US6212628 BA	20010403	US19980057481	19980409
US6275920 BA	20010814	US20000552319	20000424
WO9953439 A2	19991021	WO1999US07002	19990409
WO9953439 A3	20000330	WO1999US07002	19990409

Priority:

US19980057481 19980409 US20000552319 20000424 WO1999US07002 19990409

Probable Assignee: GEO SEMICONDUCTOR INC

Assignee(s): (std): TERANEX INC ; LOCKHEED CORP

Assignee(s): LOCKHEED MARTIN CORP ; SILICON OPTIX INC ; SO DELAWARE ; SO DELAWARE (F K A SILICON OPTIX INC SUCCESSOR IN INTEREST TO TERANEX INC) AS CORP ; ROADMAP GEO LP III ADMINISTRATIVE AGENT AS ; SCOTT LAKE HOLDINGS INC ; BISHOPSGATE HOLDINGS CORP ; GEO SEMICONDUCTOR INC ; UNITED STATES AIR FORCE AFMC LO JAZ ; SUNTRUST BANK ; VENTURE LENDING AND LEASING IV INC ; UNITED STATES AIR FORCE ; SO DELAWARE CORP ; TERANEX SYSTEMS INC ; SO DELAWARE F K A SILICON OPTIX INC SUCCESSOR IN I ; SUNTRUST BANK SUNTRUST ; SO DELAWARE F K A SILICON OPTIX INC SUCCESSOR IN INTEREST TO TERANEX INC CORP AS ; SO DELAWARE F K A SILICON OPTIX INC SUCCESSOR IN INTEREST TO TERANEX INC AS CORP ; SUNTRUST BANK (SUNTRUST) ; VENTURE LENDING AND LEASING IV INC AND VENTURE LEN ; VENTURE LENDING AND LEASING IV INC AND VENTURE LENDING AND LEASING V INC

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Agent(s): GERMAN CASTILLO GRAU

Designated states: AE AL AM AT AU AZ BA BB BE BF BG BJ BR BY CA CF CG CH CI CM CN CU CY CZ DE DK EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MC MD MG MK ML MN MR MW MX NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT UA UG UZ VN YU ZA ZW

Title: CREATING ENSEMBLES OF DECISION TREES THROUGH SAMPLING

Abstract: Source: US2003229630A [EN] A system for decision tree ensembles that includes a module to read the data, a module to sort the data, a module to evaluate a potential split of the data according to some criterion using a random sample of the data, a module to split the data, and a module to combine multiple decision trees in ensembles. The decision tree method is based on statistical sampling techniques and includes the steps of reading the data; sorting the data; evaluating a potential split according to some criterion using a random sample of the data, splitting the data, and combining multiple decision trees in ensembles.

Classifications:

International (IPC 8-9): G06F17/30 G06F7/00 G06K9/62 G06N5/02 (Advanced/Invention);

G06F17/30 G06F7/00 G06K9/62 G06N5/00 (Core/Invention)

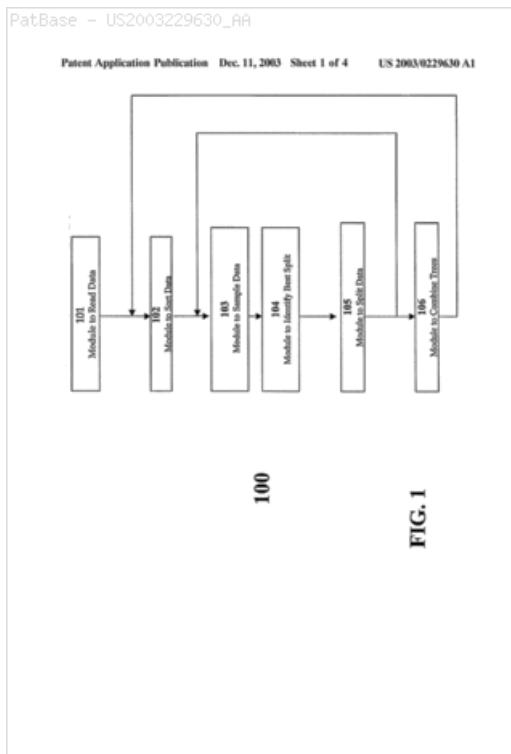
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CPC: Y10S707/99943 G06K9/6282 G06N5/022

European: G06F17/30Z1T G06K9/62C2M2A G06N5/02K

US: 1/1 1/1P 705/7 706/14 707/102 707/3 707/999.003

707/999.003S 707/999.102 707/E17.012 707/E17.012S

**Family:**

Publication number	Publication date	Application number	Application date
US2003229630 AA	20031211	US20020167892	20020611
US6938049 BB	20050830	US20020167892	20020611

Priority:

US20020167892 20020611

Probable Assignee: LAWRENCE LIVERMORE NATIONAL SECURITY LLC

Assignee(s): (std): UNIV CALIFORNIA

Assignee(s): CALIFORNIA UNIV ; CALIFORNIA UNIV OF THE ; CALIFORNIA UNIVERSITY ; ENERGY US DEPARTMENT OF ENERGY ; ENERGY US DEPARTMENT OF ENERGY PO BOX ; LAWRENCE LIVERMORE NATIONAL SECURITY LLC ; THE REGENTS OF THE UNIVERSITY OF CALIFORNIA ; THE UNIV OF CALIFORNIA

Inventor(s): (std): CANTU PAZ ERICK ; KAMATH CHANDRIKA

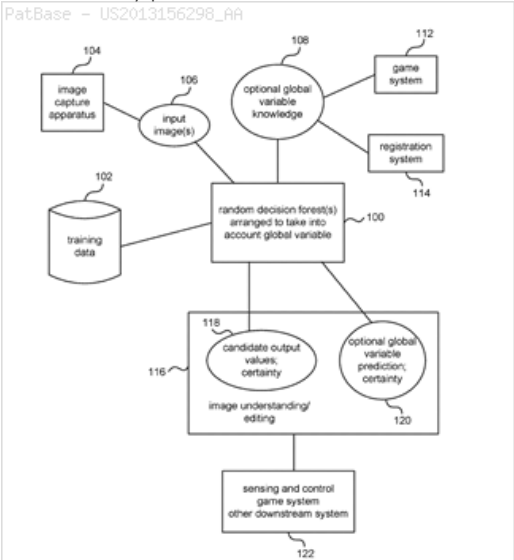
Agent(s): SCOTT EDDIE E; THOMPSON ALAN H; ALAN H; EDDIE E

Title: USING HIGH-LEVEL ATTRIBUTES TO GUIDE IMAGE PROCESSING

Abstract: Source: US2013156298A [EN] Using high-level attributes to guide image processing is described. In an embodiment high-level attributes of images of people such as height, torso orientation, body shape, gender are used to guide processing of the images for various tasks including but not limited to joint position detection, body part classification, medical image analysis and others. In various embodiments one or more random decision forests are trained using images where global variable values such as player height are known in addition to ground-truth data appropriate for the image processing task concerned. In some examples sequences of images are used where global variables are static or vary smoothly over the sequence. In some examples one or more trained random decision forests are used to find global variable values as well as output values for the task concerned such as joint positions or body part classes.

Classifications:

International (IPC 8-9): G06K9/00 G06K9/62
G06K9/68 (Advanced/Invention)
CPC: G06K9/00362 G06K9/469
US: 382/153 382/159 382/226



Family:

Publication number	Publication date	Application number	Application date
US2013156298 AA	20130620	US20110327464	20111215
US8879831 BB	20141104	US20110327464	20111215

Priority:

US20110327464 20111215

Probable Assignee: MICROSOFT TECHNOLOGY LICENSING LLC

Assignee(s): (std): KOHLI PUSHMEET ; MICROSOFT CORP ; SHOTTON JAMIE DANIEL JOSEPH ; SUN MIN

Assignee(s): MICROSOFT TECHNOLOGY LICENSING LLC

Inventor(s): (std): KOHLI PUSHMEET ; SHOTTON JAMIE DANIEL JOSEPH ; SUN MIN

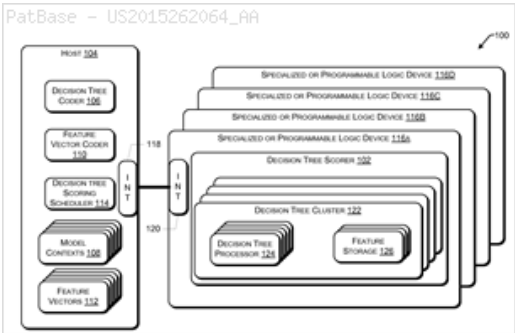
Agent(s): JUDY; MICKY; STEVE

Title: PARALLEL DECISION TREE PROCESSOR ARCHITECTURE

Abstract: Source: US2015262064A [EN] Disclosed herein is a decision tree multi-processor system. The system includes a plurality of decision tree processors that access a common feature vector and execute one or more decision trees with respect to the common feature vector.

Classifications:

International (IPC 8-9): G06F17/30 G06N5/02
G06N99/00 (Advanced/Invention);
G06F17/30 (Core/Invention)
CPC: G06N5/022 G06F17/30961 G06F17/30979
US: 706/46



Family:

Publication number	Publication date	Application number	Application date
AU2015231828 AA	20150924	AU20150231828	20150312
BR112016020215 A2	20170815	BR20161120215	20150312
CA2939959 AA	20160817	CA20152939959	20150312
CL2016002294 A1	20170324	CL20160002294	20160913
CN106133721 A	20161116	CN201580014613	20150312
CO20160002623 A2	20170209	CO20160002623	20161003
EP3120262 A1	20170125	EP20150713082	20150312
ID201706091 A	20170609	ID2016P0005890	20150312
IN201647031543 A	20161104	IN201647031543	20160915
JP2017517082 T2	20170622	JP20170501068T	20150312
KR20160132853 A	20161121	KR20167025570	20150312
MX2016011670 A1	20161107	MX20160011670	20150312
PH2016501639 A	20161003	PH20160501639	20160817
SG11201607431X A1	20161028	SG20161107431	20150312
TH169001 A	20171012	TH20161005013	20150312
US2015262064 AA	20150917	US20140216990	20140317
WO15142595 A1	20150924	WO2015US20050	20150312

Priority:

US20140216990 20140317 WO2015US20050 20150312

Probable Assignee: MICROSOFT TECHNOLOGY LICENSING LLC

Assignee(s): (std): MICROSOFT CORP ; MICROSOFT TECHNOLOGY LICENSING LLC ; MICROSOFT TECH LICENSING LLC

Assignee(s): PUTNAM ANDREW ; BURGER DOUGLAS C ; GRAY JAN ; LARUS JAMES R

Inventor(s): (std): ANDREW PUTNAM ; BURGER DOUGLAS C ; DOUGLAS C BURGER ; GRAY JAN ; JAMES R LARUS ; JAN GRAY ; LARUS JAMES R ; PUTNAM ANDREW

Agent(s): DAVIES COLLISON CAVE; DAVIES COLLISON CAVE PTY LTD; SMART AND BIGGAR; ESTUDIO FEDERICO VILLASECA Y CIA; LUZ HELENA ADARVE GOMEZ; FISCHER MICHAEL MARIA; LANNY SETIAWAN MBA MGMT MA LPC MA LMFT; YAMAMOTO OSAMU; TAKEUCHI SHIGEO; ONO SHINJIRO; KOBAYASHI YASUSHI

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: DECISION TREE THRESHOLD CODING

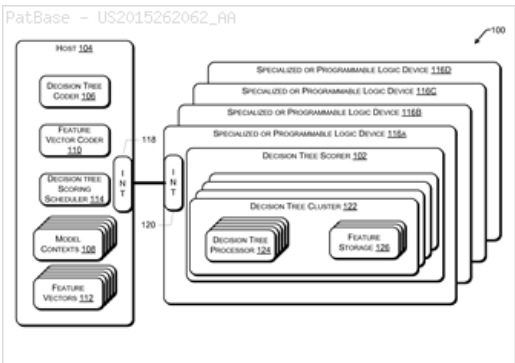
Abstract: Source: US2015262062A [EN] Disclosed herein are systems and methods for coding decision trees, such as for execution on a decision tree scorer system. A computing system determines, for a particular feature of a plurality of features included in one or more decision trees, a list of unique threshold values associated with the particular feature in the one or more decision trees. The computing system determines a plurality of threshold index values for the list of unique threshold values, and represents the one or more decision trees such that decision nodes of the one or more decision trees associated with the particular feature include ones of the threshold index values.

Classifications:

International (IPC 8-9): G06F17/30 G06N5/02 (Advanced/Invention)

CPC: G06N5/025 G06F17/30961

US: 706/46



Family:

Publication number	Publication date	Application number	Application date
US2015262062 AA	20150917	US20140216663	20140317

Priority:

US20140216663 20140317

Probable Assignee: MICROSOFT TECHNOLOGY LICENSING LLC

Assignee(s): (std): MICROSOFT CORP

Assignee(s): MICROSOFT TECHNOLOGY LICENSING LLC

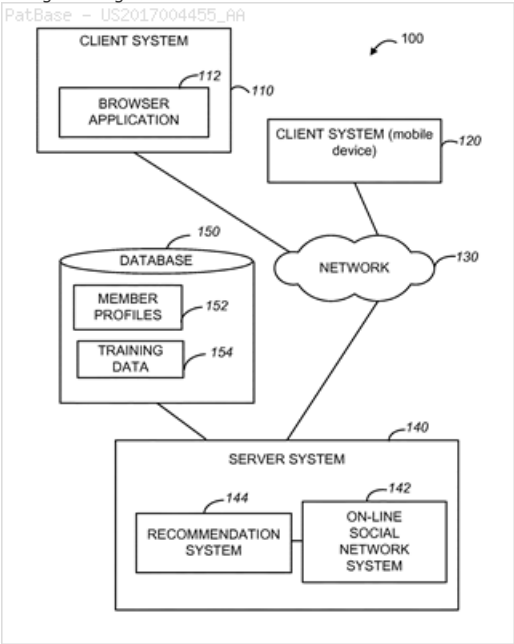
Inventor(s): (std): BURGER DOUGLAS C ; GRAY JAN ; LARUS JAMES R ; PUTNAM ANDREW

Title: NONLINEAR FEATURIZATION OF DECISION TREES FOR LINEAR REGRESSION MODELING

Abstract: Source: US2017004455A [EN] Nonlinear featurization of decision trees for linear regression modeling in the context of an on-line social network is described. A computer-implemented converter is provided that is capable of reading a decision tree structure that is included in the learning to rank algorithm and convert each path from root to a leaf into an s-expression. The s-expressions are used as additional features to train a logistic regression model.

Classifications:

International (ipc 8-9): G06F17/30 G06N99/00
G06Q10/10 (Advanced/Invention)
CPC: G06Q10/1053 G06F17/30327 G06N99/005 G06Q50/01
G06N5/025
US: 705/321



Family:

Publication number	Publication date	Application number	Application date
US2017004455 AA	20170105	US20150788717	20150630

Priority:

US20150788717 20150630

Probable Assignee: LINKEDIN CORP

Assignee(s): (std): LINKEDIN CORP

Assignee(s): MICROSOFT TECHNOLOGY LICENSING LLC

Inventor(s): (std): HARDTKE DAVID ; HUANG ERIC ; MIAO XU ; TANG LIJUN ; YOUNG JEOL DANIEL ; ZHOU YITONG