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Analysis of a parallel lexical-tree-based speech decoder for multi-core processors

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Abstract:
We present a systematic analysis of a lexical-tree based parallel search algorithm for multi-core desktop processors. We introduce an analytical model that predicts the speedup from parallelization after accounting for load imbalance among the cores. Various sources of overhead in the parallel search algorithm are described, benchmarked and analyzed. Besides load imbalance, these include the inherently serial steps of the parallel search algorithm and an increase in main memory access latency.

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