

Packaging meets heterogeneous integration driving direction for advanced system in packages

Sign In or Purchase
to View Full Text

Related Articles

[Point to point GALS interconnect](#)

[SPA - a synthesisable Amulet core for smartcard applications](#)

[View All](#)

3

Author(s)

✓ M. Juergen Wolf ; ✓ Wolfram Steller ; ✓ Klaus-Dieter Lang

[View All Authors](#)

Abstract

[Authors](#)

[Figures](#)

[References](#)

[Citations](#)

[Keywords](#)

[Metrics](#)

[Media](#)

Abstract:

Heterogeneous integration of different devices by using 3D architectures allows the realization of application specific System in Packages (SiP) with a high functionality in a cost effective way. Enabling building blocks technologies are substrate-, interconnect-, assembly- and device integration technologies to integrate sensors, ASICs, transceiver, memories and passive elements. SiPs based on interposer architectures are very attractive due to system performance improvements and due to optimized form factor achievements on wafer level.

Published in: [Pan Pacific Microelectronics Symposium \(Pan Pacific\)](#), 2018

Date of Conference: 5-8 Feb. 2018

DOI: [10.23919/PanPacific.2018.8318987](#)

Date Added to IEEE Xplore: 19 March 2018

Publisher: IEEE

► **ISBN Information:**

Conference Location: Waimea, HI, USA