

Search history

Search 1: (USB or Universal Serial Bus) and (debug* or EUD or diagnos*) and electronic* (Results 34073)
Search 2: 1 and JTAG and hub and interface+ and peripheral (Results 197)
Search 3: 1 and JTAG and hub and peripheral (Results 198)
Search 4: 3 and (send* or convert* or trasmit* or transport*) and (data or packet*) (Results 195)
Search 5: 4 and oscillator* and (suppl* or source*) (Results 106)
Search 6: 5 and (SWD or serial wire debug) and COM (Results 1)
Search 7: 5 and (SOC or IC or SIP) and super speed (Results 5)
Search 8: 5 and PD<20141030 (Results 98)
Search 9: 8 and IC = G06F* (Results 57)

Title: RELATIVELY UNIQUE ID IN INTEGRATED CIRCUIT

Abstract: A method of manufacturing a series of integrated circuits having related functionality, the method including the steps of: (a) determining an identifier; (b) permanently storing the identifier on one of the integrated circuits; (c) repeating steps (a) and (b) for each integrated circuit in the series; and wherein the identifiers for the series are determined in such a way that knowing the identifier of one of the integrated circuits does not improve the ability of an attacker to determine the identifier of any of the other integrated circuits.

Classifications:

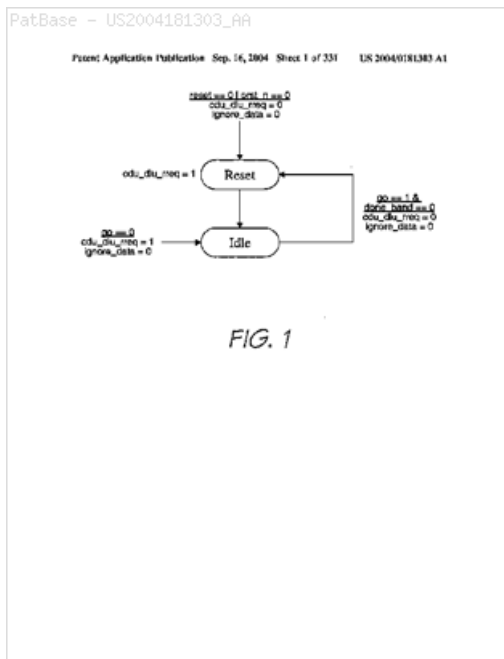
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**Family:**

Publication number	Publication date	Application number	Application date
AU2002953134 A0	20021219	AU20020953134	20021202
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Priority:

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US20060488841 20060719		

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EP1765595 B1	20110316	EP20040734974	20040527
EP2301753 A1	20110330	EP20100193974	20040527
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PT2301753 T	20130123	PT20100193974T	20040527
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Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NA NE NI NL NO NZ OM PG PH PL PT RO RU SC SD SE SG SI SK SL SN SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Title: VOICE GATEWAY WITH DOWNSTREAM VOICE SYNCHRONIZATION

Abstract: A network gateway is configured to facilitate on line and off line bi-directional communication between a number of near end **data** and telephony devices with far end **data** termination devices via a hybrid fiber coaxial network and a cable modem termination system. The described network gateway combines a QAM receiver, a transmitter, a DOCSIS MAC, a CPU, a voice and audio processor, a voice synchronizer, an Ethernet MAC, and a **usb** controller to provide high performance and robust operation. It is emphasized that this abstract is provided to comply with the rules requiring an abstract which will allow a searcher or other reader to quickly ascertain the subject matter of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or the meaning of the claims.

Classifications:

International (ipc 8-9): E05C1/00 G01R31/08 G06F11/00 G10L11/02 G10L11/04 G10L11/06 G10L19/14 G10L21/02 H04B1/44 H04B3/04 H04B3/20 H04B3/23 H04B3/30 H04B7/216 H04J1/02 H04J1/16 H04J3/00 H04J3/06 H04J3/10 H04J3/12 H04J3/14 H04J3/16 H04J3/22 H04L1/00 H04L12/26 H04L12/28 H04L12/54 H04L12/56 H04L12/58 H04L12/64 H04L12/66 H04L27/06 H04L27/08 H04L29/06 H04L29/08 H04L5/14 H04L7/00 H04L7/04 H04M1/24 H04M1/253 H04M11/00 H04M3/00 H04M3/22 H04M7/00 H04M7/12 H04M9/08 H04N21/2383 H04N21/438 H04N7/10 H04N7/173 H04N7/24 H04N7/52 H04Q1/45 (Advanced/Invention); E05C1/00 G10L21/02 H04L1/00 H04L12/28 H04L29/08 H04Q1/45 (Advanced/Non-invention); G10L11/00 H04B3/23 H04J3/06 H04L12/28 H04L12/54 H04L12/66 H04L29/06 H04M11/00 H04M7/00 (Core/Invention); E05C1/00 G10L21/00 H04L29/08 (Core/Non-invention)

International (ipc 1-7): H04B1/707 H04B3/20 H04B3/23 H04J1/02 H04J3/06 H04J3/16 H04L1/00 H04L12/26 H04L12/28 H04L12/56 H04L12/64 H04L12/66 H04L27/14 H04L27/30 H04L29/06 H04L29/06 H04L7/00 H04L7/02 H04L7/04 H04M1/24 H04M1/253 H04M11/00 H04M3/00 H04M7/00 H04M9/08 H04N7/173 H04N7/52

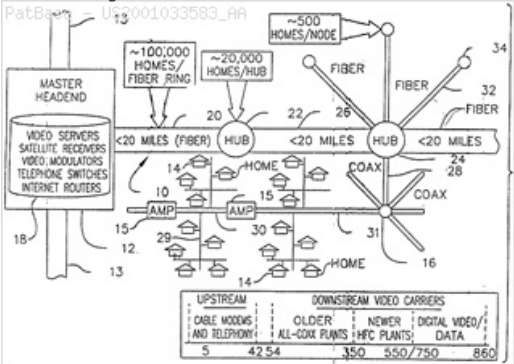
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Family:

Publication number	Publication date	Application number	Application date
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Designated states:

AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CR CU CY CZ DE DK DM DZ EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Title: CACHE UPDATING METHOD AND APPARATUS

Abstract: A method of updating a cache in an integrated circuit comprising: the cache; a processor connected to the cache via a cache bus; a memory interface connected to the cache via a first bus and to the processor via a second bus, the first bus being wider than the second bus or the cache bus; and memory connected to the memory interface via a memory bus; the method comprising the steps of: (a) following a cache miss, using the processor to issue a request for first **data** via a first address, the first **data** being that associated with the cache miss; (b) in response to the request, using the memory interface to fetch the first **data** from the memory, and **sending** the first **data** to the processor; (c) **sending**, from the memory interface and via the first bus, the first **data** and additional **data**, the additional **data** being that stored in the memory adjacent the first **data**; (d) updating the cache with the first **data** and the additional **data** via the first bus; and (e) updating flags in the cache associated with the first **data** and the additional **data**, such that the updated first **data** and additional **data** in the cache is valid.

Classifications:

International (IPC 8-9): B23P17/00 B41J2/01 B41J2/015 B41J2/05 B41J2/135 B41J2/155 B41J2/165 B41J2/175 B41J2/21 B41J29/38 B41J29/393 G06F1/00 G06F1/08 G06F12/00 G06F12/02 G06F12/10 G06F13/00 G06F13/28 G06F19/00 G06F21/00 G06F9/36 H03K19/00 H04L9/00 H04N1/40 H04N1/405 (Advanced/Invention); B41J2/01 B41J2/05 G06F12/10 G06F13/20 G06F21/00 H04L9/00 H04N1/40 H04N1/405 (Core/Invention)

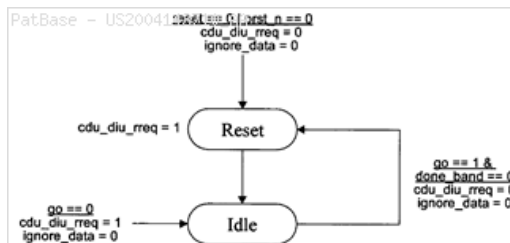
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CPC: G06F12/0859 G06F12/0891 G06F12/12 Y10S707/99933

Y10S707/99939 Y10T29/49401 G06F21/73 B41J2/04508 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 G06F21/445 H04N1/405 B41J2/04505 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20

European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F12/08B20 G06F12/08B6P4 G06F12/12 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20

US: 29/890.1 29/890.100P 323/313 326/8 327/156 327/158 327/263 331/16 331/57 347/109 347/109P 347/12 347/12P 347/12S 347/13 347/13P 347/14 347/15 347/19 347/20 347/20P 347/29 347/42 347/49 347/5 347/5P 347/67 347/86 347/86P 347/87 347/9 358/1.14 358/1.140P 358/3.13 358/3.130P 380/255 380/255P 455/556.2 455/556.200S 455/558 455/558S 702/106 709/225 709/225P 711/103 711/103S 711/118 711/128 711/137 711/141 711/141S 711/144 711/144P 711/157 711/158 711/164 711/3 711/3P 711/E12.008 711/E12.008S 711/E12.022 711/E12.051 711/E12.069 713/171 713/200 713/300 713/340 713/340P 713/503 713/503P 726/22 726/22P

**Family:**

Publication number	Publication date	Application number	Application date
AU2003302611 AA	20040623	AU20030302611	20031202
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CA2508141 AA	20050601	CA20032508141	20031202
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Inventor(s): GARY SHIPTON ; WALMSLEY SIMON R SILVERBROOK RESEARCH PTY LTD ; WALMSLEY SIMON ROBERTAU ; PAUL LAPSTUN ; MARK JACKSON PULVER ; KIA SILVERBROOK ; SIMON ROBERT WALMSLEY ; RICHARD THOMAS PLUNKETT ; JACKSON PULVER MARK SILVERBROOK RESEACH PTY LTD ; JACKSON PULVER MARKAU ; LAPSTUN PAUL SILVERBROOK RESEARCH PTY LTD ; LAPSTUN PAULAU ; PLUNKETT RICHARD ; PLUNKETT RICHARD T SILVERBROOK RESEARCH PTY LTD ; PLUNKETT RICHARD THOMASAU ; SHIPTON GARY SILVERBROOK RESEARCH PTY LTD ; SHIPTON GARYAU ; SILVERBROOK KIA SILVERBROOK RESEARCH PTY LTD ; SILVERBROOK KIAAU ; WALMSLEY SIMON

Agent(s): SILVERBROOK RESEARCH PTY LTD; PIZZEYS PATENT AND TRADE MARK ATTORNEYS; PIZZEYS PATENT AND TRADE MARK ATTORNEYS PTY LTD; OYEN WIGGS GREEN AND MUTALA LLP; MOORE BARRY

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NI NL NO NZ OM PG PH PL PT RO RU SC SD SE SG SI SK SL SN SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Title: TIGHTLY-COUPLED NEAR-FIELD COMMUNICATION-LINK CONNECTOR-REPLACEMENT CHIPS

Abstract: Tightly-coupled near-field transmitter/receiver pairs are deployed such that the transmitter is disposed at a terminal portion of a first conduction path, the receiver is disposed at a terminal portion of a second conduction path, the transmitter and receiver are disposed in close proximity to each other, and the first conduction path and the second conduction path are discontinuous with respect to each other. In some embodiments of the present invention, close proximity refers to the transmitter antenna and the receiver antenna being spaced apart by a distance such that, at wavelengths of the transmitter carrier frequency, near-field coupling is obtained. In some embodiments, the transmitter and receiver are disposed on separate substrates that are moveable relative to each other. In alternative embodiments, the transmitter and receiver are disposed on the same substrate.

Classifications:

International (IPC 8-9): F01C1/348 F01C1/356 F01C1/40 F01C21/08

F01C21/10 F03C2/30 F03C4/00 F04C18/00 F04C18/40 F04C2/00

F04C2/348 F04C2/356 F04C2/40 G01D5/12 G01R27/26 G01S11/02

G01S13/04 G01S13/08 G06F1/16 G06F1/18 G06F13/00 G06F13/40

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G06K19/07 G06K19/077 G09G3/20 G09G5/00 H01F38/14 H01F7/02

H01L23/00 H01L23/12 H01L23/31 H01L23/495 H01L23/498

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H01Q1/12 H01Q1/22 H01Q1/24 H01Q1/38 H01Q1/48 H01Q1/50

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H04W52/02 H04W76/02 H04W76/04 H04W8/00 H04W8/08 H05K1/02

H05K9/00 (Advanced/Invention);

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H04B1/38 H04B1/40 H04B5/00 H04L7/00

H05K1/02 (Advanced/Non-invention);

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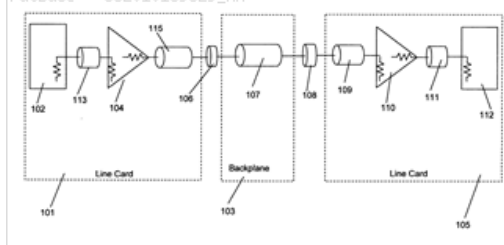
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KEYSSA INC CAMPELL

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Inventor(s): BURNS SR ; ROGER D ; WOLCOTT JOHN CAMPBELL ; KYLES IAN A CAMPBELL ; MCCORMACK GARY D CAMPBELL ; ISAAC ROGER CAMPBELL

Agent(s): GRIFFITH HACK; BORDEN LADNER GERVAIS LLP; BEETZ AND PARTNER MBB PATENT U RECHTSANWAELTE; SPLANEMANN PATENTANWAELTE PARTNERSCHAFT MBB; STAINTHORPE VANESSA JULIET; HOEFER AND PARTNER; COLOMBO STEFANO PAOLO; MORRALL JONATHAN IAN MCLACHLAN; BOULT WADE TENNANT; RAYMOND J WERNER; KOLISCH HARTWELL PC; FENWICK AND WEST LLP; VAN COURT AND ALDRIDGE LLP; FENWICK AND WEST; MICHAEL BEST AND FRIEDRICH LLP; COOPER DAVID P; LINDEN GERALD E; VAN COURT ANDREW ET AL; PATEL RAJIV P ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: ON-LINE WEB ACCESSED ENERGY METER

Abstract: An electrical metering system capable of performing multiple metering functions, collecting **data**, and wirelessly provides the collected metering **data** to a utility operator. In the electrical metering system, at least one computing device for initiating a request for **data**. A first modem connects the computing device to an infrastructure. A wireless embedded modem for wirelessly connects an electric meter to an infrastructure, and the wireless electric meter receives a request from the computing device and wirelessly transmits the metering **data** to the computing device, thereby initiating the request.

Classifications:

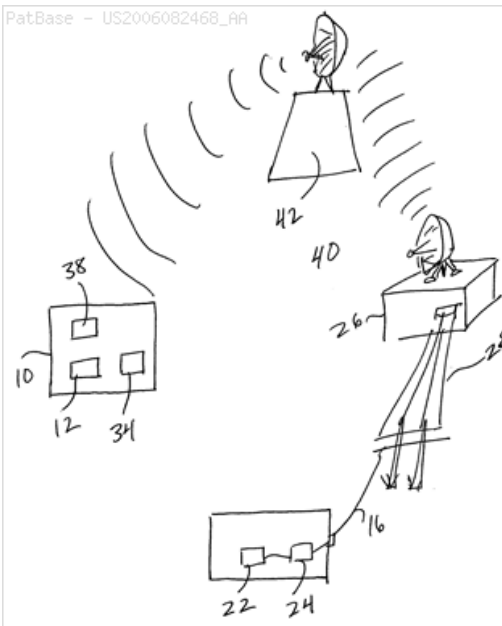
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CPC: G01R21/1331 Y04S20/46 H03M1/0682 H03M1/12 G01R19/0084 G01R15/04 G01R35/005 H04L43/0876 H04L63/029 G06F17/00 G01R23/20 G01R15/08 G06F11/30 G01R13/00 G01R19/2509 G01R19/00 G01R21/133 G06F17/30569 G01R21/00 G01R35/00 G06F17/30067 G06F17/30864 G06F7/76 G06F3/04847 H04B3/542 H04L43/08 H04L67/02 H04L69/03 H04L63/0823 G06F21/12 G06F21/14 G06F2221/0704 G06F17/30899 G06F17/30091 G06F3/0613 G06F17/30227 G06F17/30368 G06F17/30575 G06F17/30218 G06F17/30076 G06F3/0688 G06F3/0655 G06F3/0619 Y02B90/246 Y04S20/42 H04L63/0876 H04L63/166 H04L67/28 G06F21/572 G06F8/65 G06F21/602 Y02B90/241 Y02B90/243 Y04S20/32 Y04S20/325 H04L12/2816 G05B19/042 G05B2219/2642 G01D18/008 G01R22/06 G01R22/065 H05K7/1424 G01D4/004 G01R1/025 G01R22/063 G06Q50/06 H04L63/0435 H04L67/06 H04L67/12 Y02B90/242 Y04S20/322 Y04S40/24 G01R1/40 G01R19/04 G01R19/2513 G01R29/02 G01D4/002 G06Q10/06 H04L51/02 G06F17/40 G06F19/00 H04L51/36 H04W4/38 G01R22/10 G01R22/00

European: G01D4/00R G01D4/00R1 G01R11/04 G01R19/25D G01R21/133B G01R22/06D2 G01R22/10 G06Q50/06 H03M1/06M9D2N H05K7/14F5 S01R19/04 S01R19/25D S01R22/06 S01R22/10 S01R29/02 T03M1/12 Y02B90/24B2 Y04S20/30 Y04S20/32B Y04S20/46

US: 1/1 323/209 324/102 324/103.00R 324/103.00RS 324/103R 324/113 324/115 324/115S 324/120 324/120P 324/123.00RP 324/123R 324/140.00R 324/140R 324/142 324/500 324/510 324/72 324/74 324/76.11 324/76.110P 324/76.110S 324/76.38 324/76.39 324/99D 327/50 330/252 340/500 340/635 340/652 340/657 340/659 340/660 340/662 340/870.02 340/870.020P 340/870.020S 340/870.03 340/870.05 341/155 341/155P 341/156 345/440 345/440S 361/1 361/196 361/35 361/56 361/57 361/603 361/62 361/668 361/673 361/736 361/79 361/84 361/86 361/88 361/94 361/97 370/252 370/252P 370/401 379/106.03 379/106.03S 455/426.1 455/426.100S 455/445 700/22 700/286 700/291 700/292 700/293 702/107 702/107S 702/187 702/187S 702/188 702/188S 702/189 702/57 702/58 702/60 702/60P 702/61 702/61P 702/61S 702/62 702/62P 702/63 702/64 702/64P 702/65 702/66 702/66S 702/69 702/70 702/72 702/79 702/85 705/412 705/416 707/100 707/648 707/812 707/821 707/821P 707/999.1 707/999.100S 707/E17.01 707/E17.010S 707/E17.044 707/E17.044S 708/105 708/200 708/207 709/213 709/218 709/219 709/219P 709/224 711/103 711/170 713/151 713/156 713/189 713/191 715/771 731/1.01 73/865.8 73/865.9

PatBase - US2006082468_AA



Family:

Publication number	Publication date	Application number	Application date
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Priority:

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Assignee(s): (std): BANHEGYESI TIBOR ; BANKER PATRICIA E ; ELECTRIC IND GAUGE TECH ; ELECTRO IND GAUGETECH ; KAGAN ERRAN ; KAGAN ANDREW ; ZHU HAI ; WANG WEI ; SIQUEIRA DA SILVA DULCIANE ; SPANIER JOSEPH ; SLOTA FREDERICK B ; WERNER ANDREW J ; TECH ELECTRO IND GAUGE ; KOVAL RORY A ; ELECTRO IND GAUGE TECH

Assignee(s): ELECTRO INDUSTRIES GAUGE TECH ; ELECTRO INDUSTRIES GAUGETECH ; ELECTRO IND AND GAUGE TECH ; ELECTRO IND

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Agent(s): DILWORTH AND BARRESE LLP; CASELLA AND HESPOS; ELECTRO IND GAUGETECH C O CASELLA AND HESPOS LLP; ELECTRO INDUSTRIES/ GAUGETECH,C/O HESPOS AND PORCO LLP; ELECTRO IND GAUGETECH C O HESPOS AND PORCO LLP; GERALD E HESPOS ESQ HESPOS AND PORCO LLP; GERALD E; ANTHONY J; HESPOS GERALD E; CASELLA ANTHONY J; PORCO MICHAEL J; MICHAEL J; GERLAD E; MATTHEW T

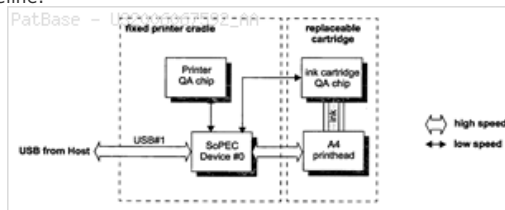
Title: CONFIGURABLE IMAGE PROCESSOR

Abstract: An image processor, including: memory; a plurality of processing modules; and a general purpose processor; the image processor being configurable into: a first mode, in which at least some of the modules form a processing pipeline for processing image **data**; a second mode, in which the general purpose processor processes **data** output by, or **supplies** processed **data** to, at least one of the processing modules in the pipeline.

Classifications:**International (IPC 8-9):** B41J2/165 B41J29/38

G06F7/00 (Advanced/Invention);

B41J2/165 B41J29/38 G06F7/00 (Core/Invention)

CPC: G06K15/1857 G06K15/102 B41J2/2139 G06K2215/0085**European:** B41J2/21D2 G06K15/10B S06K215/00D2**US:** 347/14 347/14P 347/19 347/5 347/9 382/303 382/303P**Family:**

Publication number	Publication date	Application number	Application date
US2006067592 AA	20060330	US20040934628	20040907
US2006164454 AA	20060727	US20040854521	20040527
US2008122883 AA	20080529	US20070961940	20071220
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US7980647 BB	20110719	US20090483241	20090612

Priority:

US20040854521 20040527

US20040934628 20040907

US20070961940 20071220

US20090483241 20090612

Probable Assignee: MEMJET TECHNOLOGY LTD**Assignee(s):** (std): HORSBURGH BRUCE M ; SILVERBROOK RES PTY LTD ; WALMSLEY SIMON R ; WEBB MICHAEL J**Assignee(s):** ZAMTEC LTD ; SILVERBROOK RESEARCH PTY LTD ; MEMJET TECHNOLOGY LTD**Inventor(s):** (std): HORSBURGH BRUCE M ; JACKSON PULVER MARK ; PLUNKETT RICHARD T ; PLUNKETT RICHARD THOMAS ; PULVER MARK J ; PULVER MARK JACKSON ; SHEAHAN JOHN R ; SHEAHAN JOHN ROBERT ; SILVERBROOK KIA ; WALMSLEY SIMON R ; WALMSLEY SIMON ROBERT ; WEBB MICHAEL J ; WEBB MICHAEL JOHN**Inventor(s):** WEBB MICHAEL ; WALMSLEY SIMON ; SHEAHAN JOHN ; PULVER MARK ; PLUNKETT RICHARD ; HORSBURGH BRUCE MERVYN ; HORSBURGH BRUCE**Agent(s):** SILVERBROOK RESEARCH PTY LTD

Title: CARTRIDGE HAVING INTEGRATED CIRCUIT FOR ENABLING VALIDATION THEREOF BY A MOBILE DEVICE

Abstract: A replaceable print cartridge for installation in a mobile device, the print cartridge comprising: a printhead; at least one ink reservoir; and a first integrated circuit that permanently stores an identifier that is relatively unique to that integrated circuit; such that, upon installation in the mobile device, the mobile device is able to determine the identifier.

Classifications:

International (ipc 8-9): B41J2/165 B41J2/175 B41J29/393

G06F13/28 G06K7/10 G06K7/12 H04L9/32

H04M1/00 (Advanced/Invention);

B41J2/165 B41J2/175 G06F13/20 H04L9/32 (Core/Invention)

International (ipc 1-7): B41J2/165

CPC: B41J2/17546

European: B41J2/175C7E

US: 235/462.42 235/472.01 235/472.010P 347/107 347/19 347/86
347/86P 380/259 380/283 380/44 455/556.1 455/556.100P 713/161
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PatBase - US2005264622_A1

Patent Application Publication Dec. 1, 2005 Sheet 1 of 58 US 2005/0264622 A1

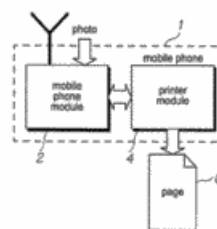


FIG. 1

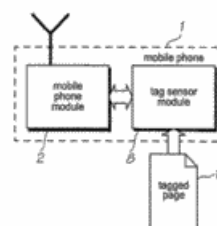


FIG. 2

Family:

Publication number	Publication date	Application number	Application date
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Priority:

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US20100778122 20100512 US20100817185 20100617

Probable Assignee: SILVERBROOK RESEARCH PTY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): SILVERBROOK KIA ; WALMSLEY SIMON R ; WALMSLEY SIMON ROBERT

Inventor(s): WALMSLEY SIMON

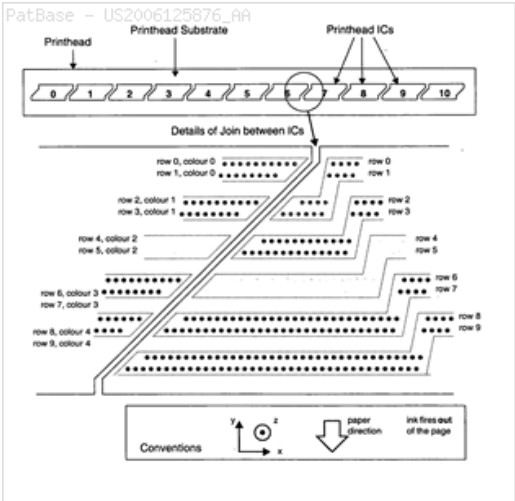
Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: PRINTER COMPRISING TWO UNEVEN PRINthead MODULES AND AT LEAST TWO PRINTER CONTROLLERS, ONE OF WHICH SENDS PRINT DATA TO BOTH OF THE PRINthead MODULES

Abstract: A printer comprising: a printhead comprising first and second elongate printhead modules, the printhead modules being parallel to each other and being disposed end to end on either side of a join region, wherein the first printhead module is longer than the second printhead module; at least first and second printer controllers configured to receive print data and process the print data to output dot data to the printhead, wherein: the first printer controller outputs dot data to both the first printhead module and the second printhead module; and the second printer controller outputs dot data only to the second printhead module.

Classifications:

International (IPC 8-9): B41J2/145 B41J2/15 B41J29/38 G06F15/00 (Advanced/Invention);
B41J2/145 B41J29/38 G06F15/00 (Core/Invention)
CPC: B41J2/145
European: B41J2/145
US: 347/40 347/48 347/49 347/5 347/50 347/58 358/1.9 358/1.900P



Family:

Publication number	Publication date	Application number	Application date
US2006125876 AA	20060615	US20040854510	20040527
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Priority:

US20040854510 20040527 US20070706295 20070215 US20080202308 20080831

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): WEBB MICHAEL JOHN ; WEBB MICHAEL J ; WALMSLEY SIMON ROBERT ; WALMSLEY SIMON R ; SILVERBROOK KIA ; SHEAHAN JOHN ROBERT ; SHEAHAN JOHN R ; PULVER MARK JACKSON ; PULVER MARK J ; PLUNKETT RICHARD THOMAS ; PLUNKETT RICHARD T ; JACKSON PULVER MARK

Inventor(s): PLUNKETT RICHARD ; PULVER MARK ; SHEAHAN JOHN ; WALMSLEY SIMON ; WEBB MICHAEL

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: SYSTEMS AND METHODS FOR PROCESSING INFRARED IMAGES

Abstract: One or more embodiments of the invention provide a system and method for processing an infrared image to receive infrared image **data** of a non-uniform scene, apply column noise filter correction to the infrared image **data**, and/or apply row noise filter correction to the infrared image **data**, and provide corrected infrared image **data** based on the column and/or row noise filter correction as infrared output image **data**.

Classifications:

International (IPC 8-9): A61B5/01 A61B5/087 B60Q1/00 B60R11/04

G01J5/00 G01J5/02 G01J5/04 G01J5/06 G01J5/08 G01J5/10
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G01V8/10 G05D1/00 G06F1/14 G06F11/07 G06K9/00 G06K9/40
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H04N5/374 H04N5/376 H04N5/378 H04N7/18 H04N9/04

H05B37/02 (Advanced/Invention);

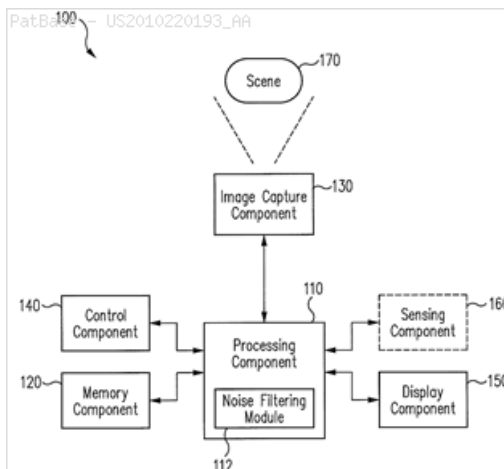
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H04N5/365 (Advanced/Non-invention);
G06K9/40 H04N5/217 H04N5/33 (Core/Invention)

CPC: G06K9/00785 G06K9/2018 H04N1/2137 G06T1/20 G01V8/10
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European: H04N5/33 H04N5/365A3

US: 1/1 250/349 315/149 348/143 348/148 348/164 348/164P 348/165 348/47 348/82 348/E.09 348/E50.90S 382/103
382/218 382/260 382/260S 382/263 382/264 438/66 438/67 701/2 713/502 713/503 D14/433

Locarno class: 14/02

**Family:**

Publication number	Publication date	Application number	Application date
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Agent(s): GOWLING LAFLEUR HENDERSON LLP; KITZLER MICHAEL; HAYNES AND BOONE LLP IP SECTION; HAYNES AND BOONE LLP; HYNES AND BOONE LLP; MICHELSON GREG J; FOLSOM BRENT A; MICHELSON GREGORY J

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: USE OF VARIANT AND BASE KEYS WITH THREE OR MORE ENTITIES

Abstract: A first entity including: a first bit-pattern a non-volatile memory storing resource **data**, a first base key for use with at least a first variant key; a second variant key for use with a second base key, the second variant key being the result of a one way function applied to: the second base key; and the first bit-pattern or a modified bit-pattern based on the first bit-pattern.

Classifications:

International (IPC 8-9): G06F15/00 G06F3/12

G06K15/00 (Advanced/Invention);

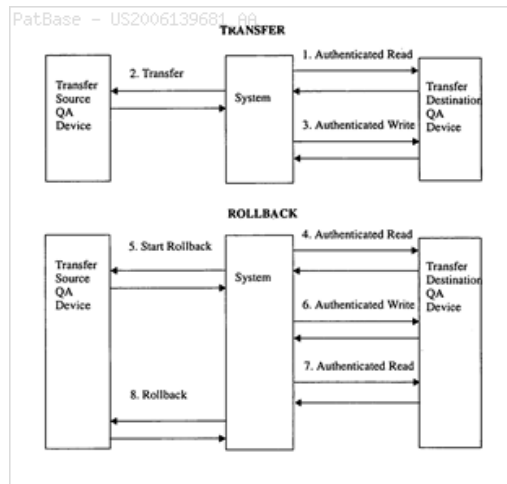
G06F11/30 H04L9/00 (Advanced/Non-invention);

G06F15/00 G06F3/12 (Core/Invention)

CPC: G06F21/445 G06F21/606

European: G06F21/44A G06F21/60C

US: 358/1.14 358/1.140P 358/1.15 358/1.150P 358/1.9 380/268 380/285 713/193



Family:

Publication number	Publication date	Application number	Application date
US2006139681 AA	20060629	US20040854519	20040527
US2009213427 AA	20090827	US20090436133	20090506
US2009268246 AA	20091029	US20090501457	20090712
US7557941 BB	20090707	US20040854519	20040527
US7986439 BB	20110726	US20090436133	20090506

Priority:

US20040854519 20040527 US20090436133 20090506 US20090501457 20090712

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): WALMSLEY SIMON R ; WALMSLEY SIMON ROBERT

Inventor(s): WALMSLEY SIMON

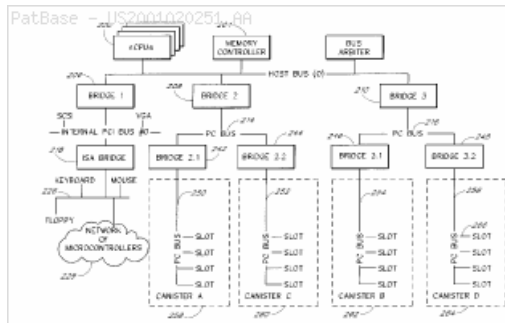
Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: SYSTEM ARCHITECTURE FOR REMOTE ACCESS AND CONTROL OF ENVIRONMENTAL MANAGEMENT

Abstract: A fault tolerant system by which individual components of a server are monitored and controlled through independent, programmable microcontrollers interconnected through a microcontroller network. An external agent can control and monitor the microcontrollers by extending the interconnection network beyond the physical server. The extension to the interconnection network **converts** protocols between media, and directs the microcontrollers and the state managed by the microcontrollers. Intervention of the server operating system software is not required and is not utilized for the access and control operations. A remote interface board provides the interface between the microcontroller network and an external modem that communicates with a remote client computer. The remote interface board also provides for connection to a local client computer.

Classifications:

International (ipc 8-9): F16D3/227 G05D23/00 G06F1/00 G06F1/20 G06F1/26 G06F11/00 G06F11/07 G06F11/16 G06F11/20 G06F11/22 G06F11/273 G06F11/30 G06F11/32 G06F11/34 G06F13/00 G06F13/38 G06F13/40 G06F21/00 G06F21/30 G06F21/31 G06F9/44 G06F9/445 G06F9/46 H02P7/285 H04L12/12 H04L12/24 H04L12/26 H04L12/28 H04L12/40 H04L12/56 H04L12/06 H04L29/08 H04L29/12 H04L29/14 H05K5/00 H05K7/20 (Advanced/Invention); G06F1/00 G06F11/20 G06F11/22 G06F11/32 G06F3/06 H04L12/24 H04L29/08 (Advanced/Non-invention); G06F1/00 G06F11/20 G06F11/26 G06F11/00 G06F11/07 G06F11/16 G06F11/20 G06F11/273 G06F11/30 G06F11/32 G06F11/34 G06F13/38 G06F13/40 G06F21/00 G06F9/445 G06F9/46 H02P7/18 H04L12/12 H04L12/24 H04L12/26 H04L12/40 H04L12/56 H04L29/06 H04L29/08 H04L29/12 H04L29/14 H05K7/20 (Core/Invention); G06F1/00 G06F11/22 G06F3/06 H04L29/08 (Core/Non-invention)



International (ipc 1-7): C06F13/00 E06F13/00 F04B41/06 G01R31/08 G05D23/00 G06F1/00 G06F1/16 G06F1/24 G06F1/26 G06F11/00 G06F11/30 G06F11/32 G06F11/00 G06F11/07 G06F11/10 G06F11/16 G06F11/30 G06F11/34 G06F13/00 G06F13/14 G06F13/36 G06F13/38 G06F13/40 G06F15/16 G06F15/163 G06F9/445 G06Z13/10 H01H35/00 H02H3/05 H02H3/05 H03K19/003 H03K19/003 H04B1/74 H04L1/00 H04L1/22 H05K5/00 H05K7/20 **CPC:** G06F11/3068 G06F11/327 H04L12/2856 H04L12/2898 G06F11/079 G06F13/4068 G06F2213/0024 H04L1/069 H04L67/1002 H04L67/1095 H04L69/40 G06F13/409 H04L49/9073 H05K7/1492 H05K7/207 H05K7/20736 G06F11/2005 G06F11/2007 G06F11/2012 H04L29/12009 H04L61/00 H04L2029/06054 H04L47/125 G06F11/2002 G06F11/2017 H04L41/08 G06F9/4413 H04L49/9057 G06F11/3089 G06F11/1482 G06F11/2089 G06F2201/85 H04L12/4013 H04L41/0668 G06F11/0745 G06F11/1658 G06F11/2023 G06F11/2035 H04L41/0663 G06F11/0709 G06F11/0757 G06F11/3048 H04L43/0805 G06F11/203 G06F11/2038 H04L29/12047 H04L61/15 H04L29/06 G06F11/20 H04L12/40195 H04L29/12839 H04L45/58 H04L61/6022 G06F11/1443 H04L12/40032 H04L41/042 H04L41/0886 H04L2012/40215 G06F11/3013 H04L49/9063 F04D27/004 F04D25/166 H05K7/2072 G06F11/3093 G06F11/3072 H05K7/20209 H04L41/0826 H04L41/0836 Y10T307/766 Y10T307/832 Y10T307/858 Y10T307/937 F04D29/601 G06F11/0784 G06F11/2015 G06F11/2736 H02P7/285 H04L43/06 G06F11/324 H04L3/50 G06F11/0775 H04L41/0654 H04L41/0681 H04L41/0816 H04L49/901 G06F13/385 G06F11/30 G06F11/3034 G06F11/328 G06F11/0751 G06F11/2268 H04L43/10 H04L41/06 G06F11/2294 G06F11/3476 G06F11/3495 H04L43/0811 H04L47/621 H04L49/90 G06F9/44521 G06F11/0772 G06F11/3024 G06F11/3027 G06F11/3031 G06F11/3044 G06F11/3055 H05K7/20836 H04L41/0659 H04L43/00 Y02D50/40 Y02D50/30 Y02D10/14 Y02D10/151 Y02D10/16 Y02D10/34 Y02D50/20 H04L41/0806 H04L41/0843 H04L41/0856 H04L41/0869 H04L41/0809 H04L41/0803 H04L41/0866 H04L43/16 G06F1/206 G06F11/0787 G06F11/3058 G06F11/3466 G06F11/349 G06F2201/835 H04L12/403 G06F9/547 G06F11/0769 H04L12/40071 H04L12/413 H04L43/045 H04L43/065 H04L43/0817 H04L43/0823 H04L43/106 H04L41/12 G06F1/20 G06F1/26 G06F3/0601 G06F9/4411 G06F11/0748 G06F11/0766 G06F11/0793 G06F11/3006 G06F11/3041 G06F11/3051 G06F11/3065 G06F13/4027 G06F13/4081 G06F21/305 G06F21/31 G06F2003/0692 G06F2201/86 H04L12/12 H04L12/40169 H04L41/0213 H04L41/082 H04L41/22

European: F16D3/227 G06F1/00N5A2 G06F1/20 G06F1/20T G06F1/26 G06F11/07P1A G06F11/07P1K G06F11/07P1L G06F11/07P2 G06F11/07P4 G06F11/07P4A G06F11/07P4B G06F11/07P4C G06F11/07P4F G06F11/07P4G G06F11/07P6 G06F11/14A8T G06F11/14S1 G06F11/16D G06F11/20 G06F11/20C2 G06F11/20C4 G06F11/20M G06F11/20P12 G06F11/20P2 G06F11/20P2M G06F11/20P2S G06F11/20P4 G06F11/20P6 G06F11/20U G06F11/22R G06F11/273S G06F11/30A1 G06F11/30A11 G06F11/30A12 G06F11/30A13 G06F11/30A3 G06F11/30A6 G06F11/30A7 G06F11/30A8 G06F11/30A9 G06F11/30C G06F11/30D G06F11/30E G06F11/30R G06F11/30R1 G06F11/30R2 G06F11/30S G06F11/30S1 G06F11/32S G06F11/32S6 G06F11/34T G06F11/34T10 G06F11/34T4 G06F13/38A2 G06F13/40D5 G06F13/40E2 G06F13/40E2H G06F13/40E4 G06F21/30A G06F21/31 G06F9/445L G06F9/444A G06F9/444A4 G06F9/54P H02P7/285 H04L12/12 H04L12/24B1 H04L12/24C2 H04L12/24D H04L12/24D2 H04L12/24D3 H04L12/24E1 H04L12/24E1A H04L12/24E1A1 H04L12/24E1B1 H04L12/24E1B2 H04L12/24E1C1 H04L12/24E4B H04L12/24E5 H04L12/24E5A H04L12/24F3 H04L12/26M H04L12/26M2B2 H04L12/26M3A2 H04L12/26M4 H04L12/26M4B H04L12/26M7 T04L12/40M T04L12/40S1 T04L29/06C8A T04L29/08N9A T04L29/12A H04L29/12A2 H04L29/12A9D11 H04L29/14 H04L41/04A H04L41/06 H04L41/06C1A H04L41/06C2 H04L41/08A H04L41/08A1 H04L41/08A1A H04L41/08A2A H04L41/08A2B H04L41/08A4A H04L41/08B2 H04L41/08C H04L41/08C1 H04L41/12 H04L41/22 H04L43/00 H04L43/06B H04L43/08C H04L43/08D H04L43/10 H04L43/10B H04L43/50 H04L45/58 H04L47/12B H04L47/62B H04L49/90 H04L49/90C H04L49/90P H04L49/90Q H04L49/90Q1A H04L61/00 H04L61/15 H04L61/60D11 H05K7/14S4F H05K7/20B90 H05K7/20R90 H05K7/20S10B H05K7/20S10C H05K7/20S90 S06F11/07P10 S06F11/07P2 S06F11/07P2A1 S06F11/20C S06F11/20C2 S06F11/20C6 S06F11/20K S06F11/20P12 S06F11/20P2S S06F11/20P4 S06F11/20S4 S06F11/20U S06F11/22L S06F11/22R S06F11/30 S06F11/30E S06F11/32S4 S06F11/34T12 S06F11/34T4 S06F201/835 S06F201/850 S06F201/860 S06F213/0024 S06F3/06A S06F3/06D T04L12/24A2 T04L12/24D T04L12/24E T04L12/24E1A T04L12/24E1A1 T04L12/24E1B1 T04L12/24E1B2 T04L12/24E1B3A T04L12/24E1B3D T04L12/24E5 T04L12/24E6C T04L12/24F3 T04L12/26M2A T04L12/26M2B T04L12/26M2B2 T04L12/26M3A T04L12/26M3A1 T04L12/26M3A2 T04L12/26M3B T04L12/26M4 T04L12/26M4B T04L12/26M7 T04L12/40M T04L12/40S1 T04L29/06C8A T04L29/08N9A T04L41/02B T04L41/06 T04L41/06C T04L41/06C1 T04L41/06E T04L41/08 T04L41/08A1 T04L41/08A1A T04L41/08A2A T04L41/08A2B T04L41/08A3A T04L41/08A3D T04L41/08C T04L41/08D T04L41/22 T04L43/04A T04L43/06 T04L43/06B T04L43/08C T04L43/08D T04L43/08E T04L43/10 T04L43/10B T04L43/16 T05K999/99 Y02B60/12H Y02B60/12J2 Y02B60/12L Y02B60/32 Y02B60/33 Y02B60/34

US: 1/1 165/80.3 236/1.00E 236/1E 307/116 307/126 307/130 307/139 360/5 361/679.4 361/679.41 361/686 361/695 361/731 370/216 370/217 370/254 370/409 388/827 388/840 392/283 395/182.03 395/281 395/282 395/283 395/284 395/822 395/828 395/837 395/838 395/866 395/882 395/892 395/893 4/10 4/11 4/3 417/3 417/42 417/45 700/299 700/300 702/132 702D11 187 709/187 709/203 709/203 709/208 709/208 709/217 709/223 709/224 709/224P 709/224S 709/225 709/235 709/239 709/300 710/10 710/10 710/100 710/100.104 710/101 710/102 710/103 710/104 710/126 710/128 710/129 710/130 710/131 710/135 710/17 710/18 710/19 710/2 710/260 710/300 710/301 710/302 710/302P 710/305 710/305P 710/306 710/306P 710/310 710/312 710/313 710/314 710/362 710/46 710/5 710/52 710/53 710/62 710/72 710/72.4 710/73 710/74 710/8 711/145 713/1 713/100 713/100S 713/2 713/300 713/310 713/320 713/324 713/330 713/340 713/400 714/1 714/10 714/11 714/13 714/13P 714/13S 714/14 714/23 714/24 714/25 714/25P 714/3 714/30 714/31 714/32 714/37 714/38 714/38.13 714/39 714/4 714/4.1 714/4.100S 714/4.11 714/4.12 714/4.120P 714/4.4 714/4.5 714/4.500P 714/42 714/43 714/44 714/46 714/47 714/47.2 714/47.200P 714/47.3 714/47P 714/48 714/48P 714/4P 714/4S 714/5 714/5.1 714/5.11 714/51 714/57 714/7 714/7P 714/E11.007 714/E11.007S 714/E11.008 714/E11.008S 714/E11.015 714/E11.015S 714/E11.024 714/E11.025 714/E11.025S 714/E11.026 714/E11.067 714/E11.071 714/E11.073 714/E11.073S 714/E11.078 714/E11.08 714/E11.094 714/E11.094S 714/E11.173 714/E11.173S 714/E11.174 714/E11.174S 714/E11.179 714/E11.179S 714/E11.184 714/E11.188 714/E11.188S 714/E11.2 714/E11.200S 714/E11.201 714/E11.204 715/5 718/105 719/310

Family:

Publication number	Publication date	Application number	Application date
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US2001020251 AA	20010906	US20010815596	20010323
US2001052042 AA	20011213	US20010885597	20010619
US2001056554 AA	20011227	US20010879587	20010611
US2002042896 AA	20020411	US20010911884	20010723
US2003009613 AA	20030109	US20010016296	20011030
US2003126496 AA	20030703	US20020287554	20021101
US2004153786 AA	20040805	US20030675917	20030929
US2004210701 AA	20041021	US20040808220	20040323
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US2010146346 AA	20100610	US20090640681	20091217
US2013073110 AA	20130321	US20120620275	20120914
US2014115404 AA	20140424	US20130059348	20131021
US5892928 A	19990406	US19970943072	19971001
US5962933 A	19991005	US19970942216	19971001
US5987554 A	19991116	US19970942413	19971001
US5990582 A	19991123	US19970942447	19971001
US6052733 A	20000418	US19970940302	19971001
US6073255 A	20000606	US19970942068	19971001
US6105151 A	20000815	US19970942407	19971001
US6122746 A	20000919	US19970943076	19971001
US6122758 A	20000919	US19970942222	19971001
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US6138250 A	20001024	US19970942070	19971001
US6145098 A	20001107	US19970942347	19971001
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US9348722 BB	20160524	US20130059348	20131021

Priority:

US19970046311P 19970513	US19970046312P 19970513	US19970046326P 19970513
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Probable Assignee: MEI CALIFORNIA INC

Assignee(s): (std): AGNETA DON ; AMAD AHL CARLTON G ; AMDAHL CARLTON G ; JOHNSON KARL S ; CHRABASZCZ MICHAEL ; HENDERSON MICHAEL G ; FINDLAY BRUCE ; SHEIKH TAHIR Q ; NGUYEN KEN ; WALLACH WALTER A ; REED JOHN M ; PAPA STEPHEN E J ; SCHIRO DON ; SMITH DENNIS H ; MICRON ELECTRONICS INC ; MICRON TECHNOLOGY INC ; 3COM CORP ; PAPA STEPHEN E ; ROUND ROCK RES LLC

Assignee(s): US BANK NATIONAL ASSOCIATION COLLATERAL AGENT AS ; MORGAN STANLEY SENIOR FUNDING INC COLLATERAL AGENT AS ; ROUND ROCK RESEARCH LLC ; HEWLETT PACKARD ENTERPRISE DEVELOPMENT LP ; PAPA STEPHEN EJ ; MICON ELECTRONICS INC ; MICRON ELECTRONICS ; MEI CALIFORNIA INC ; KHALILI MEHRDAD ; MAHALINGAM MALLIKARJUNAN ; HEWLETT PACKARD CO ; HEWLETT PACKARD DEVELOPMENT CO LP

Inventor(s): (std): HENDERSON MICHAEL G ; JOHNSON KARL ; JOHNSON KARL S ; KHALILI MEHRDAD ; LIU JI HWAN ; MAHALINGAM MALLIKARJUNAN ; MAHALINGHAM MALLIKARJUNAN ; NGUYEN KEN ; NOURI AHMAD ; AMDAHL CARLTON G ; CHRABASZCZ MICHAEL ; FINDLAY BRUCE ; AGNETA DON ; AGNETA DON A ; PAPA STEPHEN E ; PAPA STEPHEN E J ; PELLICER THOMAS J ; REED JOHN M ; SCHIRO DON ; SHEIKH TAHIR Q ; SMITH DENNIS H ; WALLACH WALTER A ; WALLACH WALTER AUGUST ; AMAD AHL CARLTON G

Inventor(s): WALLACH WALTER ; SMITH DENNIS ; PAPA STEPHEN EJ ; AMDAHL CARLTON ; HENDERSON MICHAEL ; PAPA STEPHEN

Agent(s): KNOBBE MARTENS OLSON AND BEAR LLP ; GAZDZINSKI AND ASSOCIATES PC

Title: **DATA** INTERFACE FOR HARDWARE OBJECTS

Abstract: Embodiments of the invention include a system for an integrated circuit development. Elements of the development system include hardware and software objects. These objects can be instantiated, ordered, parameterized, and connected in a software environment to implement different functions. Once in software, the description defines the topology and the properties of a set of objects and hence the overall function. These objects are hierarchically composed from a set of primitive objects. By using a piece of hardware that can model any primitive object set as pre-established encapsulated hardware objects, the topology and properties define a piece of hardware that can perform the desired, implemented, functions. Using embodiments of the invention, circuit designers can design hardware systems with little or no knowledge of hardware or hardware design, requiring only a high-level software description.

Classifications:

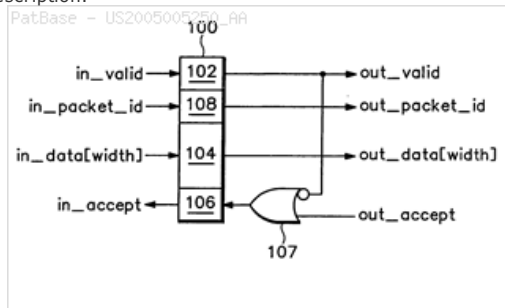
International (IPC 8-9): G01F1/12 G01R31/00 G01R31/08 G06F1/04 G06F1/08 G06F11/00 G06F13/14 G06F13/40 G06F15/00 G06F15/16 G06F15/17 G06F15/80 G06F17/50 G06F19/00 G06F3/00 G06F5/00 G06F5/06 G06F5/08 G06F9/00 G06F9/40 G06F9/45 H04B17/00 H04B3/32 H04B3/46 H04L12/28 H04L12/403 H04L12/64 H04L25/00 H04L25/40 H04L29/00 H04L7/00 H04N17/00 H04N7/16 H04N7/173 (Advanced/Invention); G01R31/08 G06F17/50 (Advanced/Non-invention); G01F1/05 G01R31/08 G06F1/08 G06F11/00 G06F13/40 G06F15/00 G06F15/16 G06F15/76 G06F17/50 G06F9/00 G06F9/40 G06F9/45 H04B17/00 H04B3/46 H04L12/28 H04L25/00 H04L25/40 H04L7/00 H04N17/00 (Core/Invention); G06F (Subclass/Invention)

International (IPC 1-7): G06F17/50 G06F5/06

CPC: H04L7/02 H04L12/40019 G06F11/3656 G06F11/362 G06F1/12 G06F17/5045 G01R31/025 G06F15/17337 G06F1/04 G06F1/10 H04L7/0008 G06F15/16 G06F9/30189 G06F9/30076 G06F15/7842 G06F15/8007 G06F9/30054 G06F9/30181 G06F9/3802 G06F9/3877 G06F9/3885 G06F9/3891 H04N17/00 G01R31/001 G01R31/083 H04B3/32 H04L29/00 G06F13/4022 G06F13/4059

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US: 326/38 326/39 326/93 370/230 370/235 370/419 370/431 370/431P 370/450 375/356 375/356P 702/189 702/189P 702/59 702/59P 709/250 709/250P 710/34 710/52 710/55 712/1 712/15 712/15P 712/200 712/201 712/201P 712/32 712/E9.033 712/E90.33S 713/100 713/100P 713/400 713/401 713/500 713/501 713/502 713/600 714/10 714/30 714/31 714/34 714/34P 714/37 714/45 714/45P 714/47 714/47.1 714/798 714/E11.207 714/E11.207S 716/1 716/100 716/100P 716/102 716/102P 716/104 716/104S 716/108 716/113 716/117 716/117S 716/119 716/126 716/126S 716/139 716/16 716/18 717/136 717/136P 725/107 725/149



Family:

Publication number	Publication date	Application number	Application date
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Priority:

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Probable Assignee: METAGENCE TECHNOLOGIES LTD

Assignee(s): (std): AMBRIC INC ; BUTTS MICHAEL R ; JONES ANTHONY MARK ; JONES ANTHONY M ; KOSCHORECK KEVIN M ; TRILITHIC INC ; NETHRA IMAGING INC ; STELLE IV RALEIGH BENTON ; WASSON PAUL M ; WHITE EDMUND H

Assignee(s): STELLE RALEIGH BENTON IV ; METAGENCE TECHNOLOGIES LTD ; VIAVI SOLUTIONS INC ; SILICON VALLEY BANK ; IMAGINATION TECHNOLOGIES LTD ; AMBRIC INC150 - 15655 SW GREYSTONE COURTBEAVERTONOR97006-6007US ; ARM LTD

Inventor(s): (std): JONES ANTHONY M ; JONES ANTHONY MARK WASSON PAUL ; KOSCHORECK KEVIN M ; STELLE RALEIGH BENTON ; STELLE RALEIGH BENTON IV ; WASSON PAUL M ; STELLE IV RALEIGH BENTON ; JONES ANTHONY MARK ; BUTTS MICHAEL R ; WHITE EDMUND H

Inventor(s): ASSON PAUL M ; WASSON PAUL ; WASSON PAUL MUS ; WHITE EDMUND ; PAUL M WASSON ; ANTHONY MARK JONES ; BUTTS MICHAEL ; JONES ANTHONY ; JONES ANTHONY MARK WASSON PAUL M ; JONES ANTHONY MARKUS ; KOSCHORECK KEVIN

Agent(s): WRAYS; PERRY AND CURRIER; MACRAE AND CO; BETTEN AND RESCH; MARGER JOHNSON AND MCCOLLOM PC; AMBRIC INC C O MARGER JOHNSON AND MCCOLLOM PC; BARNES AND THORNBURG LLP; GALBI ELMER W ET AL; REED JULIE L ET AL; JOHNSON ALEXANDER C ET AL

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN SV SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Title: STORAGE OF PROGRAM CODE IN ARBITRARY LOCATIONS IN MEMORY

Abstract: A method of storing at least one functionally identical code segment in each of a plurality of devices, each of the devices having a memory, the method comprising, for each device: (a) determining a first memory location; and (b) storing a first of the at least one code segments in the memory at the first memory location; wherein the first memory location is different in at least a plurality of the respective devices.

Classifications:

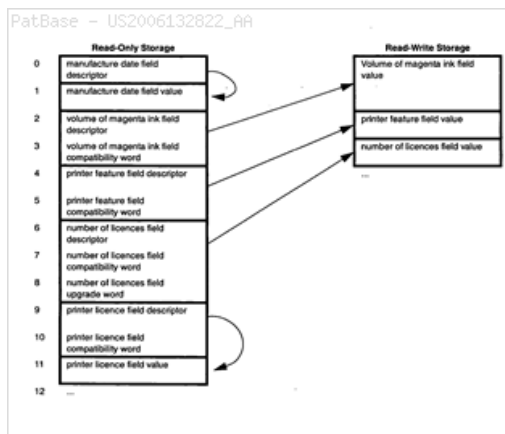
International (IPC 8-9): B41B1/02 G06F13/00 G06F15/00 G06F9/00 (Advanced/Invention);

B41B1/00 G06F15/00 G06F9/00 (Core/Invention)

CPC: G06F12/1408 G06F21/57 G06F21/72

European: G06F12/14B G06F21/57 G06F21/72

US: 358/1.14 358/1.140P 358/1.16 358/1.160P 358/1.160S 711/154 711/164 711/168 711/E12.092 711/E12.092S



Family:

Publication number	Publication date	Application number	Application date
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Priority:

US20040854502 20040527 US20070749123 20070515

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): WALMSLEY SIMON R ; WALMSLEY SIMON ROBERT

Inventor(s): WALMSLEY SIMON

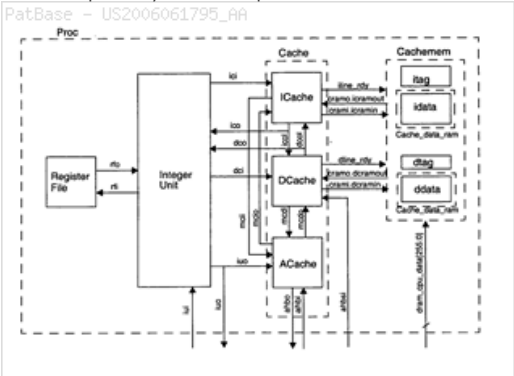
Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: STORAGE OF KEY IN ARBITRARY LOCATIONS IN MEMORY

Abstract: A method of storing a bit-pattern in each of a plurality of devices, each of the devices having a memory, the method comprising, for each device: (a) determining a first memory location; and (b) storing the bit-pattern at the first memory location; wherein the first memory locations are different in at least a plurality of the respective devices.

Classifications:

International (IPC 8-9): B41B1/02 G06F12/00 G06F13/00 G06F15/00 (Advanced/Invention); B41B1/00 G06F13/00 G06F15/00 (Core/Invention)
CPC: G06F21/73 G06F21/75
European: G06F21/73 G06F21/75
US: 358/1.14 358/1.140P 358/1.16 358/1.160P 358/1.160S 711/154 711/164 711/168



Family:

Publication number	Publication date	Application number	Application date
US2006061795 AA	20060323	US20040854500	20040527
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Priority:

US20040854500 20040527 US20070748483 20070514

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): WALMSLEY SIMON ROBERT ; WALMSLEY SIMON R

Inventor(s): WALMSLEY SIMON

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: GENERATION SEQUENCES

Abstract: A method for providing a sequence of nonces (R0, R1, R2,) commencing with a current seed of a sequence of seeds (x1, x2, x3,...), the method comprising: (a) applying a one-way function to the current seed, thereby to generate a current nonce; (b) outputting the current nonce; (c) using the current seed to generate a next seed in a sequence of seeds, the seed so generated becoming the current seed; and (c) repeating steps (a) to (c) as required to generate further nonces in the sequence of nonces.

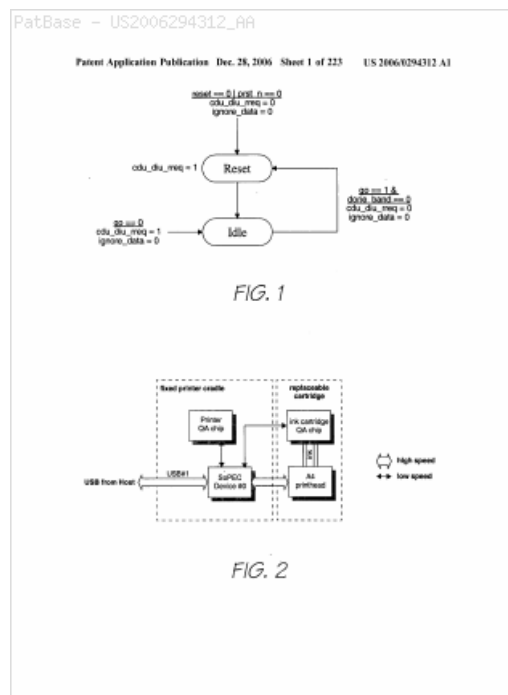
Classifications:

International (IPC 8-9): G06F12/14 H04L9/08 (Advanced/Invention); G06F12/14 (Core/Invention)

CPC: H04L9/3271 G06F2221/2103 H04L9/0662 H04L9/3215
H04L9/3239 H04L9/3247

European: H04L9/06M2B H04L9/22 H04L9/32F H04L9/32H
H04L9/32L2 H04L9/32N H04L9/32R H04L9/32S S06F221/2103

US: 380/278 380/278P 711/122 711/122P



Family:

Publication number	Publication date	Application number	Application date
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Priority:

US20040854518 20040527 US20100959296 20101202

Probable Assignee: SILVERBROOK RESEARCH PTY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD

Inventor(s): (std): WALMSLEY SIMON R ; WALMSLEY SIMON ROBERT

Inventor(s): WALMSLEY SIMON

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: **DATA** RATE EQUALISATION TO ACCOUNT FOR RELATIVELY DIFFERENT PRINthead WIDTHS

Abstract: A printer controller configured to generate dot **data** for **supply** to a printhead that includes at least first and second longitudinally extending printhead chips that are positioned adjacent each other either side of a join region such that a printing width of the printhead is wider than the length of either printhead chip, the printer controller being configured such that, in the event that the printhead chips to which dot **data** is being **supplied** are of sufficiently unequal relative length, the dot **data** is **supplied** more frequently, or at a higher rate, to the longer of the two printhead chips.

Classifications:

International (ipc 8-9): B41J2/05 B41J2/155 B41J29/38 G06F21/00 H04L9/00 H04N1/405 (Advanced/Invention); B41J2/05 G06F21/00 H04L9/00 H04N1/405 (Core/Invention)

International (ipc 1-7): B41J29/38

CPC: Y10S707/99933 Y10S707/99939 Y10T29/49401 G06F21/73 B41J2/04505 B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405

European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20

US: 347/13 347/40 347/42 347/5 347/6 347/6P 347/9

PatBase - US2004223010_AA

Patent Application Publication Nov. 11, 2004 Sheet 1 of 331 US 2004/0223010 A1

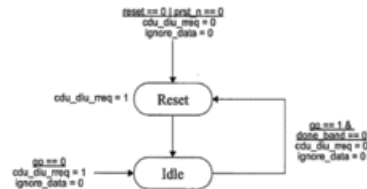


FIG. 1

Family:

Publication number	Publication date	Application number	Application date
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US7121639 BB	20061017	US20030727204	20031202

Priority:

AU20020953134 20021202 AU20020953135 20021202

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD ; PLUNKETT RICHARD THOMAS

Inventor(s): (std): PLUNKETT RICHARD THOMAS

Title: DATA RATE SUPPLY PROPORTIONAL TO THE RATIO OF DIFFERENT PRINthead LENGTHS

Abstract: A printer controller configured to generate dot data for supply to a printhead which includes at least a first printhead integrated circuit and a second printhead integrated circuit positioned adjacent each other either side of a join region, the printer controller configured to transfer dot data to each of the first printhead integrated circuit and the second printhead integrated circuit at a rate proportional to the relative lengths of the first printhead integrated circuit and the second printhead integrated circuit.

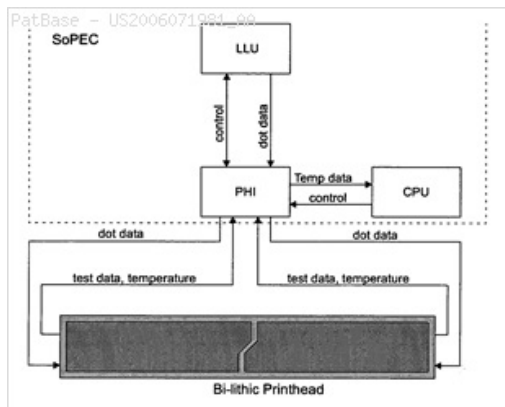
Classifications:

International (IPC 8-9): B41J2/05 B41J2/155 B41J29/38 G06F21/00 H04L9/00 H04N1/405 (Advanced/Invention); G06F21/00 H04L9/00 H04N1/405 (Core/Invention)

CPC: Y10S707/99933 Y10S707/99939 G06F21/73 B41J2/04505 B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 Y10T29/49401

European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20

US: 347/13 347/49 347/5 347/59 347/59P



Family:

Publication number	Publication date	Application number	Application date
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Priority:

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US20050272491 20051114

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): PLUNKETT RICHARD THOMAS ; PLUNKETT RICHARD T

Inventor(s): PLUNKETT RICHARD

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: CONTROLLER FOR PRINthead HAVING ARBITRARILY JOINED NOZZLE ROWS

Abstract: A controller for a printhead is provided. The printhead has rows of printing nozzles with each nozzle row formed by adjacent sub-rows of printing nozzles of adjacently disposed printhead modules. Each nozzle row is arranged such that the join of the respective adjacent sub-rows is arbitrarily located relative to the other nozzle rows thereby forming an arbitrarily shaped join region. The controller being configured to determine the arbitrary shape of the join region and to supply dot data to the printhead which compensates for the determined arbitrary shape.

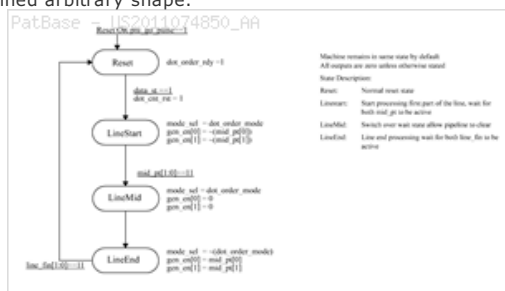
Classifications:

International (IPC 8-9): B41J2/05 B41J2/14 B41J29/38 G06F21/00 H04L9/00 H04N1/405 (Advanced/Invention)

CPC: Y10S707/99933 Y10S707/99939 G06F21/73 B41J2/04505 B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 Y10T29/49401

European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20

US: 347/12 347/12P 347/14 347/49 347/5

**Family:**

Publication number	Publication date	Application number	Application date
US2011074850 AA	20110331	US20100958968	20101202
US8038239 BB	20111018	US20100958968	20101202

Priority:

AU20020953134 20021202 AU20020953135 20021202 US20030727162 20031202
US20100958968 20101202

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): PLUNKETT RICHARD THOMAS ; WALMSLEY SIMON ROBERT

Title: PFN/TRAC SYSTEM™ FAA UPGRADES FOR ACCOUNTABLE REMOTE AND ROBOTICS CONTROL TO STOP THE UNAUTHORIZED USE OF AIRCRAFT AND TO IMPROVE EQUIPMENT MANAGEMENT AND PUBLIC SAFETY IN **TRANSPORTATION**

Abstract: This invention, a Protected Primary Focal Node PFN is a Trusted Remote Activity Controller TRAC and mobile communication router platform that provides accountable remote and robotics control to **transportation** vehicles by interfacing with the vehicles E/E systems. It connects each vehicle either on the earth's surface or near the earth's surface with application specific intranets for air, sea and land travel, via either host commercial servers or agency providers through wireless communication gateways and then further interfaces these vehicles in a larger machine messaging matrix via wireless and IP protocols to further coordinate movement assess and manage equipment use and impact on the world resources, societies infrastructure and the environment. This filing focuses directly on PFN/TRAC System use to augment and upgrade public safety and security in the Airline Industry and restrict any unauthorized use of an aircraft. Additionally, this application and related filings teaches the PFN/TRAC System™ use for all vehicle platforms to increase safety and security in a free society like the United State of America. The other related filings instruct in the technology's use for robust and accountable remote control for personal applications, stationary equipment and standalone functions, and coordinates them and interfaces them within the communication matrix. The TRAC controller also performs translation and repeating functions across a wide variety of communication protocols to complete a more mobile flexible matrix or web. This connected communication matrix of computers and humans provides an enhanced Human Machine Interfacing HMI scenario both locally and systemically in real-time for improve equipment management and world stability.

Classifications:

International (IPC 8-9): B64C13/20 B64D45/00

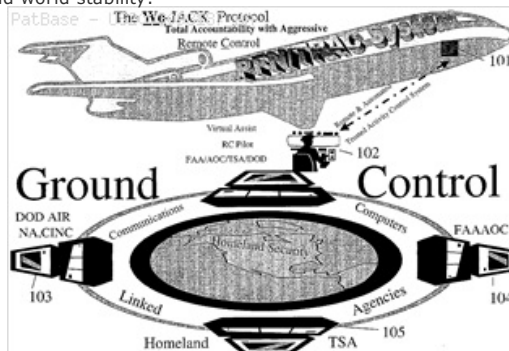
G07C5/00 (Advanced/Invention)

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European: B64C13/20 B64D45/00H G07C5/00T G08B13/196L3A G08B27/00T G08B31/00 L64D45/00H2A L64D45/00H3 L64D45/00H5 Y02T50/44

US: 244/189 340/961 340/961S 701/1 701/16 701/16P 701/1P 701/2 701/3 701/36 701/36S 701/3S



Family:

Publication number	Publication date	Application number	Application date
AU2002334708 AA	20030414	AU20020334708	20021001
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US6965816 BB	20051115	US20020260525	20021001
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Priority:

US20010325538P 20011001 US20010330085P 20011019 US20020260525 20021001
 WO2002US30857 20021001 US20050086494 20050323

Probable Assignee: KLINE AND WALKER LLC

Assignee(s): (std): KLINE AND WALKER LLC ; WALKER RICHARD C

Inventor(s): (std): RICHARD C WALKER ; WALKER RICHARD C

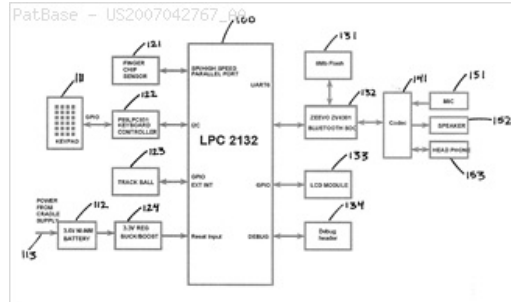
Inventor(s): WALKER RICHARD

Agent(s): WILMER CUTLER PICKERING HALE AND DORR LLP; IRAH H

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CO CR CY CZ DE DK DM DZ EC EE ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ OM PH PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW

Abstract: The present invention relates to a tethered digital butler consumer **electronics** product and method. The tethered digital butler, of a price and form factor suitable for consumer **electronics** markets of developed and developing countries, includes a communications and multi-media console and a wireless remote. The remote may resemble a handheld personal computer (HPC), a palm-held personal computer (PPC or PDA) or a smart phone, but has a low cost and feature set supported by the console that is novel in the consumer **electronics** market. In particular, this disclosure relates to combining telephone service, device control and, optionally, a fingerprint reader for easy user identification/authorization and personalization. As another option, a camera can be incorporated into the remote, thereby enabling video conferencing and other visual features. Alternatively, the remote may be packaged separately from a console and sold to interact with capabilities of a communications and console, set-top box, multi-media PC or other consumer **electronics** device from a different **source**, such as one running on a Windows, OS X or Linux platform, with or without telephone capabilities. The remote may include a media reader and remote **USB** port.

International (IPC 8-9): G05B15/00 G05B19/02 G05B19/04
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H04M7/00 H04N21/41 H04N21/4147 H04N21/422 H04N21/4223
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H04W4/00 H04W4/16 (Advanced/Invention);
G05B19/02 G05B19/04 G06F15/16 G06F7/02 G10L15/00 H04B1/06
H04B1/38 H04B7/00 H04M1/00 H04M1/72 H04M11/00 H04M3/00
H04N5/00 H04Q9/00 (Core/Invention);
H04M (Subclass/Invention)



Family:

Publication number	Publication date	Application number	Application date
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Priority:

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Probable Assignee: NEXSTEP INC

Assignee(s): (std): NEXSTEP INC ; NEXTSTEP INC ; ROBERT STEPANIAN ; ROBERT STEPHANIAN ; STEPANIAN ROBERT ; STEPHANIAN ROBERT

Inventor(s): (std): ROBERT STEPANIAN ; ROBERT STEPHANIAN ; STEPANIAN ROBERT ; STEPANIAN ROBERT

Agent(s): HORNER DAVID RICHARD; DAVIES SIMON ROBERT; MOETTELI MANTELLI NOVELLA; OHTSUKA FUMIAKI; SUDA HIROYUKI; KUMAKURA YOSHIO; NISHIJIMA TAKAKI; KOSHISHIBA ERI; KONDO NAOIKI; UESUGI HIROSHI; DESHIMARU TAKESHI; MASAKI YOSHIFUMI; HAYNES BEFFEL AND WOLFELD LLP; BEFFEL JR ERNEST J; ERNEST J; HAYNES BEFFEL AND WOLFELD; BEFFEL ERNEST J JR

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT QA RO RS RU RW SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: ENTERTAINMENT MONITORING SYSTEM AND METHOD

Abstract: An entertainment management system for the gaming industry provides real-time multi-site, slot accounting, player tracking, cage credit and vault, sports book **data** collection, and table game accounting.

Classifications:

International (ipc 8-9): A63F11/00 A63F13/00 A63F13/06 A63F13/10 A63F13/12 A63F13/20 A63F13/216 A63F13/35 A63F13/428 A63F9/24 G06F15/16 G06F17/00 G06F17/40 G06F19/00 G06F3/041 G06Q20/00 G06Q50/34 G07F17/32 G07F17/42 G07F7/08 H04L29/06 H04N7/18 (Advanced/Invention);

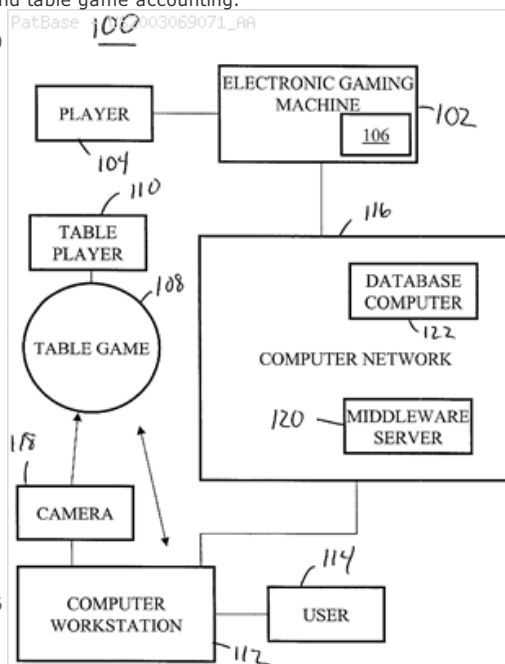
A63F13/00 A63F13/12 A63F9/24 G06F17/00 G06F19/00 G06Q20/00 G07F17/00 G07F17/32 G07F7/08 (Core/Invention)

International (ipc 1-7): A63B71/00 A63F13/00 A63F9/24 G06F15/00 G06F17/00 G06F17/40 G06F19/00 G06F3/041 G07F17/32 H04N7/18

CPC: G06Q20/045 G06Q20/06 G06Q30/0209 G06Q30/0212 G06Q30/0225 G07F17/42 G07F17/3255 G07F17/3248 G07F17/3253 G07F17/3258 G07F17/3241 G06Q30/0208 G07F17/323 G07F17/3283 G07F17/3286 A63F13/35 H04L29/06027 A63F13/00 A63F13/428 G07F17/3209 G07F17/3211 G07F17/3227 G07F17/3234 G07F17/3237 G07F17/3239 G07F17/32 G07F17/3202 G07F17/3232 A63F13/06 A63F13/20 G06F3/041

European: G06F3/041 G06Q20/045 G06Q20/06 G06Q30/0208 G06Q30/0209 G06Q30/0212 G06Q30/0225 G07F17/32 G07F17/32C G07F17/32C2D G07F17/32C2F G07F17/32E2 G07F17/32E4 G07F17/32E6 G07F17/32E6B G07F17/32E6D G07F17/32E6D2 G07F17/32H G07F17/32K10 G07F17/32K12 G07F17/32K4 G07F17/32K8 G07F17/32M8H G07F17/42

US: 1/1 273/138.1 273/138.100P 463/16 463/17 463/20 463/21 463/25 463/25P 463/25S 463/26 463/27 463/27P 463/29 463/29P 463/29S 463/31 463/36 463/37 463/37P 463/38 463/40 463/40P 463/42 463/42P 463/42S 463/43 463/43S 700/91 700/91P 705/14 705/14.11 705/14.12 705/14.120P 705/14.14 705/14.140S 705/14.26 705/14.260S 709/201 709/202 709/203 709/205 709/208 709/217 709/218 709/219 709/227 709/228 709/230 709/246 709/249

**Family:**

Publication number	Publication date	Application number	Application date
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Priority:

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Probable Assignee: KONAMI GAMING INC

Assignee(s): (std): GUIBORD MARK ; GEORGE JEFF ; KONAMI GAMING INC ; GEORGE JEFFREY ; HUANG ZHIGUO ; HUBER DOUG ; MILLER CHARLES WAYNE ; MILLER WAYNE ; PERRY ROBERT ; TYNDALL TERRY ; SEPICH EDWARD ; POCHIN JOHN PAUL ; SMILEY DAVID ; SOUKUP THOMAS E ; SEPICH EDWARD IV ; SUTHERLAND STEVE ; SUTHERLAND STEPHEN ; BRITT TIM ; CRITTENDEN MICHAEL D ; DEMPSEY MARTIN ; TONE NORIO ; SEPICH IV EDWARD

Inventor(s): (std): CRITTENDEN MICHAEL D ; DAVID SMILEY ; DEMPSEY MARTIN ; DOUG HUBER ; GEORGE JEFF ; GEORGE JEFFREY ; GUIBORD MARK ; HUANG ZHIGUO ; HUBER DOUG ; JEFFREY GEORGE ; JOHN PAUL POCHIN ; MICHAEL D CRITTENDEN ; MILLER CHARLES WAYNE ; MILLER WAYNE ; PERRY ROBERT ; POCHIN JOHN PAUL ; SEPICH EDWARD ; SEPICH EDWARD IV ; SEPICH IV EDWARD ; SMILEY DAVID ; SOUKUP THOMAS E ; SUTHERLAND STEPHEN ; SUTHERLAND STEVE ; THOMAS E SOUKUP ; TONE NORIO ; TYNDALL TERRY ; ZHIGUO HUANG ; BRITT TIM ; CHARLES WAYNE MILLER

Inventor(s): CRITTENDEN MICHAEL ; SOUKUP THOMAS

Agent(s): FISHER ADAMS KELLY CALLINANS; FISHER ADAMS KELLY; FISHER ADAMS KELLY PTY LTD; GOWLING LAFLEUR HENDERSON LLP; HOWARD AND HOWARD ATTORNEYS PC; HOWARD AND HOWARD ATTORNEYS PLLC; YEE JAMES R ET AL; AMBURN DEAN W ET AL

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN SV SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Title: STORAGE OF KEY IN NON-VOLATILE MEMORY

Abstract: A method of storing a first bit-pattern in non-volatile memory of a device, the method comprising: (a) applying a one way function to a second bit-pattern associated with the device, thereby to generate a first result; (b) applying a second function to the first result and the first bit-pattern, thereby to generate a second result; and (c) storing the second result in the memory, thereby indirectly storing the first bit-pattern.

Classifications:

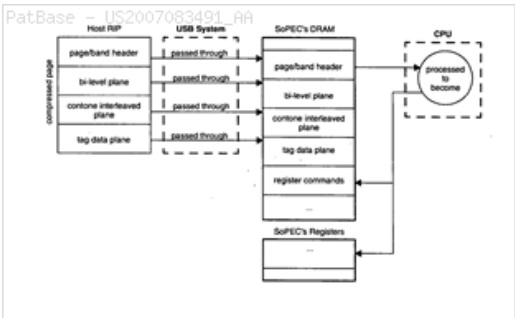
International (IPC 8-9): G06F17/30 (Advanced/Invention);

G06F17/30 (Core/Invention)

CPC: G06F21/608

European: G06F21/60C2

US: 1/1 1/1P 707/3 707/999.003 707/999.003S



Family:

Publication number	Publication date	Application number	Application date
US2007083491 AA	20070412	US20040854501	20040527

Priority:

US20040854501 20040527

Probable Assignee: SILVERBROOK RESEARCH PTY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD

Inventor(s): (std): MORPHETT BENJAMIN D ; WALMSLEY SIMON R

Inventor(s): WALMSLEY SIMON ROBERT ; MORPHETT BENJAMIN DAVID ; WALMSLEY SIMON ; MORPHETT BENJAMIN

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: MECHANISM FOR REDUCING WRITE PROBLEMS BY CONTROLLING CHARGE PUMPS FOR FLASH MEMORY

Abstract: An integrated circuit comprising a processor, a memory that the processor can access, a memory access unit for controlling accesses to the memory, an input for receiving power for the integrated circuit from an external power **source**, and a power detection unit, the power detection unit being configured to: monitor a quality of power **supplied** to the input; and in the event the quality of the power drops below a predetermined threshold, disabling a power **supply** to circuitry for use in writing to the memory, such that the memory access unit's ability to alter **data** in the memory is disabled prior to address or **data** values to be written to the memory becoming unreliable due to failing power.

Classifications:

International (ipc 8-9): B41J2/05 G06F21/00 H04L9/00

H04N1/405 (Advanced/Invention);

B41J2/05 G06F21/00 H04L9/00 H04N1/405 (Core/Invention)

International (ipc 1-7): H02H3/05

CPC: Y10S707/99933 Y10S707/99939 G06F21/73 B41J2/04505

B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543

B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554

G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74

G06F21/75 G06F21/78 H03K5/1252 H04N1/405 Y10T29/49401

European: B41J2/045D12 B41J2/045D14 B41J2/045D15

B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47

B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B

G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78

H03K5/1252 H04N1/405 L41J202/20

US: 713/300 714/22 714/22P

PatBase - US2005160316_AA

Patent Application Publication Jul. 21, 2005 Sheet 1 of 331 US 2005/0160316 A1



FIG. 1

Family:

Publication number	Publication date	Application number	Application date
US2005160316 AA	20050721	US20030727238	20031202

Priority:

AU20020953134 20021202 AU20020953135 20021202

Probable Assignee: SILVERBROOK RES PTY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): SHIPTON GARY

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: TIME-BASED APPARATUS AND METHOD TO MITIGATE SEMICONDUCTOR AGING EFFECTS

Abstract: Systems, methods, and computer readable media that can mitigate the effects of semiconductor aging in a semiconductor device are described. Traditional methods of mitigating semiconductor aging can be wasteful since they overcorrect for aging using a high operational voltage. The approach discussed herein steps up the operational voltage for the **electronic** device with time based on predetermined aging models. This allows power consumption by the **electronic** device, particularly early in the designed operational life, to be much less than it would otherwise be.

Classifications:

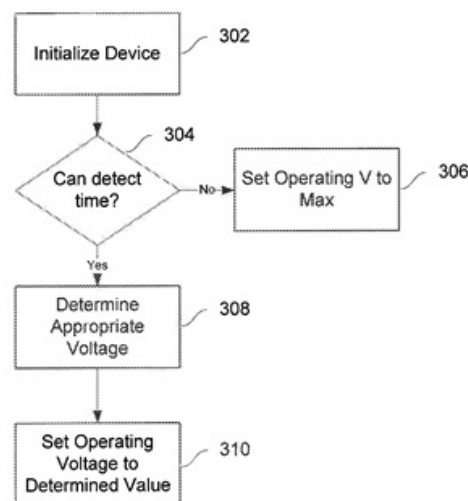
International (IPC 8-9): G05D3/12 G05F1/10 G06F1/00 G06F1/04 G06F1/20 G06F1/26 G06F1/32 G06F11/00 G06F11/10 G06F12/08 G06F12/14 G06F13/14 G06F13/24 G06F17/00 G06F21/00 G06F21/44 G06F3/14 G06F9/00 G06F9/46 G06T1/00 G09G5/00 G09G5/10 G09G5/36 G11C29/00 H01L21/66 H01L23/34 H01L25/00 H01L35/00 H03K19/01 H03K3/011 H03K3/03 H03K3/037 H03K5/13 H03L7/00 H03L7/06 H03L7/08 H03L7/097 H03L7/099 H03M13/00 H03M13/09 H04B1/40 H04B17/00 H04L7/02 H04W88/02 (Advanced/Invention); G06F1/00 G06F1/26 G06F1/32 G06F13/00 G09G5/37 H03K3/03 H03K3/037 H03K5/00 H03K5/13 (Advanced/Non-invention)

CPC: G06F11/1064 G06F12/0864 G06F2212/1028 G06F2212/601 H03M13/19 H03M13/3715 G09G2320/041 G09G2330/021 G09G2330/045 G09G2370/02 G06F1/3275 H03K3/0315 H03K3/0375 H03K5/133 H03K2005/00026 H03K2005/00058 H03K19/01 G06F1/3206 G06F1/324 G09G5/363 G09G5/37 G09G2340/02 G09G2360/121 G09G2370/022 H01L2924/0002 G06F1/3296 G06F1/206 H01L2924/00 H03L7/0802 G06F1/26 G06F1/3203 G06F1/3228 G06F12/14 G06F21/44 H03L7/097 H03L7/0997 H03K3/037 H03K2005/00019 H01L23/34 G06F3/14 Y02D10/126 Y02D10/172 Y02D10/13 Y02D10/14

US: 1/1 324/532 324/535 326/17 327/142 327/143 327/146 327/147 327/149 327/155 327/158 327/161 327/291 327/298 327/512 327/530 327/544 327/564 327/99 345/520 345/522 370/318 370/329 375/224 375/294 375/327 375/349 375/359 375/360 375/376 455/114.2 455/115.1 455/118 455/260 455/314 455/323 455/550.1 455/572 455/63.1 455/67.11 455/67.13 455/67.14 455/76 455/78 455/80 710/260 710/317 713/100 713/189 713/300 713/320 713/322 713/500 713/502 714/758 714/762 714/E11.044 718/102 718/105 726/16 726/34

PatBase - US2013043914_AA

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**Family:**

Publication number	Publication date	Application number	Application date
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Priority:

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Probable Assignee: AVAGO TECHNOLOGIES LTD

Assignee(s): (std): BROADCOM CORP ; JUNG HWISUNG ; FULLERTON MARK ; BENNETT JAMES ; HUKKOO AJAT ; GELMAN ANATOLY ; GUETTAF AMAR ; CHOU PAUL ; WALLEY JOHN ; SIPPEL TIM ; PENZES PAUL ; KOTHARI LOVE ; ZHANG ZHONGMIN ; RAJAN RAJESH ; THOMPSON KERRY ALAN ; THOMPSON KERRY ; ALARCON VERONICA

Assignee(s): AVAGO TECHNOLOGIES GENERAL IP SINGAPORE PTE LTD ; AVAGO TECHNOLOGIES LTD ; BANK OF AMERICA NA COLLATERAL AGENT AS

Inventor(s): (std): ALARCON VERONICA ; BENNETT JAMES ; BENNETT JAMES D ; CHOU PAUL ; FULLERTON MARK ; GELMAN ANATOLY ; GUETTAF AMAR ; HUKKOO AJAT ; HWISUNG JUNG ; JUNG HWISUNG ; KOTHARI LOVE ; PENZES PAUL ; RAJAN RAJESH ; SIPPEL TIM ; THOMPSON KERRY ; THOMPSON KERRY ALAN ; WALLEY JOHN ; ZHANG ZHONGMIN

Agent(s): Jehle Volker Armin; JEHLER VOLKER ARMIN; STERNE KESSLER GOLDSTEIN AND FOX PLLC; SOKOHL ROBERT E ET AL; BONOWIT DONALD R ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT QA RO RS RU RW SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A RECONFIGURABLE HARDWARE-BASED MULTIMEDIA DEVICE

Abstract: A system, method and article of manufacture are provided for providing a hardware-based reconfigurable multimedia device. A default multimedia application is initiated on a reconfigurable multimedia device. A request for a second multimedia application is received from a user. Configuration **data** is retrieved from a **data source** and is used for configuring the logic device to run the second multimedia application. The second multimedia application is run on the logic device.

Classifications:

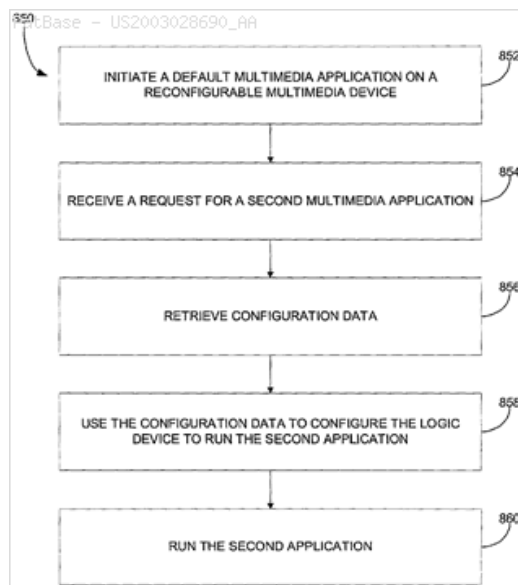
International (IPC 8-9): G06F1/24 G06F11/00 G06F13/00 G06F15/177 G06F15/78 G06F3/00 G06F9/00 G06F9/445 G06F9/45 (Advanced/Invention)

International (IPC 1-7): G06F1/24 G06F11/00 G06F13/00 G06F15/177 G06F15/78 G06F17/00 G06F17/00 G06F17/50 G06F3/00 G06F9/00 G06F9/44 G06F9/445 G06F9/45 H03K19/00 H04M1/253 H04M7/00

CPC: G06F15/7867

European: G06F15/78R

US: 703/20 709/221 710/8 713/100



Family:

Publication number	Publication date	Application number	Application date
AU2001270873 AA	20020205	AU20010270873	20010719
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EP1334437 A2	20030813	EP20010949766	20010719
EP1374042 A2	20040102	EP20010951797	20010719
JP2004508617 T2	20040318	JP20020514570T	20010719
US2003028690 AA	20030206	US20010772533	20010129
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WO0208888 A3	20040226	WO2001GB03250	20010719
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WO0208936 A2	20020131	WO2001GB03248	20010719
WO0208936 A3	20031009	WO2001GB03248	20010719
WO0208937 A2	20020131	WO2001GB03256	20010719
WO0208937 A3	20031009	WO2001GB03256	20010719
WO0209286 A2	20020131	WO2001GB03254	20010719
WO0209286 A3	20030530	WO2001GB03254	20010719
WO0209403 A2	20020131	WO2001GB03241	20010719
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Priority:

US20000219753P 20000720	US20010772495 20010129	US20010772522 20010129
US20010772534 20010129	US20010772525 20010129	US20010772533 20010129
WO2001GB03248 20010719	WO2001GB03241 20010719	WO2001GB03250 20010719
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Probable Assignee: CELOXICA LTD

Assignee(s): (std): APPLEBY ALLIS JOHN DOMINIC OLI ; CELOXICA LTD ; WILSON ALEX ; SUTCLIFFE ASHLEY JOHN

Assignee(s): SURCLIFFE ASHLEY ; APPLCBY ALLIS JOHN ; APPLEBY ALIS JOHN ; APPLEBY ALLIS JOHN ; SUTCLIFFE ASHLEY ; APPLEBY ALLIS JOHN DOMINIC OLIVER ; CELOXIA LTD ; CELOXICA LIMITED

Inventor(s): (std): APPLCBY ALLIS JOHN ; APPLEBY ALIS JOHN ; APPLEBY ALLIS JOHN ; APPLEBY ALLIS JOHN DOMINIC OLI ; SURCLIFFE ASHLEY ; SUTCLIFFE ASHLEY ; SUTCLIFFE ASHLEY JOHN ; WILSON ALEX

Inventor(s): APPLEBY ALLIS JOHN DOMINIC OLIVER ; ASHLEY JOHN SUTCLIFFE ; JOHN DOMINIC OLIVER APPLEBY ALLIS ; ALEX WILSON

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Title: VEHICLE COMPUTER SYSTEM WITH OPEN PLATFORM ARCHITECTURE

Abstract: A vehicle computer system has a housing sized to be mounted in a vehicle dashboard or other appropriate location. A computer is mounted within the housing and executes an open platform, multi-tasking operating system. The computer runs multiple applications on the operating system, including both vehicle-related applications (e.g., vehicle security application, vehicle **diagnostics** application, communications application, etc.) and non-vehicle-related applications (e.g., entertainment application, word processing, etc.). The applications may be **supplied** by the vehicle manufacturer and/or by the vehicle user.

Classifications:

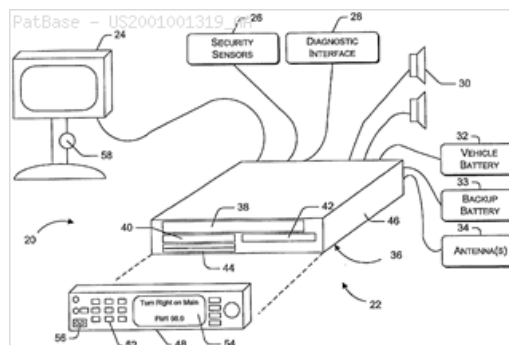
International (IPC 8-9): B60R11/00 B60R11/02 B60R16/02 B60R16/03 B60R25/00 G01C21/34 G06F1/16 G06F17/00 G06F19/00 H04B1/08 H04B7/00 H04L12/00 H04L29/06 H04L29/08 H04M1/60 (Advanced/Invention); B60R11/00 B60R16/03 G01C21/34 G06F1/16 H04L29/08 H04M1/60 (Advanced/Non-invention); B60R11/02 B60R16/02 B60R25/00 G01C21/34 G06F1/16 G06F17/00 G06F19/00 H04B7/00 H04L12/00 H04L29/06 H04L29/08 (Core/Invention); B60R11/00 B60R16/03 H04L29/08 H04M1/60 (Core/Non-invention)

International (IPC 1-7): B60R11/02 B60R16/00 B60R16/02 G01M17/00 G06F1/16 G06F17/00 G06F19/00 G06F7/00 H04B1/03 H04B1/08 H04B7/00 H04L12/00

CPC: H04L67/12 H04L67/42 H04L69/324 H04L69/329 G01C21/3688 B60R11/02 B60R11/0211 B60R11/0229 B60R11/0252 B60R16/0315 B60R25/00 B60R2011/0005 B60R2011/027 B60T2270/406 G01C21/3661 H04L29/06 H04L29/06027 H04M1/6041

European: B60R11/02 B60R25/00 G01C21/36G11 G01C21/36S H04L29/06 H04L29/06C6 H04L29/08A7 H04L29/08N11 L60R11/00P1A L60R11/02C L60R11/02E L60R11/02J L60R11/02Q L60R16/03M L60T270/406 T04L29/06C2 T04L29/06C8 T04L29/06J1 T04L29/08A2 T04M1/60T2

US: 248/27.1 248/558 307/10.2 307/10.7 340/4.37 340/4.41 340/825.14 340/825.24 340/825.25 361/679 361/679.33 361/679.4 361/679.55 361/683 361/725 361/731 361/733 361/814 370/522 455/3.06 455/345 455/346 455/348 455/552 455/557 701/1 701/29.1 701/31.4 701/31.400S 701/33 701/33S 701/34.3 701/36 701/36P

**Family:**

Publication number	Publication date	Application number	Application date
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AU199878528 A1	19981001	AU19980078528	19980728
AU200014956 A1	20000601	AU20000014956	20000207
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EP0804351 B1	20030827	EP19960942096	19961127
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EP1376882 B1	20070502	EP20030076562	19961127
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US5794164 A	19980811	US19950564586	19951129
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Priority:

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 US20000736531 20001211

Probable Assignee: MICROSOFT TECHNOLOGY LICENSING LLC

Assignee(s): (std): BECKERT RICHARD D ; MICROSOFT CORP ; MOELLER MARK M ; WONG WILLIAM S

Assignee(s): WONG WILLIAM ; MICROSOFT CORP REDMOND ; MICROSOFT TECHNOLOGY LICENSING LLC

Inventor(s): (std): BECKERT D ; MARK M MOELLER ; MOELLER M ; RICHARD D BECKERT ; WILLIAM WONG ; WONG WILLIAM S ; WONG WILLIAM ; RANDALL RON ; MOELLER MARK M ; BECKERT RICHARD D

Agent(s): DAVIES COLLISON CAVE; DAVIES COLLISON CAVE PTY LTD; RICHES MCKENZIE AND HERBERT LLP

Designated states: AT AU BE CA CH DE DK ES FI FR GB GR IE IT JP LU MC NL PT SE

Title: REMOTE MONITORING AND CONTROL SYSTEM COMPRISING MESH AND TIME SYNCHRONIZATION TECHNOLOGY

Abstract: A remote monitoring and control system comprising synchronized wireless MESH technology for remote monitoring and control of utility grids (e.g., utility meters), commodity distribution networks, industrial equipment, and infrastructure including remote disconnection/connection and self-generating power.

Classifications:

International (ipc 8-9): F03B13/10 F16K31/02 F17D3/01 F17D3/18 G05D11/00 G05D17/00 G05D3/12 G05D5/00 G05D9/00 G06F1/26 G06F1/28 G08C15/06 G08C17/00 G08C19/20 G08C19/22 H02P9/04 H04Q9/00 (Advanced/Invention);

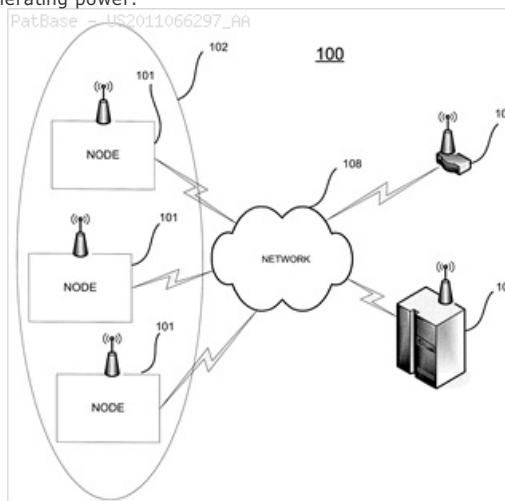
F16K31/02 F16K31/08 H04B7/00 (Advanced/Non-invention);

F16K31/02 (Core/Invention)

CPC: F16K37/0091 F16K31/046

European: F16K31/04E F16K37/00G

US: 251/129.04 251/129.11 251/65 290/43 290/54 340/870.03 340/870.07 700/287 700/287P



Family:

Publication number	Publication date	Application number	Application date
CA2725065 AA	20091126	CA20092725065	20090520
US2011066297 AA	20110317	US20090993780	20090520
US8843241 BB	20140923	US20090993780	20090520
WO09143287 A1	20091126	WO2009US44730	20090520

Priority:

US20080054779P 20080520
US20090993780 20090520

US20080108312P 20081024

WO2009US44730 20090520

Probable Assignee: SABERI ALI

Assignee(s): (std): GILBERT JAMES ROBERT ; LAY KEVIN ; LIVE METERS INC ; LIVEMETERS INC ; SABERI ALI

Inventor(s): (std): GILBERT JAMES ROBERT ; LAY KEVIN ; SABERI ALI

Agent(s): BERESKIN AND PARR LLP SENCRL SRL; DITTHAVONG AND STEINER PC; POSORSKE LAURENCE H ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: PROGRAMMABLE INPUT/OUTPUT CIRCUIT

Abstract: A apparatus, having a processing system and an input buffer coupled with both the processing system and one of two IO pads, and a reference buffer coupled to both the input buffer and the second of the IO pads such that the reference generator controls the input threshold of the input buffer in response to an analog voltage received from an external circuit on the second of the IO pads.

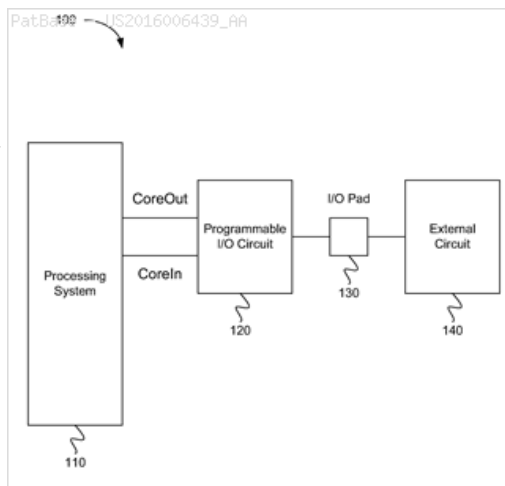
Classifications:

International (IPC 8-9): G01R31/317 G01R31/3177 G06F12/02 G06F13/28 G06F5/06 G11C16/10 G11C7/10 H03K19/0175 H03K19/094 H03K19/173 (Advanced/Invention); G06F13/40 (Advanced/Non-invention)

CPC: G06F13/4072 G06F13/28 H03K19/017581 G06F12/0246 G11C16/102 G06F2212/7201 G06F5/065 H03K19/01759 G11C7/1084 G11C7/1057 G01R31/3177 G01R31/31721 H03K19/173

European: H03K19/0175R

US: 1/1 326/38 326/82 326/83 326/86 327/109 327/112 710/302

**Family:**

Publication number	Publication date	Application number	Application date
US2016006439 AA	20160107	US20150690106	20150417
US2017194963 AA	20170706	US20160369674	20161205
US8179161 BA	20120515	US20100753657	20100402
US8487655 BA	20130716	US20100774680	20100505
US8558578 BA	20131015	US20120427264	20120322
US9013209 BA	20150421	US20130054657	20131015
US9143134 BA	20150922	US20130916386	20130612
US9515659 BB	20161206	US20150690106	20150417
US9952282 BA	20180424	US20150860515	20150921

Priority:

US20090175586P 20090505	US20090175856P 20090506	US20090176933P 20090510
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Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP ; HASTINGS MARK ; KOHAGEN NATHAN ; MAR MONTE ; KUTZ HAROLD ; SHUTT JAMES ; THIAGARAJAN EASHWAR ; SNYDER WARREN S ; SEGUINE DENNIS ; SULLAM BERT ; WILLIAMS TIMOTHY ; WRIGHT DAVID G ; VERGE GREGORY J ; WILLIAMS TIMOTHY J ; BYRKETT BRUCE ; BYRKETT BRUCE E

Assignee(s): CYPRESS SEMICONDUCTOR A OF DELAWARE CORP ; MORGAN STANLEY SENIOR FUNDING INC ; MORGAN STANLEY SENIOR FUNDING INC COLLATERAL AGENT AS

Inventor(s): (std): BYRKETT BRUCE ; BYRKETT BRUCE E ; HASTINGS MARK ; HASTINGS MARK E ; KOHAGEN NATHAN ; KOHAGEN NATHAN WAYNE ; KUTZ HAROLD ; KUTZ HAROLD M ; MAR MONTE ; SEGUINE DENNIS ; SEGUINE DENNIS R ; SEGUINE DENNIS RAYMOND ; SHUTT JAMES ; SHUTT JAMES H ; SNYDER WARREN S ; SULLAM BERT ; SULLAM BERT S ; THIAGARAJAN EASHWAR ; VERGE GREGORY J ; VERGE GREGORY JOHN ; WILLIAMS TIMOTHY ; WILLIAMS TIMOTHY J ; WILLIAMS TIMOTHY JOHN ; WRIGHT DAVID G

Title: MATH COPROCESSOR

Abstract: A math coprocessor **1300** includes a multiply-accumulate unit **1600**. Multiplier-accumulate unit **1600** includes a multiplier array **1603** for selectively multiplying first and second operands, the first and second operands having a **data** type selected from the group including floating point and integer **data** types. An adder **1604** selectively performs addition and subtraction operations on third and fourth operands, the third and fourth operands selected by multiplexer circuitry from the contents of a set of associated **source** registers, **data** output from multiplier array **1603** and **data** output from adder **1604**.

Classifications:

International (ipc 8-9): G06F7/38 G06F7/544 G06F7/57

G06F9/38 (Advanced/Invention);

G06F7/52 G06F7/53 (Advanced/Non-invention);

G06F7/48 G06F9/38 (Core/Invention)

International (ipc 1-7): G06F7/38 G06F7/48 G06F7/544

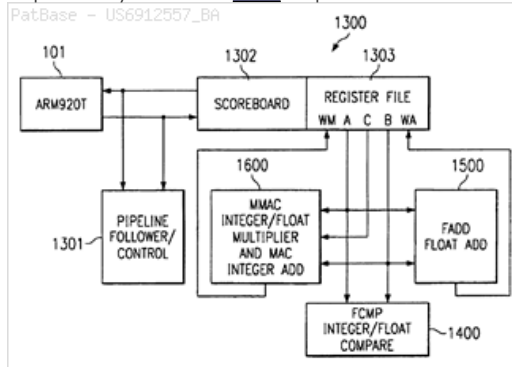
CPC: G06F9/3885 G06F7/483 G06F7/5324 G06F7/5443 G06F7/57

G06F2207/382 G06F2207/3884

European: G06F7/483 G06F7/48A G06F7/48A2 G06F7/544A

G06F7/57 G06F9/38S S06F207/38A4D2 S06F207/38A6P S06F7/53C

US: 708/490 708/495 708/524 712/E09.069 712/E9.069 712/E90.69



Family:

Publication number	Publication date	Application number	Application date
AU2001259389 AA	20011224	AU20010259389	20010503
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AU200159389 A5	20011224	AU20010059389	20010503
TW561399 B	20031111	TW20010112103	20010521
US6912557 BA	20050628	US20000591659	20000609
US7974996 BA	20110705	US20060474545	20060626
WO0197007 A2	20011220	WO2001US14203	20010503
WO0197007 A3	20020411	WO2001US14203	20010503

Priority:

US20000591659 20000609

WO2001US14203 20010503

US20040920879 20040818

US20060474545 20060626

Probable Assignee: CIRRUS LOGIC INC

Assignee(s): (std): CIRRUS LOGIC INC

Inventor(s): (std): NORTH GREGORY ALLEN ; GANESHAN MURLI

Inventor(s): GREGORY ALLEN NORTH ; MURLI GANESHAN

Agent(s): THOMPSON AND KNIGHT LLP; MURPHY JAMES J; JAMES J

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY CA CF CG CH CI CM CN CR CU CY CZ DE DK DM DZ EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Title: GLOBAL HARDWARE SUPERVISED POWER TRANSITION MANAGEMENT CIRCUITS, PROCESSES AND SYSTEMS

Abstract: An **electronic** circuit including a bus (3521), a **peripheral** (3510.i/3552.1) coupled to the bus (3521), the **peripheral** having a storing circuit (3620.i, 3625.i) for a succession-presetting and a parameter setting currently-effective for **peripheral** operation on the bus (3521); and a power management circuit (3570) operable in response to a power management transition request (GO_bit) to **send** a first signal (START_bit_i) to the **peripheral**, and to initiate a bus frequency transition, and to **send** a second signal (PER_ENABLE_i) to the **peripheral** after the bus frequency transition; and the **peripheral** is responsive to the first signal (START_bit_i) to stall **peripheral** operation on the bus (3521), the **peripheral** operable to automatically promote the succession pre-setting to currently-effective status for the **peripheral** after **peripheral** operations on the bus (3521) are stalled and responsive to the second signal (PER_ENABLE_i) to re-enable **peripheral** operation on the bus (3521). Other circuits, devices, systems, apparatus, and processes are disclosed.

Classifications:

International (IPC 8-9): G06F1/00 G06F1/08

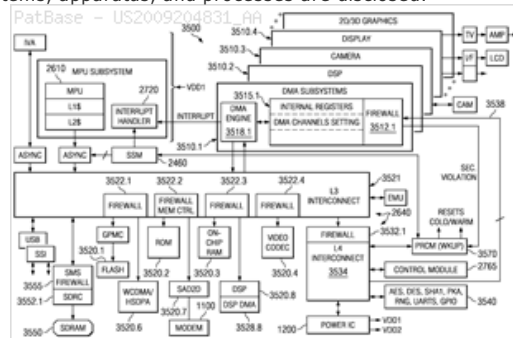
G06F1/32 (Advanced/Invention);

G06F1/08 (Core/Invention)

CPC: G06F1/3253 G06F1/3203 G06F1/324 G06F1/325 G06F1/3275
G06F1/3287 G06F1/3296 G09G5/006 G09G2360/128 G09G2370/16
Y02D10/126 Y02D10/14 Y02D10/171 Y02D10/172

European: G06F1/32P G06F1/32P5F G06F1/32P5P G06F1/32P5P8
G06F1/32P5S G06F1/32P5V G09G5/00T4 S09G360/12T S09G370/16
Y02B60/12D6 Y02B60/12F Y02B60/12N Y02B60/12N2 Y02B60/12N4

US: 713/322 713/322P



Family:

Publication number	Publication date	Application number	Application date
US2009204831 AA	20090813	US20090354351	20090115
US87755839 BB	20140708	US20090354351	20090115

Priority:

EP20080209119 20080208

Probable Assignee: TEXAS INSTRUMENTS INC

Assignee(s): (std): COUSSON BENOIT ; TEXAS INSTRUMENTS INC ; TITIANO PATRICK

Inventor(s): (std): COUSSON BENOIT ; TITIANO PATRICK

Agent(s): TEXAS INSTRUMENTS INC; RONALD O; FREDERICK J

Title: Memory resource arbitrator for multiple gate arrays

Abstract: A system, method and computer program product for arbitrating access to a shared memory resource by a plurality of gate arrays. During use, operations are executed on a plurality of gate arrays. Further, the gate arrays are allowed access to at least one shared memory resource during the execution of the operations thereon. Such access to the at least one shared memory resource is arbitrated to prevent conflict between the gate arrays.

Classifications:

International (IPC 8-9): G06F13/16 G06F15/78 G06F9/00

G06F9/455 (Advanced/Invention);

G06F13/16 G06F15/76 G06F9/00 G06F9/455 (Core/Invention)

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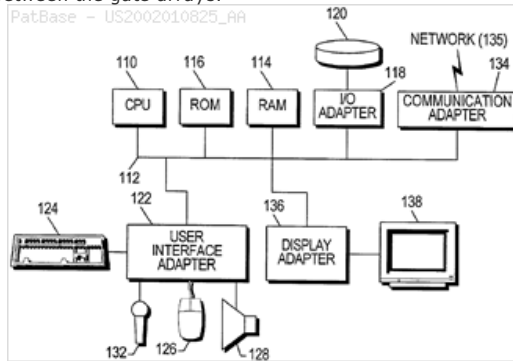
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G06F9/54 H03K19/177

CPC: G06F11/3672 G06F13/1605

European: G06F11/36T2 G06F13/16A

US: 703/26 710/240 714/E11.207



Family:

Publication number	Publication date	Application number	Application date
AU2001270874 AA	20020205	AU20010270874	20010719
AU2001270884 AA	20020205	AU20010270884	20010719
AU2002210676 AA	20020422	AU20020210676	20011011
AU2002210677 AA	20020422	AU20020210677	20011011
US2002010825 AA	20020124	US20010841701	20010423
US2002072893 AA	20020613	US20010859051	20010516
WO0208886 A2	20020131	WO2001GB03243	20010719
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WO0231653 A3	20031002	WO2001GB04536	20011011

Priority:

US20000219808P 20000720	US20000687012 20001012	US20000687481 20001012
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Probable Assignee: CELOXICA LTD

Assignee(s): (std): CELOXICA LTD ; CHENG PAULINE ; NICHOLS BENJAMIN ; ROWLAND JAMES ; WILSON ALEX

Assignee(s): CELOXICA LIMITED

Inventor(s): (std): CHENG PAULINE ; NICHOLS BENJAMIN ; ROWLAND JAMES ; WILSON ALEX

Inventor(s): PAULINE CHENG ; JAMES ROWLAND ; BENJAMIN NICHOLS ; ALEX WILSON

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PH PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Title: TEST, VALIDATION, AND **DEBUG** ARCHITECTURE

Abstract: An apparatus and method is described herein for providing a test, validation, and **debug** architecture. At a target or base level, hardware (Design for Test or DfX) are designed into and integrated with silicon parts. A controller may provide abstracted access to such hooks, such as through an abstraction layer that abstracts low level details of the hardware DfX. In addition, the abstraction layer through an interface, such as APIs, provides services, routines, and **data** structures to higher-level software/presentation layers, which are able to collect test **data** for validation and **debug** of a unit/platform under test. Moreover, the architecture potentially provides tiered (multiple levels of) secure access to the test architecture. Additionally, physical access to the test architecture for a platform may be simplified through use of a unified, bi-directional test access port, while also potentially allowing remote access to perform remote test and de-bug of a part/platform under test. In essence, a complete test architecture stack is described herein for test, validation, and **debug** of **electronic** parts, devices, and platforms.

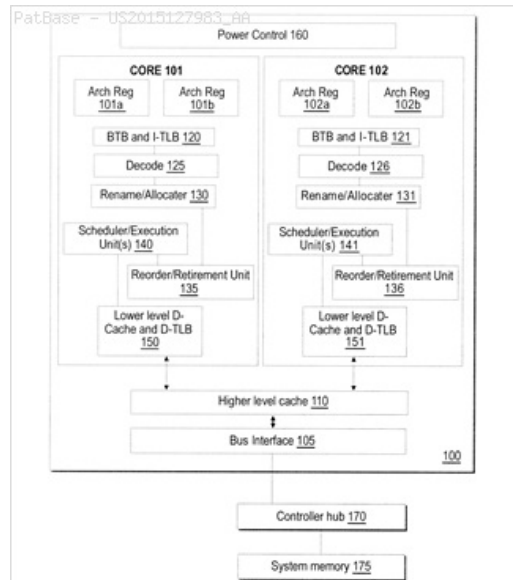
Classifications:

International (IPC 8-9): B01J19/00 C10L1/00 G06F G06F11/22 G06F11/273 G06F11/28 G06F11/36 G06F15/78

G06F21/62 (Advanced/Invention)

CPC: G06F11/3648 G06F11/3636 G06F11/267 G06F11/2733

US: 714/30



Family:

Publication number	Publication date	Application number	Application date
CN103748562 A	20140423	CN201080035787	20101223
DE112010006087 T5	20140626	DE201011006087T	20101223
GB201122290 A0	20120201	GB20110022290	20101223
GB2493793 A1	20130220	GB20110022290	20101223
IN09948DN2011 A	20121116	IN2011DN09948	20111216
JP2013529321 T2	20130718	JP20120549998T	20101223
JP2014170576 A2	20140918	JP20140092409	20140428
JP2017076412 A2	20170420	JP20160226340	20161121
JP5548966 B2	20140716	JP20120549998T	20101223
JP6047520 B2	20161221	JP20140092409	20140428
KR101581702 B1	20160111	KR20137016196	20101223
KR20130128424 A	20131126	KR20137016196	20101223
US2015127983 AA	20150507	US20100997182	20101223
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WO12087330 A3	20130613	WO2010US61995	20101223

Priority:

JP20120549998 20101223 JP20120549998T 20101223 US20100997182 20101223
 JP20140092409 20101223 WO2010US61995 20101223 JP20140092409 20140428
 JP20160226340 20161121

Probable Assignee: INTEL CORP

Assignee(s): (std): BAUDREXL JOHN ; BAUDREXL JOHN L ; CHEAH WEE HOO ; COOL LYLE ; COOL LYLE E ; DAVARE ABHIJIT ; GOFF TRAVIS ; FOO JIUN LONG ; GRAWROCK DAVID ; GOPAL SELVAKUMAR RAJA ; DOBLER NIEL ; DOBLER NEIL ; GRAWROCK DAVID W ; GOPAL PADMAKUMAR ; DRESCHER KEITH ; GOFF TRAVIS K ; FLOREY DAVID C ; GARTLER HERMANN W ; INTEL CORP ; MEYER BRIAN ; GREALISH JAMES ; MOHAMMED RAHIMA ; LEE YEN TAT ; KATARIA MUKESH ; LOVIN CHRISTIAN ; KABADI ASHOK ; MCCONNELL LOREN ; HALPRIN EVAN J ; KILLPACK KIP ; MARKLEY KYLE ; HAKIM NAGIB Z ; KOZACZUK ANTHONY ; LEE YUEN TAT ; KILLPACK KIP C ; IOVIN CHRISTIAN E ; LIEW VUI YONG ; MEYER BRIAR ; MOHAMMED RAHIMA K ; GREALISH JAMES J ; KABADI ASHOK N ; MCCONNELL LOREN J ; PRUDVI CHINNA ; PENNER BILL ; UDAWATTA KAPILA ; TIRUVALLUR KRESHAVAN ; YONG VUI ; SAMAN SAMIE B ; ZHENG TIEYU ; XIA AMY ; NEJEDLO JAY ; STOREY TIM ; SAHA RIDVAN ; WUNDERLICH RUSS ; TROBOUGH MARK ; WHITE MICHAEL T ; SALEM SANJAY S ; PENNER WILLIAM H ; NEJEDLO JAY J ; UDAWATTA KAPILA B ; WUNDERLICH RUSSELL J ; TROBOUGH MARK B ; RAMADORAI ARUN R ; STOREY TIMOTHY S ; QUERBACH BRUCE ; XIA YI AMY ; TIRUVALLUR KESHAVAN K ; PRUDVI CHINNA B ; PARKS EDWIN E ; SAHAN RIDVAN A ; PATRA PRIYADARSAN

Inventor(s): (std): ABHIJIT DAVARE ; ARUN R RAMADORAI ; ASHOK N KABADI ; BAUDREXL JOHN ; BAUDREXL JOHN L ; BRIAN MEYER ; BRUCE QUERBACH ; CHEAH WEE HOO ; CHINNA B PRUDVI ; COOL LYLE ; COOL LYLE E ; DAVARE ABHIJIT ; DAVID C FLORY ; DAVID W GRAWROCK ; DOBLER NEIL ; DOBLER NIEL ; DRESCHER KEITH ; EDWIN E PARKS ; EVAN J HALPRIN ; FLOREY DAVID C ; FOO JIUN LONG ; GARTLER HERMANN W ; GOFF TRAVIS ; GOFF TRAVIS K ; GOPAL PADMAKUMAR ; GOPAL SELVAKUMAR RAJA ; GRAWROCK DAVID ; GRAWROCK DAVID W ; GREALISH JAMES ; GREALISH JAMES J ; HAKIM NAGIB Z ; HALPRIN EVAN J ; HERMAN W GERTLER ; IOVIN CHRISTIAN ; IOVIN CHRISTIAN E ; CHRISTIAN E LOVIN ; JAMES J GREALISH ; JAY J NEJEDLO ; JOHN L BAUDREXL ; KABADI ASHOK ; KABADI ASHOK N ; KAPILA B UDAWATTA ; KATARIA MUKESH ; KEITH DRESCHER ; KESHAVAN K TIRUVALLUR ; KILLPACK KIP ; KILLPACK KIP C ; KIP C KILLPACK ; JIUN LONG FOO ; KOZACZUK ANTHONY ;

MOHAMMED RAHIMA ; MOHAMMED RAHIMA K ; MUKESH KATARIA ; NAGIB Z HAKIM ; NEJEDLO JAY ; NEJEDLO JAY J ; NIEL DOBLER ; PADMAKUMAR GOPAL ; PARKS EDWIN E ; PATRA PRIYADARSAN ; PENNER BILL ; PENNER WILLIAM H ; PRIYADARSAN PATRA ; PRUDVI CHINNA ; PRUDVI CHINNA B ; QUERBACH BRUCE ; RAHIMA K MOHAMMED ; LYLE E COOL ; MARK B TROBOUGH ; MARKLEY KYLE ; MCCONNELL LOREN ; MCCONNELL LOREN J ; MEYER BRIAN ; MEYER BRIAR ; KYLE MARKLEY ; LEE YEN TAT ; LEE YUEN TAT ; LIEW LONG VUI ; LIEW VUI YONG ; LOREN J MCCONNELL ; RAMADORAI ARUN R ; RIDVAN A SAHAN ; RUSSELL J WUNDERLICH ; SAHA RIDVAN ; SAHAN RIDVAN ; SAHAN RIDVAN A ; SALEM SANJAY S ; SAMAAN SAMIE B ; SAMIE B SAMAAN ; SANJAY S SALEM ; SELVAKUMAR RAJA GOPAL ; STOREY TIM ; STOREY TIMOTHY S ; TIEYU ZHENG ; TIMOTHY S STOREY ; TIRUVALLUR KESHAVAN K ; TIRUVALLUR KRESHAVAN ; TRAVIS K GOFF ; TROBOUGH MARK ; TROBOUGH MARK B ; UDAWATTA KAPILA ; UDAWATTA KAPILA B ; WHITE MICHAEL T ; WILLIAM H PENNER ; WUNDERLICH RUSS ; WUNDERLICH RUSSELL J ; XIA AMY ; XIA YI AMY ; YEN TAT LEE ; YI AMY XIA ; YONG VUI ; ZHENG TIEYU ; LOVIN CHRISTIAN ; VUI YONG LIEW

Inventor(s): WEE HOO CHEAH ; LYLE COOL ; VUI YONG ; TRAVIS GOFF ; TIM STOREY ; RIDVAN SAHA ; RUSS WUNDERLICH ; LOREN MCCONNELL ; MICHAEL T WHITE ; RAHIMA MOHAMMED ; KRESHAVAN TIRUVALLUR ; JOHN BAUDREXL ; KIP KILLPACK ; KAPILA UDAWATTA ; JAY NEJEDLO ; CHRISTIAN LOVIN ; JAMES GREALISH ; DAVID GRAWROCK ; CHINNA PRUDVI ; BILL PENNER ; ASHOK KABADI ; AMY XIA ; ANTHONY KOZACZUK

Agent(s): RYUKA IP LAW FIRM; VINCENT LESTER J ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: Voltage level shifting circuits and methods and systems using the same

Abstract: A level shifter 200 for shifting a logic high voltage of an input signal from a lower voltage to a higher voltage includes a latch 204 for storing a bit of **data** and having an output for driving a stored logic high bit at the higher voltage. A **data** node is coupled to a **source** of the higher voltage and an input of the latch. Voltage control circuitry 203 selectively gates the input signal received at the lower voltage with a bit of **data** stored in latch 204 and selectively pulls down the voltage at the **data** node in response.

Classifications:

International (IPC 8-9): G06F1/06 H03K3/356 (Advanced/Invention); G06F1/06 H03K3/00 (Core/Invention)

International (IPC 1-7): G06F1/04 G06F1/06 H03K19/075 H03K19/094 H03K3/356

CPC: H03K3/356113 H03K3/356182

European: H03K3/356G2 H03K3/356G6

US: 326/63 326/68 326/80 326/81 326/83 327/157 713/500

PatBase - US6535018_BA

U.S. Patent Mar. 18, 2003 Sheet 1 of 3 US 6,535,018 B1

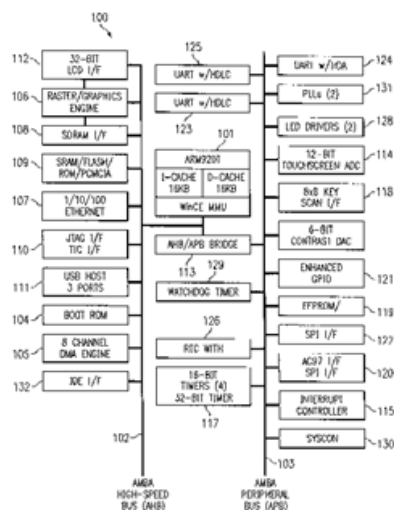


FIG. 1

Family:

Publication number	Publication date	Application number	Application date
AU2001237993 AA	20011224	AU20010237993	20010130
AU2001259825 AA	20011217	AU20010259825	20010503
TWI261159 B	20060901	TW20010112920	20010529
US6535018 BA	20030318	US20000625899	20000726
US6779125 BA	20040817	US20000590596	20000609
WO0195489 A1	20011213	WO2001US40667	20010503
WO0196992 A1	20011220	WO2001US02979	20010130

Priority:

US20000590596 20000609 US20000625899 20000726 WO2001US02979 20010130

Probable Assignee: CIRRUS LOGIC INC

Assignee(s): (std): CIRRUS LOGIC INC

Inventor(s): (std): HABAN SCOTT ; KOST MICHAEL ALLAN

Inventor(s): SCOTT HABAN ; MICHAEL ALLAN KOST

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY CA CF CG CH CI CM CN CR CU CY CZ DE DK DM DZ EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Title: DISTRIBUTED NETWORKED **DATA** ACQUISITION DEVICE

Abstract: A distributed networked **data** acquisition system having distributed networked **data** acquisition devices based on embedded Linux development platform having an ARM9 CPU is proposed. The system is defined as one or more distributed networked **data** acquisition devices together with a host. The host could dynamically display **data** and also coordinate and control the many distributed networked **data** acquisition devices. Each distributed networked **data** acquisition device is connected with the host by means of transmission media. The distributed networked **data** acquisition devices adopts the distributed **data** acquisition network to implement multi-point **data** acquisition having many distributed networked **data** acquisition devices working together and using several UTPs to connect with the distributed networked **data** acquisition devices in various distribution points. Each distributed networked **data** acquisition device can connect with different types of sensors, and each sensor can collect different types of continuous signals.

Classifications:

International (IPC 8-9): G06F15/173 G06F15/177 G08C19/00

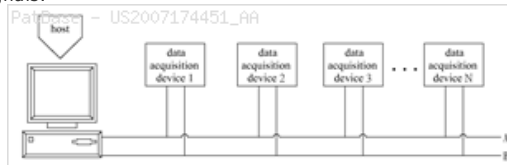
G08C23/06 H04L12/00 (Advanced/Invention);

G06F15/16 (Core/Invention)

CPC: G01D4/004 Y02B90/242 Y04S20/322

European: G01D4/00R1 Y02B90/24B2 Y04S20/32B

US: 709/220 709/221 709/222 709/224 709/224P

**Family:**

Publication number	Publication date	Application number	Application date
CN100437655 C	20081126	CN200610045690	20060120
CN1804921 A	20060719	CN200610045690	20060120
US2007174451 AA	20070726	US20060567732	20061206
US7953828 BB	20110531	US20060567732	20061206

Priority:

CN200610045690 20060120

Probable Assignee: NORTHEASTERN UNIV

Assignee(s): (std): CONGHUI SONG ; DONGSHENG YANG ; HE REN ; HUAGUANG ZHANG ; JIAN FENG ; JINHAI LIU ; UNIV NORTHEASTERN ; ZHILIANG WANG ; KAI SUN ; QIUYE SUN ; XIUCHONG LIU ; TOHOKU UNIV

Assignee(s): NORTHEASTERN UNIV ; NORTHEASTERN UNIVERSITY

Inventor(s): (std): HE REN ; HE SUN KAIREN ; HUAGUANG ZHANG ; JIAN FENG ; JINHAI LIU ; KAI SUN ; CONGHUI SONG ; CONGHUI SONG ; DONGSHENG YANG ; QIUYE SUN ; XIUCHONG LIU ; ZHILIANG WANG ; ZHANG HUAGUANG FENG

Inventor(s): HUAGUANG FENG ZHANG ; YANG DONGSHENG ; ZHANG HUAGUANG ; SONG CONGHUI ; SUN KAIREN HE ; SUN QIUYE ; WANG ZHILIANG ; FENG JIAN ; LIU JINHAI ; LIU XIUCHONG

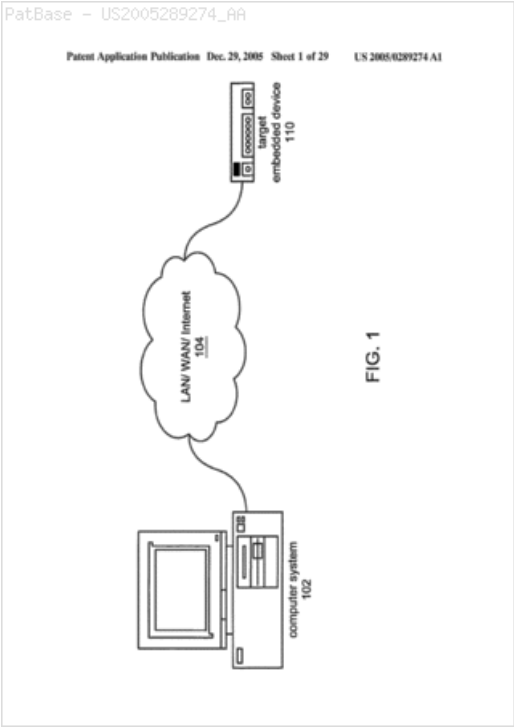
Agent(s): LIN AND ASSOCIATES INTELLECTUAL PROPERTY

Title: COMPACT MODULAR EMBEDDED DEVICE

Abstract: A compact modular embedded device. A base module includes a processor, a memory medium operable to store a bootloader for executing graphical programs, a buss and a power input coupled to the processor, memory medium, and bus, for receiving power from a power [source](#) and providing the received power to the processor, memory medium, and bus. The base module can couple to a host computer via a transmission medium, receive a program from the host computer, and store the program in the memory medium. The base module may couple to extension modules via the bus in a stacked fashion, where the base module and the extension modules each include a respective substantially planar circuit board that when stacked are substantially parallel. Each extension module provides respective functionality for the device. The base module can execute the program to perform a function in conjunction with the extension modules.

Classifications:

International (IPC 8-9): G05B15/00 G06F1/18 G06F13/00 G06F17/50 (Advanced/Invention);
G06F15/02 G06F15/16 H05K5/00 (Advanced/Non-invention);
G06F1/18 G06F13/00 (Core/Invention)
International (IPC 1-7): G06F13/00
CPC: G06F1/183 G06F8/51
European: G06F1/18S G06F8/51
US: 361/724 700/1 708/131 709/208 710/303 710/303P 716/7



Family:

Publication number	Publication date	Application number	Application date
US2005289274 AA	20051229	US20040875054	20040623
US7860582 BB	20101228	US20040875054	20040623

Priority:

US20040875054 20040623

Probable Assignee: NATIONAL INSTRUMENTS CORP

Assignee(s): (std): NAT INSTR CORP

Assignee(s): NATIONAL INSTRUMENTS CORP

Inventor(s): (std): CRISAN GRATIAN I ; FOLEA SILVIU ; GHERCIOIU MARIUS ; HEDESIU HOREA ; MONOSES IOAN ; CETERAS CIPRIAN

Inventor(s): CRISAN GRATIAN

Agent(s): MEYERTONS HOOD KIVLIN KOWERT AND GOETZEL PC; JEFFREY C; MARK S

Title: SYSTEM-ON-A-CHIP

Abstract: A system 100 fabricated on a single integrated circuit chip includes a microprocessor 101 operating from a high speed bus 102 and a peripheral bus 103 operating in conjunction with high speed bus 102 through a bus bridge 113. A first set of processing resources operate from high speed bus 102 and includes an external memory interface 108, a direct memory access engine 105 for controlling the exchange of information through memory interface 108, and a boot memory 104 for storing boot code. A second set of processing resources operate from peripheral bus 103 and includes an interrupt controller 115 for issuing interrupt requests to microprocessor 101, a set of programmable timers 117 for generating timed interrupt signals, and a phase locked loop 131 for generating timing signals.

Classifications:

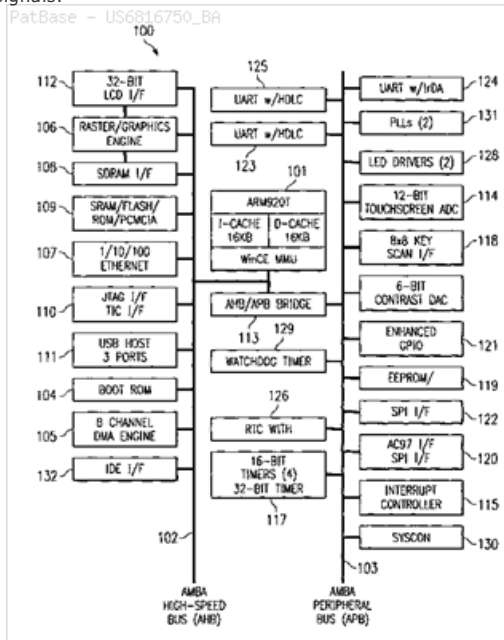
International (IPC 8-9): G06F15/00 G06F15/78 (Advanced/Invention); G06F15/00 G06F15/76 (Core/Invention)

International (IPC 1-7): G06F13/28 G06F13/40 G06F15/00 G06F15/78 G06F19/00 H05K1/00

CPC: G06F15/7832 Y02D10/12 Y02D10/13

European: G06F15/78M1

US: 700/121 710/22 710/8 712/33 712/35 712/41



Family:

Publication number	Publication date	Application number	Application date
AU2001231229 AA	20011224	AU20010231229	20010130
AU200131229 A1	20011224	AU20010031229	20010130
AU200131229 A5	20011224	AU20010031229	20010130
TW1254211 B	20060501	TW20010111834	20010517
US6816750 BA	20041109	US20000590506	20000609
WO0197576 A2	20011220	WO2001US02919	20010130
WO0197576 A3	20020510	WO2001US02919	20010130

Priority:

US20000590506 20000609 WO2001US02919 20010130

Probable Assignee: CIRRUS LOGIC INC

Assignee(s): (std): CIRRUS LOGIC INC

Inventor(s): (std): KLAAS JEFF ; KLASS JEFFREY

Inventor(s): JEFFREY KLASS ; JEFF KLAAS

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY CA CF CG CH CI CM CN CR CU CY CZ DE DK DM DZ EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Title: MICROPROCESSOR BASED POWER MANAGEMENT SYSTEM ARCHITECTURE

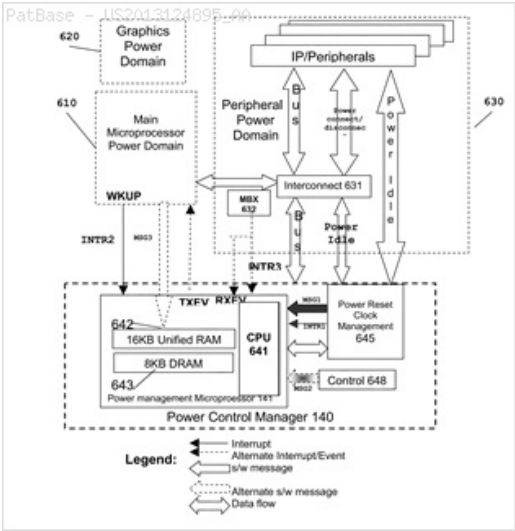
Abstract: An **electronic** system is disposed on a single integrated circuit including a plurality of power domains and a power control manager. Each power domain may be independently powered. The power control manager includes a set of control registers storing individual control bits, a power switch for each power domain and a programmable microprocessor. The programmable microprocessor controls the digital state of individual bits within the control registers thereby controlling the ON and OFF state of the corresponding power domain.

Classifications:

International (IPC 8-9): G06F1/00 G06F1/26
G06F1/32 (Advanced/Invention)

CPC: G06F1/26 G06F1/3234 G06F1/3237 G06F1/3287 Y02D10/128
Y02D10/171

US: 1/1 713/300 713/323



Family:

Publication number	Publication date	Application number	Application date
US2013124895 AA	20130516	US20120676573	20121114
US9471121 BB	20161018	US20120676573	20121114

Priority:

US20110559177P 20111114 US20120676573 20121114

Probable Assignee: TEXAS INSTRUMENTS INC

Assignee(s): (std): TEXAS INSTRUMENTS INC

Inventor(s): (std): SARATHY VIJAY ; SAHA ARINDAM ; DHAM ISH KUMAR ; BONNETT WILLIAM B

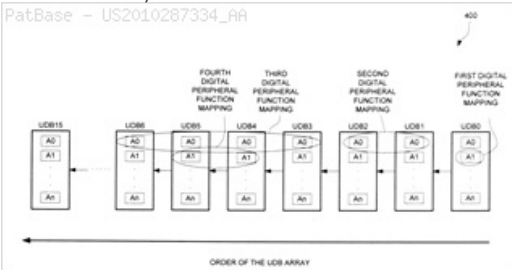
Agent(s): FRANK D; ROBERT D

Title: ADDRESSING SCHEME TO ALLOW FLEXIBLE MAPPING OF FUNCTIONS IN A PROGRAMMABLE LOGIC ARRAY

Abstract: A programmable processing device comprises a plurality of universal digital blocks (UDBs) in a UDB linear array. Each register in each UDB is associated with a plurality of memory addresses, where each memory address is from each of the different memory address spaces associated with different access mode widths of different digital peripheral functions. A digital peripheral function of an access mode width is mapped to one or more contiguous UDBs starting with a first UDB in the UDB linear array. Based on the access mode width, one of the associated memory addresses is chosen for the first UDB.

Classifications:

International (IPC 8-9): G06F12/00 G06F12/02
G06F13/00 (Advanced/Invention)
CPC: G06F12/06 G06F12/109
US: 710/3 710/8 710/9 711/103 711/103P 711/202 711/202S
711/211 711/211S 711/E12.001 711/E12.001S 711/E12.008
711/E12.008S 711/E12.016 711/E12.016S



Family:

Publication number	Publication date	Application number	Application date
US2010287334 AA	20101111	US20100776324	20100507
US8112551 BB	20120207	US20100776324	20100507
US8639850 BA	20140128	US20120364629	20120202

Priority:

US20090176291P 20090507 US20100776324 20100507 US20120364629 20120202

Probable Assignee: CYPRESS SEMICONDUCTOR CORP
Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP ; SULLAM BERT
Assignee(s): MORGAN STANLEY SENIOR FUNDING INC
Inventor(s): (std): SULLAM BERT
Agent(s): CYPRESS SEMICONDUCTOR CORP

Title: CURRENT SENSING APPARATUS AND METHOD FOR A CAPACITANCE-SENSING DEVICE

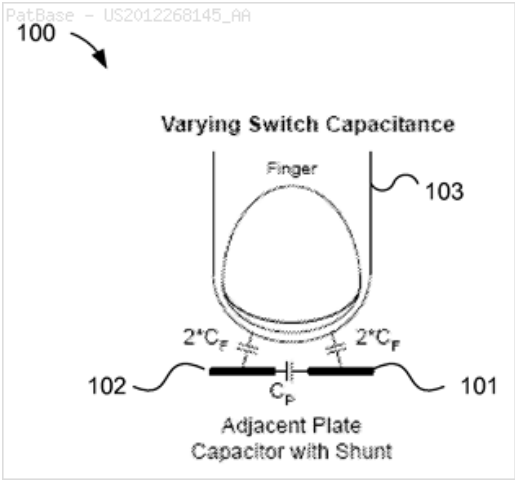
Abstract: A capacitance-sensing device including a current-to-voltage **converter** and an analog-to-digital **converter** is described. A sense element is coupled to an input of the current-to-voltage **converter**. The current-to-voltage **converter** is configured to **convert** current changes in the coupled sense element to an output voltage and to maintain a constant voltage at the input. The analog-to-digital **converter** is configured to **convert** the output voltage generated by the current-to-voltage **converter** to a digital value.

Classifications:

International (IPC 8-9): G01R27/26 G06F3/041 G06F3/044 H02M11/00 (Advanced/Invention)

CPC: G06F3/044 G06F3/0416 H03K2217/960735

US: 324/686 324/750.17 324/76.66 327/103



Family:

Publication number	Publication date	Application number	Application date
US2012268145 AA	20121025	US20110091067	20110420
US8786295 BB	20140722	US20110091067	20110420
WO12145034 A1	20121026	WO2011US66684	20111222

Priority:

US20110091067 20110420

Probable Assignee: PARADE TECHNOLOGIES LTD

Assignee(s): (std): CHANDRA LOKESH ; CYPRESS SEMICONDUCTOR CORP ; GRIVNA EDWARD

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC ; PARADE TECHNOLOGIES LTD

Inventor(s): (std): CHANDRA LOKESH ; GRIVNA EDWARD

Agent(s): LOWENSTEIN SANDLER LLP; KESSLEN MARK P ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT QA RO RS RU RW SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: System, method and article of manufacture for dynamic, automated product fulfillment for configuring a remotely located device

Abstract: A system, method and article of manufacture are provided for configuring a device according to input/selected parameters. One or more configuration parameters for a configurable hardware device are received. Hardware description **data** is generated based on the received parameters. The hardware description **data** is transmitted to the hardware device. The hardware device is configured according to the hardware description **data**.

Classifications:

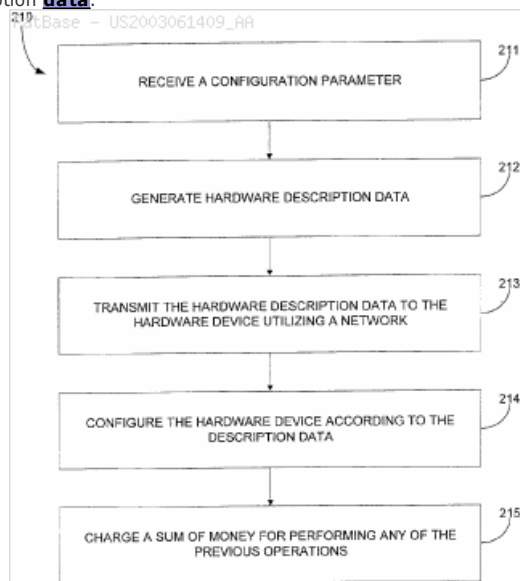
International (IPC 8-9): G06F3/033 G06F3/048
G06F9/445 (Advanced/Invention)

International (IPC 1-7): G06F3/00 G06F9/00 G06F9/24

CPC: G06F3/0481 G06F9/4411

European: G06F3/033A1 G06F3/0481 G06F9/44A4

US: 710/8 710/8P 713/1 713/1S 719/327 719/327S



Family:

Publication number	Publication date	Application number	Application date
US2003061409 AA	20030327	US20010792644	20010223

Priority:

US20010792644 20010223

Probable Assignee:

CELOXICA LTD

Assignee(s):

CELOXICA LTD ; RUDUSKY DARYL

Inventor(s): (std):

RUDUSKY DARYL

Title: GRAPHICAL USER INTERFACE FOR DISPLAY OF SYSTEM RESISTANCE

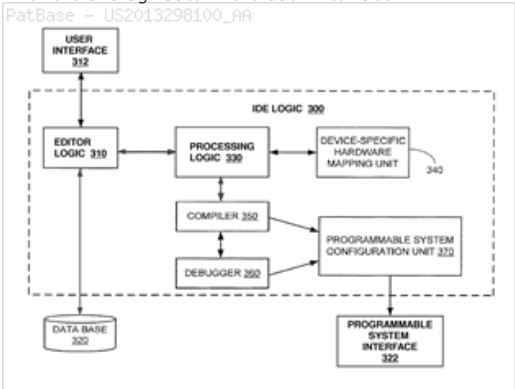
Abstract: Techniques for determining resistances of analog routes in **electronic** designs are described herein. In an example embodiment, a computer system receives first user input that indicates, in a user interface, a first component in an **electronic** design. The **electronic** design has been placed and routed for a programmable target device. The computer system receives second user input that selects, in the user interface, a particular component from one or more second components of the **electronic** design, where the one or more second components have analog connectivity to the first component. The computer system determines a resistance value of an analog route between the first component and the particular component, and displays the resistance value in association with the analog route in the user interface.

Classifications:

International (IPC 8-9): G06F17/50 (Advanced/Invention)

CPC: G06F17/50 G06F17/5036

US: 716/116 716/117 716/126 716/128 716/139



Family:

Publication number	Publication date	Application number	Application date
US2013298100 AA	20131107	US20130888148	20130506
US8640081 BB	20140128	US20130888148	20130506

Priority:

US20120643683P 20120507 US20130776107P 20130311 US20130888148 20130506

Probable Assignee:

CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std):

CYPRESS SEMICONDUCTOR CORP

Assignee(s):

MORGAN STANLEY SENIOR FUNDING INC

Inventor(s): (std):

HASTINGS MARK ; KEESER CHRIS

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A HARDWARE CONFIGURATION SERVICE

Abstract: A system, method and article of manufacture are provided for hardware design procurement. A customer request for a hardware configuration module is received. A **source** of the requested module is selected and a determination is made as to whether the customer and the **source** agree on a price for the module. The module is provided to the customer.

Classifications:

International (IPC 8-9): G06F17/50 G06Q30/00

G06Q30/08 (Advanced/Invention);

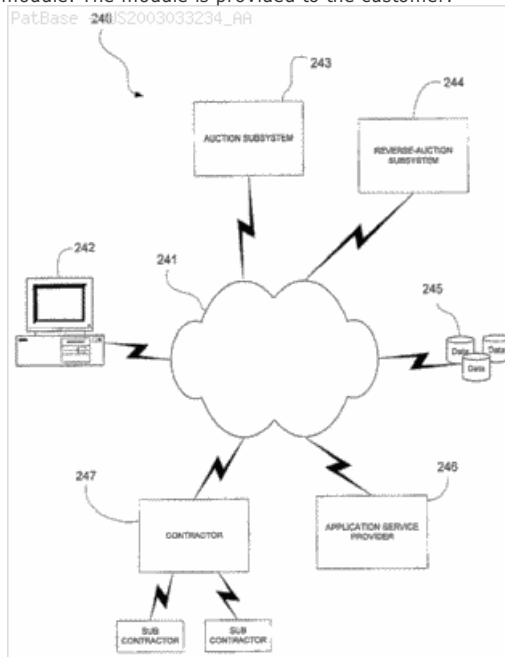
G06F17/50 G06Q30/00 (Core/Invention)

International (IPC 1-7): G06F17/60

CPC: G06F17/50 G06Q30/08 G06Q40/04

European: G06F17/50 G06F17/60B4 G06Q30/08 G06Q40/04

US: 705/37 705/37P



Family:

Publication number	Publication date	Application number	Application date
US2003033234 AA	20030213	US20010792401	20010223

Priority:

US20010792401 20010223

Probable Assignee:

CELOXICA LTD

Assignee(s):

CELOXICA LTD ; RUDUSKY DARYL

Inventor(s): (std):

RUDUSKY DARYL

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR COLLABORATIVE HARDWARE DESIGN

Abstract: A system, method and article of manufacture are provided for providing one or more modules conforming to a hardware design specification. A user specification for at least a portion of a hardware design is received. One or more modules conforming to the specification are identified. The module(s) are retrieved and sent to the user. The module can be used to configure a configurable hardware device.

Classifications:

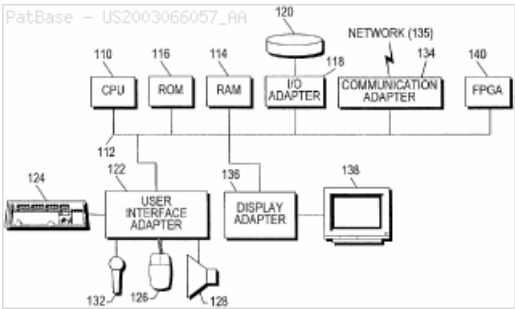
International (ipc 8-9): G06F17/50 G06F9/45 (Advanced/Invention); G06F17/50 G06F9/45 (Core/Invention)

International (ipc 1-7): G06F9/45

CPC: G06F17/5054 G06F17/5045 G06F17/505 G06F2217/04

European: G06F17/50D G06F17/50D2 G06F17/50D4

US: 717/140



Family:

Publication number	Publication date	Application number	Application date
US2003066057 AA	20030403	US20010791456	20010223

Priority:

US20010791456 20010223

Probable Assignee: RUDUSKY DARYL

Assignee(s): (std): RUDUSKY DARYL

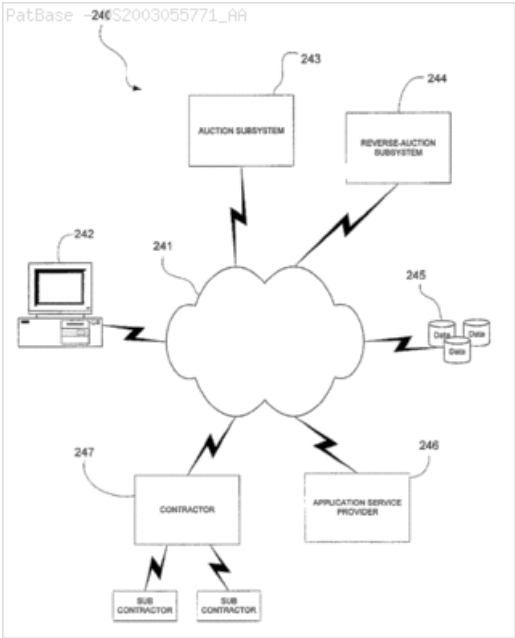
Inventor(s): (std): RUDUSKY DARYL

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A REVERSE-AUCTION-BASED SYSTEM FOR HARDWARE DEVELOPMENT

Abstract: A system, method and article of manufacture are provided for conducting a network-based reverse-auction for a hardware configuration module. A hardware design specification is received from a customer utilizing a network. A bid price is received. The bid price represents the amount of money that the customer is willing to pay for a hardware design module conforming to the design specification. The user can use the hardware design module for configuring a configurable hardware device. A determination is made as to whether the bid price is acceptable. The bid is accepted if the bid price is acceptable. The customer is notified if the bid price is not acceptable.

Classifications:

International (IPC 8-9): G06Q30/00 G06Q30/08 (Advanced/Invention); G06Q30/00 (Core/Invention)
International (IPC 1-7): G06F17/60
CPC: G06Q30/08 G06Q40/04
European: G06F17/60B4 G06Q30/08 G06Q40/04
US: 705/37 705/37P



Family:

Publication number	Publication date	Application number	Application date
US2003055771 AA	20030320	US20010792402	20010223

Priority:

US20010792402 20010223

Probable Assignee:

CELOXICA LTD

Assignee(s):

CELOXICA LTD ; RUDUSKY DARYL

Inventor(s): (std):

RUDUSKY DARYL

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR AN AUCTION-BASED SYSTEM FOR HARDWARE DEVELOPMENT

Abstract: A system, method and article of manufacture are provided for conducting an auction for a hardware configuration module utilizing a network. A description of a hardware configuration module desired to be purchased is received from a customer. Bid prices for the module are received from a plurality of customers. Bidding is terminated upon occurrence of a specified event. One or more auction winners are selected from among the customers.

Classifications:

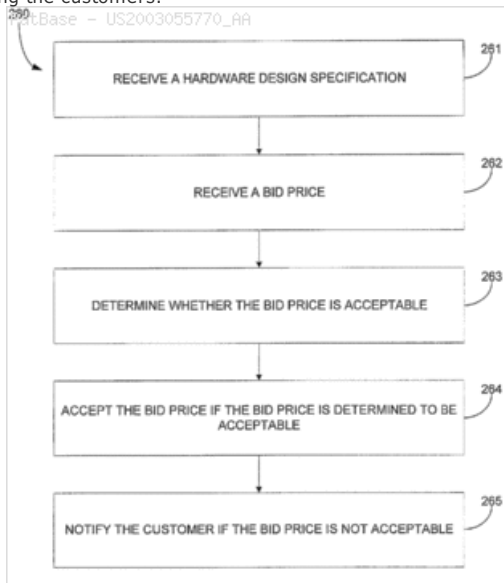
International (IPC 8-9): G06Q30/00 G06Q30/08 (Advanced/Invention); G06Q30/00 (Core/Invention)

International (IPC 1-7): G06F17/60

CPC: G06Q30/08 G06Q40/04

European: G06F17/60B4 G06Q30/08 G06Q40/04

US: 705/37 705/37P



Family:

Publication number	Publication date	Application number	Application date
US2003055770 AA	20030320	US20010792284	20010223

Priority:

US20010792284 20010223

Probable Assignee:

RUDUSKY DARYL

Assignee(s):

RUDUSKY DARYL

Inventor(s): (std):

RUDUSKY DARYL

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A CONTRACTOR-BASED HARDWARE DEVELOPMENT SERVICE

Abstract: A system, method and article of manufacture are provided for providing a hardware configuration module for generating revenue. A customer design specification for a configurable hardware device is sent to a contractor. The contractor analyzes the design specification. The contractor generates at least one hardware configuration module based on the design specification. The contractor compiles the modules into a file. The file is sent to the customer. The customer is charged an amount of money.

Classifications:

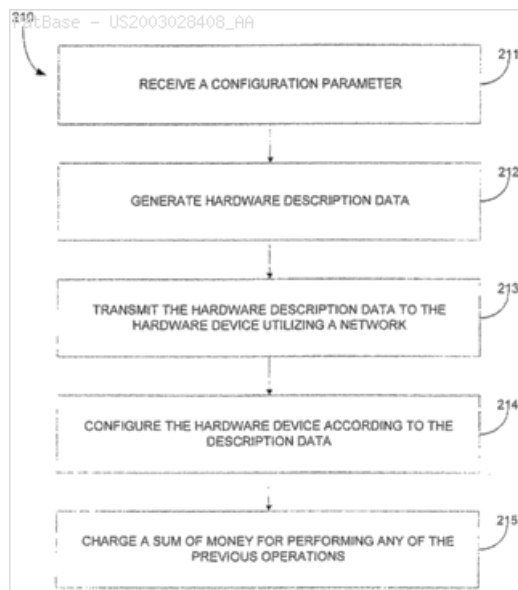
International (IPC 8-9): G06Q30/00 G06Q30/02
G06Q50/18 (Advanced/Invention);
G06Q30/00 (Core/Invention)

International (IPC 1-7): G06F17/60

CPC: G06Q30/02 G06Q40/04 G06Q50/188

European: G06F17/60B2 G06Q30/02 G06Q40/04 G06Q50/188

US: 705/37 705/37S 705/8 705/80 705/80P 705/8P



Family:

Publication number	Publication date	Application number	Application date
US2003028408 AA	20030206	US20010792283	20010223

Priority:

US20010792283 20010223

Probable Assignee:

CELOXICA LTD

Assignee(s): (std):

RUDUSKY DARYL

Assignee(s):

CELOXICA LTD

Inventor(s): (std):

RUDUSKY DARYL

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A LIBRARY-BASED HARDWARE CONFIGURATION SERVICE

Abstract: A system, method and article of manufacture are provided for generating revenue by charging for access to a library having a pre-compiled hardware configuration module therein. A plurality of hardware configuration modules are stored in a library. A customer is prompted for hardware configuration criteria, which can include such things as desired functionality, a desired clock speed, a price, a description of an I/O or other device that will be attached to the hardware to be configured, etc. The selected module is sent to the customer. The customer is charged an amount of money.

Classifications:

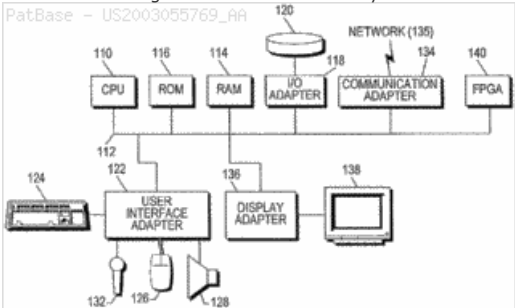
International (ipc 8-9): G06Q30/00 G06Q30/02
H04L12/24 (Advanced/Invention);
G06Q30/00 H04L12/24 (Core/Invention)

International (ipc 1-7): G06F17/60

CPC: H04L41/24 G06Q30/02 G06Q40/04 H04L41/22

European: G06F17/60B2 G06Q30/02 G06Q40/04 H04L12/24F3
H04L12/24F4 H04L41/22 H04L41/24

US: 705/37 705/37P



Family:

Publication number	Publication date	Application number	Application date
US2003055769 AA	20030320	US20010791241	20010223

Priority:

US20010791241 20010223

Probable Assignee:

CELOXICA LTD
RUDUSKY DARYL
CELOXICA LTD
RUDUSKY DARYL

Assignee(s): (std):

Assignee(s):

Inventor(s): (std):

Title: System, method and article of manufacture for a user interface for an MP3 audio player

Abstract: A system, method and article of manufacture provide a user interface for a decoder of audio **data** in the MPEG 1 Layer III (MP3) format. A display control program that controls operation of a touch screen is initiated. The touch screen is coupled to a reconfigurable logic device capable of decoding MP3 audio. A plurality of icons are displayed on the touch screen. A user selects one of the icons by touching the icon on the touch screen. A periodic determination is made as to whether a user has touched the touch screen. If a touch is detected, a location of the touch is determined. The location of the touch is correlated with one of the icons. A macro associated with the icon touched is called. The macro is utilized for processing a command for controlling the reconfigurable logic device.

Classifications:

International (IPC 8-9): G06F3/033 G06F3/048 (Advanced/Invention)

International (IPC 1-7): G09G5/00

CPC: G06F3/0488

European: G06F3/033D2 G06F3/0488

US: 715/810 715/810P

PatBase - US2003184593_AA

Patent Application Publication Oct. 2, 2003 Sheet 1 of 21 US 2003/0184593 A1

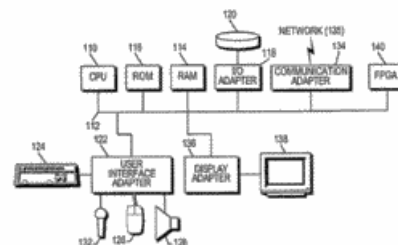


Fig. 1

Family:

Publication number	Publication date	Application number	Application date
US2003184593 AA	20031002	US20010973368	20011009

Priority:

US20010973368 20011009

Probable Assignee:

CELOXICA LTD

Assignee(s):

CELOXICA LTD ; DUNLOP ANDREW

Inventor(s): (std):

DUNLOP ANDREW

Title: COMPUTER-ASSISTED ROUTER FOR A PROGRAMMABLE DEVICE

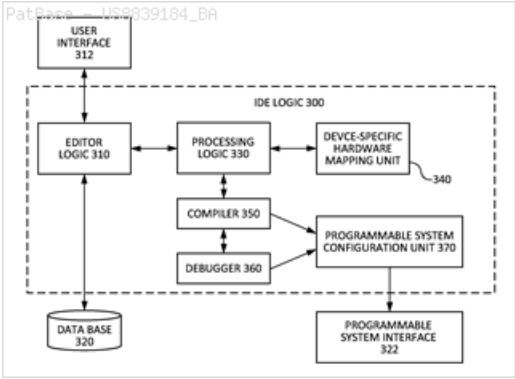
Abstract: Techniques for computer-assisted routing of an **electronic** design for a programmable target device are described herein. In an example embodiment, a computer system displays a representation of the programmable target device in a user interface. The computer system receives first user input that indicates a first component in the **electronic** design for the programmable target device. The computer system determines one or more second components of the **electronic** design that can be routed to the first component and displays one or more visual objects that indicate the one or more second components. The computer system then receives second user input that selects a particular component from the one or more second components and stores interconnect **data** indicating that the first component is routed to the

Classifications:

International (IPC 8-9): G06F17/50 (Advanced/Invention)

CPC: G06F17/5077 G06F17/5054

US: 716/110 716/116 716/119 716/126 716/139



Family:

Publication number	Publication date	Application number	Application date
US8839184 BA	20140916	US20140204440	20140311

Priority:

US20130776949P 20130312 US20140204440 20140311

Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC

Inventor(s): (std): IVANETS ADRIY ; SEGUINE DENNIS RAYMOND

Title: POLARITY INDEPENDENT POWER **SUPPLY** CONTROL METHODS AND SYSTEMS USING THE SAME

Abstract: A method of controlling a power **supply** having an output activated in response to a first logic level of a control signal and deactivated in response to a second logic level of the control signal. A clock is generated on a second power **source** and used to time a time-out period of a selected number of clock periods. In response to the step of sensing, if the state of the output of the power **supply** is inactive through the timeout period, then the first logic level of the control signal is generated to activate the power **supply** for use in powering operations of an associated device. After completion of these operations, the second logic level of the control signal is generated to deactivate the power **supply**. If however, the state of the output of the power **supply** is active during the time-out period, then the first logic level of the control signal is maintained to power operations of the associated device. At the end of these operations, the second logic level of the control signal is generated to deactivate the power **supply**.

Classifications:

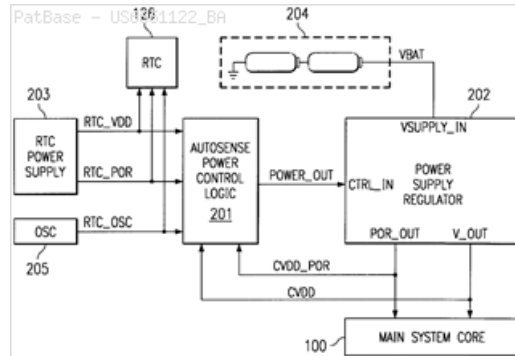
International (IPC 8-9): G06F1/26 G06F1/32 H01H35/00 H02M1/10 H02M3/00 H04L12/28 (Advanced/Invention); H02M1/10 (Advanced/Non-invention); G06F1/26 G06F1/32 H01H35/00 H02M1/10 H02M3/00 H04L12/28 (Core/Invention)

International (IPC 1-7): H01H35/00 H02B1/24 H02M1/10 H04L12/28

CPC: Y10T307/839 Y10T307/931 G06F1/3203 G06F1/26

European: G06F1/26 G06F1/32P

US: 307/127 307/138



Family:

Publication number	Publication date	Application number	Application date
AU2002362032 AA	20030623	AU20020362032	20021203
EP1451843 A1	20040901	EP20020797159	20021203
EP1451843 A4	20091118	EP20020797159	20021203
JP2005512438 T2	20050428	JP20030551801T	20021203
JP4091545 B2	20080528	JP20030551801T	20021203
KR100781831 B1	20071203	KR20047008516	20021203
KR20050044674 A	20050512	KR20047008516	20021203
US6661122 BA	20031209	US20010020142	20011207
WO03050833 A1	20030619	WO2002US38453	20021203

Priority:

US20010020142 20011207 WO2002US38453 20021203 WO2002US38453 20040603

Probable Assignee: CIRRUS LOGIC INC

Assignee(s): (std): CIRRUS LOGIC INC

Inventor(s): (std): DUNNIHOO JEFFREY

Inventor(s): JEFFREY DUNNIHOO

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ OM PH PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR DYNAMIC PROGRAMMING OF ONE RECONFIGURABLE LOGIC DEVICE FROM ANOTHER RECONFIGURABLE LOGIC DEVICE

Abstract: A system, method and article of manufacture are provided for dynamically programming a reconfigurable logic device. Configuration **data** for configuring a first reconfigurable logic device is acquired. A second reconfigurable logic device is utilized to process the configuration **data**. The second reconfigurable logic device configures the first reconfigurable logic device based on the configuration **data**.

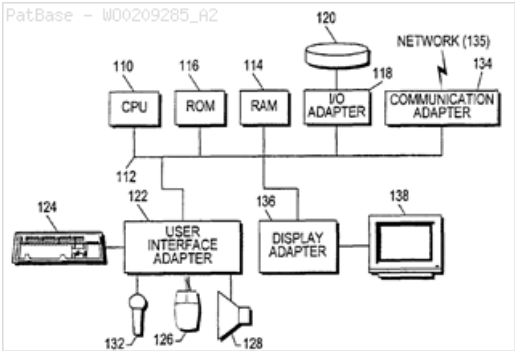
Classifications:

International (IPC 8-9): G06F15/78 (Advanced/Invention);
G06F15/76 (Core/Invention)

International (IPC 1-7): G06F15/78 G06F17/50 H03K19/00

CPC: G06F15/7867

European: G06F15/78R



Family:

Publication number	Publication date	Application number	Application date
AU2001270876 AA	20020205	AU20010270876	20010719
WO0209285 A2	20020131	WO2001GB03246	20010719
WO0209285 A3	20031002	WO2001GB03246	20010719

Priority:

US20000219748P 20000720 US20000687405 20001012 WO2001GB03246 20010719

Probable Assignee: CELOXICA LTD

Assignee(s): (std): CELOXICA LTD ; MANIKU SANJAY IBRAHIM

Assignee(s): CELOXICA LIMITED

Inventor(s): (std): MANIKU SANJAY IBRAHIM

Inventor(s): SANJAY IBRAHIM MANIKU

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Title: PROGRAMMABLE INTERRUPT ROUTING SYSTEM

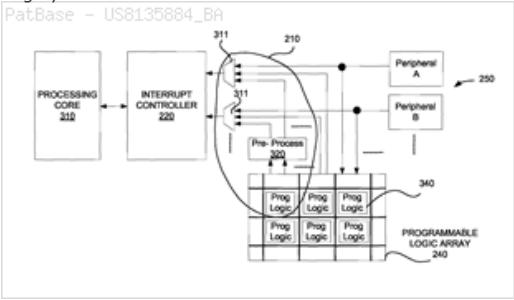
Abstract: A method and apparatus for a programmable interrupt routing system is described.

Classifications:

International (IPC 8-9): G06F13/24 G06F3/00 (Advanced/Invention)

CPC: G06F13/24

US: 710/266 710/48



Family:

Publication number	Publication date	Application number	Application date
US8135884 BA	20120313	US20100773590	20100504
US8838852 BA	20140916	US20120415671	20120308

Priority:

US20090175077P 20090504 US20100773590 20100504 US20120415671 20120308

Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP ; MOHAMMED HANEEF ; SULLAM BERT

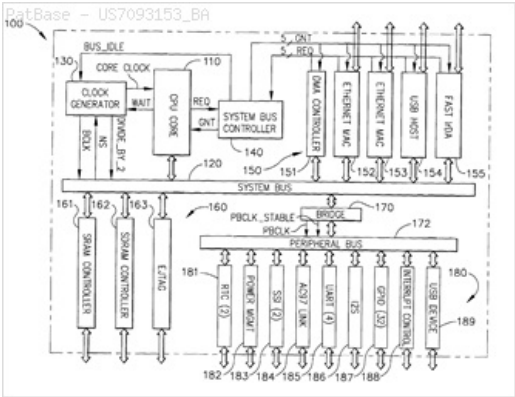
Assignee(s): MORGAN STANLEY SENIOR FUNDING INC

Inventor(s): (std): MOHAMMED HANEEF ; SULLAM BERT

Title: METHOD AND APPARATUS FOR LOWERING BUS CLOCK FREQUENCY IN A COMPLEX INTEGRATED **DATA** PROCESSING SYSTEM

Abstract: A **data** processing system (100) comprises a system bus (120), a plurality of devices (110, 150, 160, 170) coupled to the system bus (120), a bus monitor circuit (140), and a clock generator (130). The plurality of devices (110, 150, 160, 170) includes at least one bus master (110, 150) which is capable of performing accesses on the system bus (120). The bus monitor circuit (140) is coupled to the at least one bus master (110, 150), and has an output for providing a bus idle signal to indicate that no bus master is attempting to perform an access on the system bus (120). The clock generator (130) has an output coupled to at least one of the plurality of devices (110, 150, 160, 170) and provides a bus clock signal having a first frequency when the bus idle signal is inactive and having a second frequency lower than the first frequency when the bus idle signal is active.

Classifications:
International (IPC 8-9): G06F1/08 (Advanced/Invention)
CPC: Y02D10/126 Y02D10/151 G06F1/08 G06F1/3203 G06F1/324 G06F1/3253
European: G06F1/08 G06F1/32P G06F1/32P5F G06F1/32P5P1 Y02B60/12D6 Y02B60/12J2
US: 327/100 327/113 327/297 710/110 710/113 710/117 710/305 710/313 713/300 713/320 713/322 713/323 713/500 713/600 713/602 714/34 714/814 726/36



Family:

Publication number	Publication date	Application number	Application date
US7093153 BA	20060815	US20020284763	20021030

Priority:
US20020284763 20021030

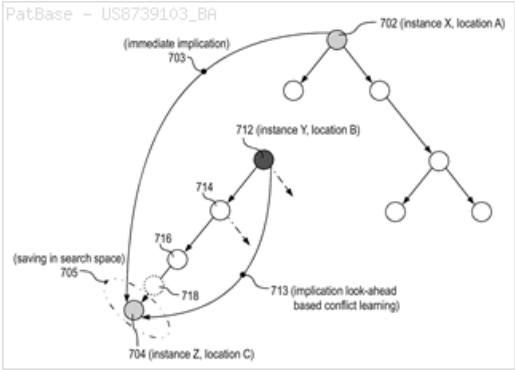
Probable Assignee: ADVANCED MICRO DEVICES INC
Assignee(s): (std): ADVANCED MICRO DEVICES INC
Assignee(s): ADVANCED MICRO DEVICES
Inventor(s): (std): HOOVER KATHRYN JEAN ; KROMER STEPHEN CHARLES ; MONTANARO JAMES JOSEPH ; PLUMMER SUZANNE ; WITEK RICHARD T
Agent(s): LARSON NEWMAN ABEL POLANSKY AND WHITE LLP

Title: TECHNIQUES FOR PLACEMENT IN HIGHLY CONSTRAINED ARCHITECTURES

Abstract: Techniques for placement in highly constraint chip architectures are described herein. In an example embodiment, a computer system places a digital portion of an **electronic** design for a programmable chip. The programmable chip comprises multiple fixed-function blocks and a plurality of pins, where each one of the multiple fixed-function blocks can be coupled only to a respective subset of the plurality of pins. The **electronic** design comprises a particular fixed-function block (FFB) instance that is connected to a particular input-output (IO) instance. The computer system places (e.g., by using a backtracking search) the particular FFB instance on a particular fixed-function block and the particular IO instance on a particular pin from a particular subset of the plurality of pins, where in the programmable chip the particular fixed-function block can be coupled only to the particular subset of the plurality of pins.

Classifications:

International (IPC 8-9): G06F17/50 (Advanced/Invention)
CPC: G06F17/5054 G06F17/5068
US: 716/111 716/117 716/118 716/119 716/122 716/132 716/136



Family:

Publication number	Publication date	Application number	Application date
US8739103 BA	20140527	US20130050105	20131009

Priority:

US20130772398P 20130304 US20130050105 20131009

Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC

Inventor(s): (std): ANANDH KRISHNAN ; DUTTA AVIJIT ; PRICE ANDREW ; SKUDLAREK JOSEPH ; THOMPSON ROBERT ; TUTTLE NEIL

Title: REDUCING WATER INFLUENCE ON A TOUCH-SENSING DEVICE

Abstract: A method and apparatus for reducing water influence on a touch-sensing device is described.

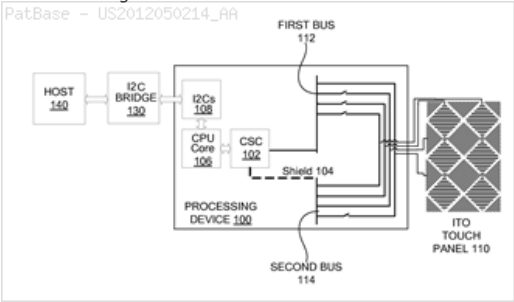
Classifications:

International (IPC 8-9): G06F3/044 (Advanced/Invention)

CPC: G06F3/0418 G06F3/044 G06F2203/04107

European: G06F3/041T2 G06F3/044 S06F203/04108

US: 345/174 345/174P



Family:

Publication number	Publication date	Application number	Application date
US2012050214 AA	20120301	US20100974991	20101221
US8717331 BB	20140506	US20100974991	20101221

Priority:

US20100376400P 20100824 US20100974991 20101221

Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP ; HUTNYK VOLODYMYR ; KARPIN OLEKSANDR ; KREMIN VIKTOR ; KULYK TARAS

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC ; PARADE TECHNOLOGIES LTD

Inventor(s): (std): HUTNYK VOLODYMYR ; KARPIN OLEKSANDR ; KREMIN VIKTOR ; KULYK TARAS

Search history

Search (USB or Universal Serial Bus) and (debug* or EUD or diagnos*) and electronic* (Results 34073)

1:

Search 1 and JTAG and hub and interface+ and peripheral (Results 197)

2:

Search 1 and JTAG and hub and peripheral (Results 198)

3:

Search 3 and (send* or convert* or trasmit* or transport*) and (data or packet*) (Results 195)

4:

Search 4 and ossillator* and (suppl* or source*) (Results 106)

5:

Search 5 and (SWD or serial wire debug) and COM (Results 1)

6:

Search 5 and (SOC or IC or SIP) and super speed (Results 5)

7:

Search 5 and PD<20141030 (Results 98)

8:

Search 8 and IC = G06F* (Results 57)

9:

Search PN=(WO2016069206) (Results 1)

10:

Search 11: [SP]: 1. an embedded universal serial bus (usb) debug (eud) in an electronic system, comprising: a usb hub, comprising: at least one upstream interface coupled to a usb physical layer (phy) in the electronic system and a plurality of downstream interfaces communicatively coupled to the at least one upstream interface and a multi-protocol debug peripheral coupled to one of the plurality of downstream interfaces, wherein the multi-protocol debug peripheral is configured to exchange usb formatted data packets with the usb hub over the one of the plurality of downstream interfaces wherein the multi-protocol debug peripheral is communicatively coupled to at least one debug function among a plurality of debug functions configured to support a plurality of debugging protocols in the electronic system to receive debugging information based on a supported debugging protocol among the plurality of debugging protocols from the at least one debug function wherein the multi-protocol debug peripheral is further configured to convert the debugging information received from the at least one debug function from the supported debugging protocol into the usb formatted data packets to be provided to the usb hub and wherein the usb hub is configured to provide the usb formatted data packets to the usb phy over the at least one upstream interface independent of whether a usb controller provided outside the eud in the electronic system is communicating with the usb phy. 2. the eud of claim 1, further comprising: an eud power supply coupled to the usb phy, wherein the eud power supply is configured to provide an operating power to the eud and an eud oscillator coupled to the usb phy, wherein the eud oscillator is configured to provide an operating clock to the eud. 3. the eud of claim 1, further comprising an eud power supply coupled to the usb phy, wherein the eud power supply is configured to provide an operating power to the eud independent of whether digital power supply voltages in the electronic system have been set to a non-operational level. 4. the eud of claim 1, further comprising an eud oscillator coupled to the usb phy, wherein the eud oscillator is configured to provide an operating clock to the eud independent of whether other system clocks in the electronic system are turned off. 5. the eud of claim 1, further comprising a bypass switch configured to enable a debugging mode for the electronic system. 6. the eud of claim 5, wherein the bypass switch comprises: a first bypass switch coupled to the at least one upstream interface and the usb phy and a second bypass switch coupled to the usb controller in the electronic system and one of the plurality of downstream interfaces. 7. the eud of claim 6, further comprising a disconnect switch configured to detach the electronic system from the usb hub by keeping the disconnect switch open. 8. the eud of claim 6, further comprising a disconnect switch configured to attach the electronic system to the usb hub by keeping the disconnect switch closed. 9. the eud of claim 1, further comprising a bypass switch configured to enable a mission mode for the electronic system by connecting the usb phy directly to the usb controller. 10. the eud of claim 9, wherein the bypass switch comprises: a first bypass switch coupled to the usb phy and decoupled from the at least one upstream interface and a second bypass switch coupled to the usb controller in the electronic system and the first bypass switch. 11. the eud of claim 1, wherein the multi-protocol debug peripheral is coupled to a joint test action group (jtag) debug function in the electronic system and configured to send or receive jtag debugging information with the respective jtag debug function. 12. the eud of claim 1, wherein the multi-protocol debug peripheral is coupled to a serial wire debug (swd) debug function in the electronic system and configured to send or receive swd debugging information with the respective swd debug function. 13. the eud of claim 1, wherein the multi-protocol debug peripheral is coupled to a system trace debug function in the electronic system and configured to send or receive system trace debugging information with the respective system trace debug function. 14. the eud of claim 1, wherein the multi-protocol debug peripheral is coupled to a communication (com) port debug function in the electronic system and configured to send or receive com port debugging information with the respective com port debug function. 15. the eud of claim 1, wherein the usb phy is a usb high-speed interface or a usb super-speed interface. 16. the eud of claim 1, wherein the electronic system is a system-on-chip (soc) integrated circuit (ic). 17. the eud of claim 1, wherein the electronic system is a system-in-package (sip) based electronic system comprising at least one secondary electronic system wherein the at least one secondary electronic system comprises a secondary eud having at least one secondary upstream interface. 18. the eud of claim 17, wherein one of the plurality of downstream interfaces is coupled to the at least one secondary upstream interface to send or receive the debugging information with the at least one secondary electronic system. 19. a method for enabling a debugging process in an electronic system using an embedded universal serial bus (usb) debug (eud), comprising: attaching the electronic system to a usb host detecting a presence of the usb host by the eud detecting if the debugging process is permitted in the electronic system by the eud receiving at least one eud configuration from the usb host receiving at least one debug command by the eud from the usb host collecting debugging information based on a supported debugging protocol among a plurality of debugging protocols according to the at least one debug command and converting the debugging information into usb formatted data packets and providing the usb formatted data packets to the usb host independent of whether a usb controller provided outside the eud in the electronic system is communicating with the usb host. 20. the method of claim 19, wherein detecting if the debugging process is permitted in the electronic system comprises detecting a debug disablement fuse in a false state. 21. the method of claim 19, wherein connecting the electronic system to the usb host comprises connecting a usb physical layer (phy) of the electronic system to a personal computer (pc). 22. an embedded universal serial bus (usb) debug (eud)-based test system, comprising: a usb host, comprising a usb host interface and an electronic system, comprising: a usb physical layer (phy) coupled to the usb host over a usb cable and, comprising: a usb hub, comprising: at least one upstream interface at least one first downstream interface communicatively coupled to the at least one upstream interface and a plurality of second downstream interfaces communicatively coupled to the at least one upstream interface at least one multi-protocol debug peripheral coupled to at least one of the plurality of second downstream interfaces, the at least one multi-protocol debug peripheral configured to receive debugging information based on a supported debugging protocol among a plurality of debugging protocols from at least one debug function coupled to the at least one multi-protocol debug peripheral a disconnect switch coupled to the at least one first downstream interface a bypass switch, comprising: a conductive wire a first bypass switch configured to alternately connect to the at least one upstream interface and the conductive wire and a second bypass switch configured to alternately connect to the conductive wire and the disconnect switch an eud power supply coupled to the usb phy and an eud oscillator coupled to the usb phy and a usb controller coupled to the second bypass switch wherein the usb hub in the eud is configured to communicate usb formatted data packets to the usb phy over the at least one upstream interface in response to the first bypass switch being connected to the at least one upstream interface and the disconnect switch being open. 23. the eud-based test system of claim 22, wherein the usb host is a personal computer (pc). 24. the eud-based test system of claim 22, wherein the usb host interface is a usb high-speed interface or a usb super-speed interface. 25. the eud-based test system of claim 22, wherein the usb phy is a usb high-speed interface or a usb super-speed interface. 26. the eud-based test system of claim 22, wherein the at least one multi-protocol debug peripheral is configured to be a debugging control peripheral. 27. the eud-based test system of claim 22, wherein the disconnect switch is a software-based two-way open-close switch or a hardware-based two-way open-close switch. 28. the eud-based test system of claim 22, wherein the disconnect switch is integrated with the at least one first downstream interface. 29. the eud-based test system of claim 22, wherein the first bypass switch and the second bypass switch are three-way switches. 30. the eud-based test system of cl (Results 0)

Search [SP]: background. i. field of the disclosure the technology of the disclosure relates generally to debugging an electronic system. ii.

12: backgroundmobile computing devices have become common in modern society. the prevalence of mobile computing devices may be attributed to the many functions that are enabled within such computing devices. increasingly complex integrated circuits (ics) have been designed and manufactured to provide increasingly greater functionality in mobile computing devices. in some cases, an entire system of a mobile computing device is integrated into a single ic known as a system-on-chip (soc). in some other cases, the entire system of the mobile computing device is supported by multiple ics that are packaged into an integrated module known as system-in-package (sip). ics and mobile computing devices are repeatedly tested and debugged during different phases of their respective development life cycles in an effort to detect and eliminate potential errors before releasing the mobile computing devices to customers. while testing is a process for detecting suspected errors under specific conditions, debugging is a process used to investigate the exact causes of the suspected errors. a de facto debugging approach involves analyzing execution logs obtained under various test conditions from a device under test (dut). in the case of debugging mobile computing devices and the ics therein, established debugging methodologies and tools, such as joint test action group (jtag) logging, serial wire debug (swd), system trace, and universal asynchronous receiver/transmitter (uart) logging, are often employed. each of these debugging methodologies is specifically designed to capture execution loggings under specific conditions from a specific circuit, component, and/or functional block in the dut. as the complexity of the mobile computing devices continues to increase and the size of the ics continues to decrease, testing and debugging are becoming more cumbersome and time consuming. accordingly, designers and developers of mobile computing devices require better testing and debugging tools. summary of the disclosure aspects disclosed in the detailed description include embedded universal serial bus (usb) debug (eud) for multi-interfaced debugging in electronic systems. electronic systems, such as mobile computing devices, contain complex integrated circuits (ics) that require extensive testing and debugging to ensure good quality and performance. in exemplary aspects, an eud is provided in an electronic system. the eud is configured to provide control information and/or collect debugging information from multiple internal debugging interfaces (e.g., joint test action group (jtag), serial wire debug (swd), system trace, universal asynchronous receiver/transmitter (uart), etc.) in the electronic system. the eud converts the debugging information into a usb format so that the debugging information can be externally accessed through a usb interface provided by the electronic system. an exemplary attribute of the eud is that it can provide non-invasive monitoring of the electronic system. the electronic system is still able to use a usb port for communications in a mission mode while the eud is enabled. in addition, the electronic system can still turn on or off all system clocks and transition to and from a power-saving mode, while the eud continues to function. by providing the eud in the electronic system to make multi-interfaced debugging information externally accessible through the usb interface, without impacting normal behavior of the electronic system, testing and debugging can be more easily and efficiently accomplished without requiring multiple connection interfaces from the electronic system. in this regard in one aspect, an embedded eud in an electronic system is provided. the eud comprises a usb hub. the usb hub comprises at least one upstream interface. the at least one upstream interface is coupled to a usb phy in the electronic system. the usb hub also comprises a plurality of downstream interfaces communicatively coupled to the at least one upstream interface. the eud also comprises a debug peripheral coupled to one of the plurality of downstream interfaces. the debug peripheral is configured to exchange usb formatted data packets with the usb hub over the one of the plurality of downstream interfaces. the debug peripheral is communicatively coupled to at least one debug function among a plurality of debug functions in the electronic system to receive debugging information from the at least one debug function. the debug peripheral is configured to convert the debugging information received from the at least one debug function into the usb formatted data packets to be provided to the usb hub. the usb hub is configured to provide the usb formatted data packets to the usb phy over the at least one upstream interface. in another aspect, a method for enabling a debugging process in an electronic system using an eud is provided. the method comprises attaching the electronic system to a usb host. the method also comprises detecting a presence of the usb host by the eud. the method also comprises detecting if the debugging process is permitted in the electronic system by the eud. the method also comprises receiving at least one eud configuration from the usb host. the method also comprises receiving at least one debug command by the eud from the usb host. the method also comprises collecting debugging information according to the at least one debug command. in another aspect, an eud-based test system is provided. the eud-based test system comprises a usb host, comprising usb host interface. the eud-based test system also comprises an electronic system. the electronic system comprises a usb phy coupled to the usb host interface over a usb cable. the electronic system also comprises an eud. the eud comprises a usb hub. the usb hub comprises at least one upstream interface. the usb hub also comprises at least one first downstream interface communicatively coupled to the at least one upstream interface. the usb hub also comprises a plurality of second downstream interfaces communicatively coupled to the at least one upstream interface. the eud also comprises at least one debug peripheral coupled to at least one of the plurality of second downstream interfaces. the eud also comprises a disconnect switch coupled to the at least one first downstream interface. the eud also comprises a bypass switch. the bypass switch comprises a conductive wire. the bypass switch also comprises a first bypass switch configured to alternately connect to the at least one upstream interface and the conductive wire. the bypass switch also comprises a second bypass switch configured to alternately connect to the conductive wire and the disconnect switch. the eud also comprises an eud power supply coupled to the usb phy. the eud also comprises an eud oscillator coupled to the usb phy. the electronic system also comprises at least one debug functions coupled to the at least one debug peripheral. the electronic system also comprises a usb controller coupled to the second bypass switch. in another aspect, an eud in an electronic system is provided. the eud comprises a usb hub. the usb hub comprises at least one upstream interface. the at least one upstream interface is to be coupled to a usb phy in the electronic system. the usb hub also comprises a plurality of downstream interfaces communicatively coupled to the at least one upstream interface. the eud also comprises at least one debug peripheral coupled to at least one of the plurality of downstream interfaces. the at least one debug peripheral is configured to exchange usb formatted data packets with the usb hub over the at least one of the plurality of downstream interfaces. the at least one debug peripheral is communicatively coupled to at least one debug function among a plurality of debug functions in the electronic system to send control information to and/or to receive debugging information from the at least one debug function. the at least one debug peripheral is configured to convert the debugging information received from the at least one debug function into the usb formatted data packets to be provided to the usb hub. the at least one debug peripheral is configured to control the electronic system. the usb hub is configured to provide the usb formatted data packets to the usb phy over the at least one upstream interface. in another aspect, an eud in an electronic system is provided. the means comprises a means for attaching the electronic system to a usb host. the means also comprises detecting a presence of the usb host by the eud. the means also comprises detecting if the debugging process is permitted in the electronic system by the eud. the means also comprises receiving at least one eud configuration by the eud from the usb host. the means also comprises receiving at least one debug command by the eud from the usb host. the means also comprises collecting debugging information according to the at least one debug command. brief description of the figures fig. 1 is a block diagram of a conventional configuration of a debugging system for testing and debugging an electronic system that may benefit from exemplary aspects of the present disclosure fig. 2 is a schematic diagram of an exemplary embedded universal serial bus (usb) debug (eud) configured to send control information to or collect debugging information from at least one debug function inside an electronic system and convert the debugging information into usb formatted data packets that can be externally accessed through a usb interface fig. 3 is a schematic diagram of an exemplary eud-based test system configured to send control infor (Results 17)

Search fn=(62992334 or 65759845 or 32459363 or 46422614 or 50119245 or 47450766 or 51298816 or 51935663 or 51935663 or 51935663 or 30541931 or 28223722 or 34891741 or 43218499 or 45918370 or 51087282 or 49914482 or 63036433) (Results 16)

Search [SP]: embedded universal serial bus (usb) debug (eud) for multi-interfaced debugging in electronic systems embedded universal serial bus (usb) debug (eud) for multi-interfaced debugging in electronic systems are disclosed. electronic systems contain complex integrated circuits (ics) that require extensive testing and debugging to ensure good quality and performance. in exemplary aspects, an eud is provided in an electronic system. the eud is configured to send control information to and/or collect debugging information from multiple internal debugging interfaces in the electronic system. the eud is also configured to convert the debugging information into a usb format so that the debugging information can be externally accessed through a usb interface provided by the electronic system. the eud can provide non-invasive monitoring of the electronic system. the electronic system is able to use a usb port for communications in a mission mode while eud is enabled. additionally, the electronic system can turn on or off all system clocks during power-saving mode while the eud continues to function. (Results 17)

Search 14 and PD<20141030 (Results 13)
15:

Title: DATA PROCESSING SYSTEM HAVING AN ON-CHIP BACKGROUND DEBUG SYSTEM AND METHOD THEREFOR

Abstract: Embodiments of the present invention relate to a mechanism to prevent the oscillator from being stopped when a host development system is coupled to the background debug communications interface and the background debug mode has been enabled. This allows background debugging operations to continue when the target data processing system is in a low power mode. Other embodiments relate to a mechanism for allowing a host development system to request a synchronization timing pulse from a target data processing system so the correct clock speed can be determined for background communications. Alternate embodiments relate to a data processing system having a system clock unit and a background debug system where the background debug system includes a background debug clock unit, separate from the system clock unit, and an enable control. When the enable control is asserted, the background debug clock unit is enabled, independent of the system clock unit.

Classifications:

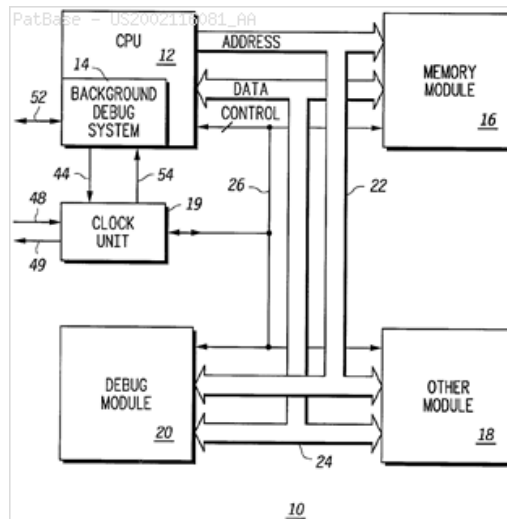
International (ipc 8-9): G05B19/42 G06F1/04 G06F1/32 G06F11/00 G06F11/36 H02H3/05 H03K19/003 (Advanced/Invention); G06F11/36 (Advanced/Non-invention); G05B19/42 G06F1/04 G06F1/32 G06F11/00 G06F11/36 H02H3/05 H03K19/003 (Core/Invention)

International (ipc 1-7): G05B19/42 G06F1/04 G06F1/32 G06F11/00 G06F11/36 H02H3/05 H03K19/003

CPC: G06F11/348 Y02D10/34

European: G06F11/34T6

US: 700/87 700/87P 714/3.8 714/30 714/38 714/38.1 717/124



Family:

Publication number	Publication date	Application number	Application date
AU2002227439 AA	20020912	AU20020227439	20011218
CN1543604 A	20041103	CN20018022793	20011218
CN1543604 B	20120530	CN20018022793	20011218
EP1423789 A2	20040602	EP20010996290	20011218
JP2005508531 T2	20050331	JP20020568201T	20011218
JP4145146 B2	20080903	JP20020568201T	20011218
KR100819720 B1	20080407	KR20037010937	20011218
KR20030075202 A	20030922	KR20037010937	20011218
TW533350 B	20030521	TW20010131692	20011220
US2002116081 AA	20020822	US20010788816	20010221
US6823224 BB	20041123	US20010788816	20010221
WO02069146 A2	20020906	WO2001US49157	20011218
WO02069146 A3	20040408	WO2001US49157	20011218

Priority:

US20010788816 20010221 WO2001US49157 20011218 WO2001US49157 20030820

Probable Assignee: FREESCALE SEMICONDUCTOR INC

Assignee(s): (std): MOTOROLA INC ; SIBIGTROTTH JAMES M ; WOOD MICHAEL C ; FREESCALE SEMICONDUCTOR INC

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC ; NXP USA INC ; NORTH STAR INNOVATIONS INC ; NXP BV ; NXP F K A FREESCALE SEMICONDUCTOR INC BV ; BAKER GEORGE E ; CITIBANK NA AS COLLATERAL AGENT ; CITIBANK NA COLLATERAL AGENT AS ; CITIBANK NA NOTES COLLATERAL AGENT AS

Inventor(s): (std): BAKER GEORGE E ; BAKER GEORGE E WOOD MICHAEL C ; SIBIGTROTTH JAMES M ; WOOD MICHAEL C ; MICHAEL C WOOD ; JAMES M SIBIGTROTTH ; GEORGE E BAKER

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PH PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW

Title: Serial bus diagnostic port of a digital system

Abstract: A digital system provides a serial bus diagnostic port such as, for example, a universal serial bus (USB) diagnostic port. The USB diagnostic port can include a USB slave device operable to interface to a universal serial bus, a flash memory controller interface coupled to the USB slave device and operable to interface to a flash memory controller, and a test access port controller coupled to the USB slave device and operable to interface to an integrated controller independently of an operating system. Via the diagnostic port, a USB testing tool with testing software can access and debug internal logic of the digital system. As an alternative to a USB diagnostic port, the serial bus diagnostic port can be implemented in a variety of wired or wireless implementations such as, for example, an I.E.E.E. 1394 diagnostic port, an Ethernet diagnostic port, or a wireless Internet diagnostic port. Further, the serial bus diagnostic port can, for example, be used for software development, in-factory testing or in-field diagnostics of the digital system.

Classifications:

International (IPC 8-9): G06F11/267 H02H3/05 (Advanced/Invention);
G06F11/267 H02H3/05 (Core/Invention)

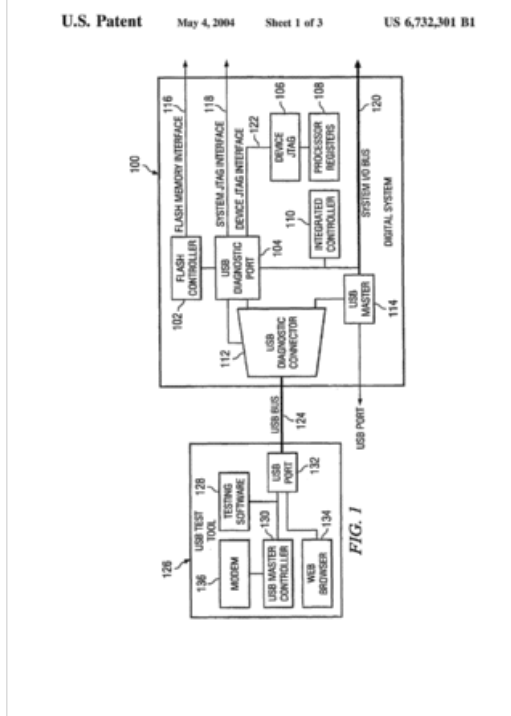
International (IPC 1-7): H02H3/05

CPC: G06F11/267

European: G06F11/267

US: 710/110 714/43 714/E11.16

PatBase - US6732301_BA



Family:

Publication number	Publication date	Application number	Application date
US6732301 BA	20040504	US20000519443	20000306

Priority:

US20000519443 20000306

Probable Assignee: HEWLETT PACKARD DEVELOPMENT CO LP

Assignee(s): (std): HEWLETT PACKARD DEVELOPMENT CO

Assignee(s): HEWLETT PACKARD DEVELOPMENT CO LP ; HEWLETT PACKARD DEVELOPMENT COMPANY L P ;
COMPAQ INFORMATION TECHNOLOGIES GROUP LP

Inventor(s): (std): DIEHL WILLIAM W ; LANDRY JOHN A

Title: DEBUG SYSTEM AND METHOD FOR EQUIPMENT HAVING POWER SAVING FUNCTION OF CPU

Abstract: PROBLEM TO BE SOLVED: To provide the debug system of equipment having the power saving function of a CPU for continuing debug even when the CPU of a debug target is shifted to a power saving state. SOLUTION: A debug target 101 is provided with a power saving mode detecting means 104, and connected to a debugger 102. A debug function 103 is operated on the debug target 101, and connected to the external debugger 102. Communication between the debugger 102 and the debug function 103 is provided with a time-out time, and when the debug target 101 is turned into a power saving state, the communication between the debugger 102 and the debug function 103 is timed out. The power saving state is detected by a power saving mode detecting means 104, and the power saving mode can be discriminated from communication failure between the debugger 102 and the debug function 103 due to runaway. When the power saving function is functioning on the debug target 101, the communication is not timed out, so that the continuation of debug can be attained.

Classifications:

International (IPC 8-9): G06F1/32 G06F11/30 (Advanced/Invention);
G06F1/32 G06F11/30 (Core/Invention)

International (IPC 1-7): G06F11/30

CPC: Y02D10/34

PatBase - JP2005293077_A2

(5)

特開2005-293077 (JP2005-293077A)

。もし、Hであれば(5-4-3)、デバッグ・ターゲット501の構成などが考えられ、
エラー処理を行う(5-4-4)。エラー処理としては、表示装置513にエラーメッセ-
ジを表示する等である。もし、Lであれば、停電モードを判定して、通信動作のタイ-
ムを減らすまで、つまりHになるまでポーリングし続け、状態の確認を続ける(5-4-5)。

【図面の簡単な説明】

【0001】

【0002】本発明の構成図である。

【0003】本発明の第1実施形態の構成図である。

【0004】デバッグ・ターゲットの動作状態の遷移図である。

【0005】デバッグのタイムアウト発生時の動作を示すフローチャートである。

【0006】本発明の第2実施形態の構成図である。

【符号の説明】

【0007】

101 デバッグ・ターゲット

102 デバッガ

103 デバッグ機能

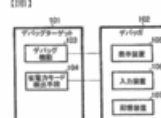
104 停電モード検出手段

105 表示装置

106 入力装置

107 記憶装置

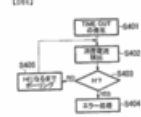
【0008】



【0009】



【0010】

**Family:**

Publication number	Publication date	Application number	Application date
JP2005293077 A2	20051020	JP20040105434	20040331
JP4479002 B2	20100609	JP20040105434	20040331

Priority:

JP20040105434 20040331

Probable Assignee:

NEC CORP

Assignee(s): (std):

NEC CORP

Inventor(s): (std):

FUJII SATORU

Title: DEBUG SUPPORT DEVICE, AND PROGRAM FOR DIRECTING COMPUTER TO PERFORM DEBUGGING METHOD

Abstract: A debug support device for debugging a multiprocessor configured by a plurality of unit processors includes a unit processor stop section realized by a plurality of the unit processors executing a program for each of the threads, and any one of the plurality of unit processors performing a process of stopping a unit processor executing a thread in which exception handling occurs together with unit processors executing other threads when the exception handling of software occurs by a break point of a part of the plurality of threads; and a debugging execution section for performing a debugging process of detecting information about a state of the plurality of unit processors stopped by the unit processor stop section.

Classifications:

International (IPC 8-9): G06F11/00 G06F11/28 G06F11/36 G06F9/46
G09F11/00 (Advanced/Invention);

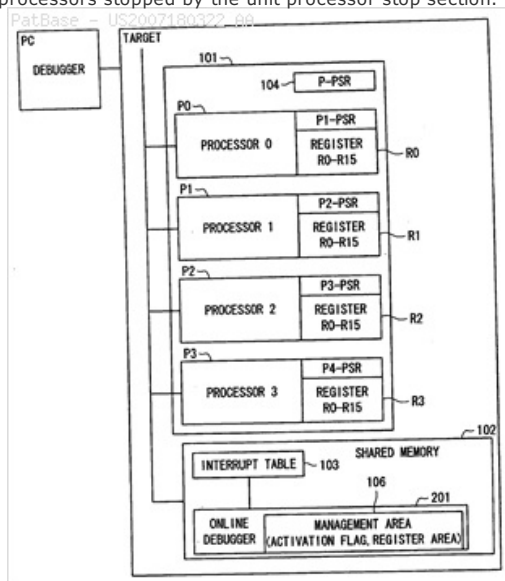
G06F11/28 G06F11/36 G06F9/46 (Advanced/Non-invention);

G06F11/00 G06F11/28 G06F11/36 G06F9/46 (Core/Invention)

CPC: G06F11/362

European: G06F11/36B

US: 712/227 714/34 714/34P 714/35 714/E11.207 714/E11.207S



Family:

Publication number	Publication date	Application number	Application date
CN101213523 A	20080702	CN200780000076	20070111
EP1855205 A1	20071114	EP20070706614	20070111
EP1855205 A4	20100428	EP20070706614	20070111
JP2007188147 A2	20070726	JP20060003529	20060111
JP4222370 B2	20090212	JP20060003529	20060111
KR20070091047 A	20070906	KR20077018139	20070807
US2007180322 AA	20070802	US20070651549	20070110
US7992042 BB	20110802	US20070651549	20070110
WO07080931 A1	20070719	WO2007JP50267	20070111

Priority:

JP20060003529 20060111 WO2007JP50267 20070111

Probable Assignee: SEIKO EPSON CORP

Assignee(s): (std): SEIKO EPSON CORP

Inventor(s): (std): AKINARI TODOROKI ; KATSUYA TANAKA ; TANAKA KATSUYA ; TODOROKI AKINARI ; TODOROKI MITSUNARI

Agent(s): NAITOH YOSHIKI; MORI TETSUYA; OLIFF AND BERRIDGE PLC

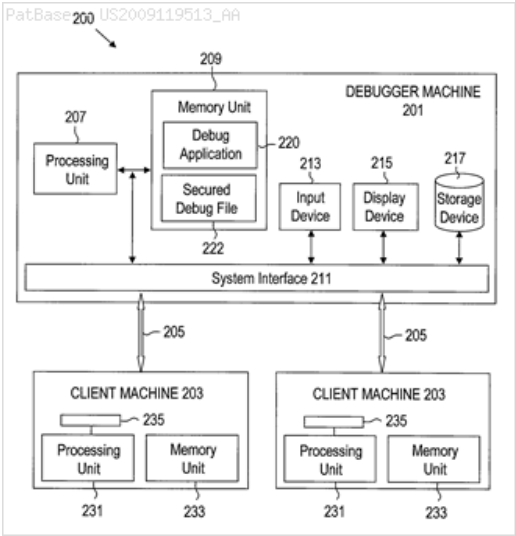
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Title: METHOD AND SYSTEM FOR REMOTELY DEBUGGING A FAILED COMPUTER MACHINE

Abstract: A method for conducting a remote debugging session comprises setting a secure connection link with a failed client machine, receiving status information from the client machine through the connection link in response to a debug instruction sent to the client machine, displaying the status information in a readable form, requesting a user to enter a cryptographic key in response to a request for saving the status information, and generating a secured file containing the status information encrypted with the cryptographic key.

Classifications:

International (IPC 8-9): G06F11/28 G06F11/30 G06F12/14 H04L12/24 H04L9/32 (Advanced/Invention); G06F12/14 (Core/Invention)
CPC: G06F11/362 G06F2221/2101
European: G06F11/36B S06F221/2101 S06F221/2107
US: 713/187 713/187P 713/193



Family:

Publication number	Publication date	Application number	Application date
TW200921372 A	20090516	TW20080104001	20080201
TWI377467 B	20121121	TW20080104001	20080201
US2009119513 AA	20090507	US20070934690	20071102
US8205095 BB	20120619	US20070934690	20071102

Priority:

US20070934690 20071102

Probable Assignee:

NVIDIA CORP

Assignee(s): (std):

CHUNG CHIEN CHUNG ; NVIDIA CORP

Inventor(s): (std):

CHUNG CHIEN CHUNG

Agent(s):

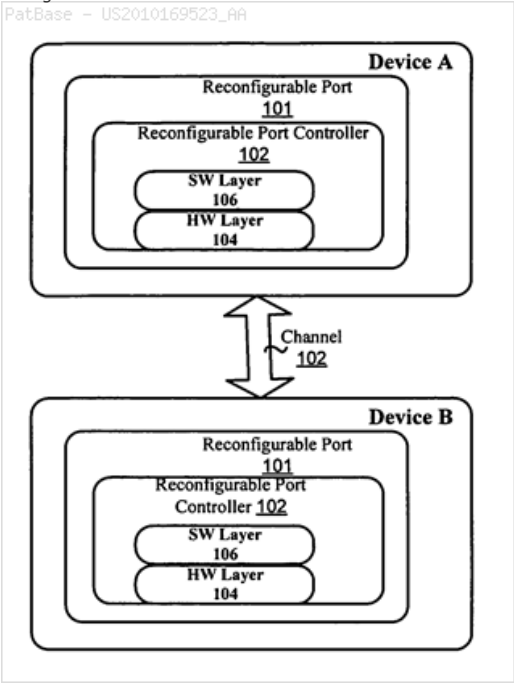
PATTERSON AND SHERIDAN LLP

Title: SCALABLE METHOD AND APPARATUS TO CONFIGURE A LINK

Abstract: Disclosed herein are reconfigurable ports and methods for doing the same.

Classifications:

International (IPC 8-9): G06F11/22 G06F11/267 G06F13/00 G06F13/38 G06F13/42 G06F3/00 G06F9/44 (Advanced/Invention); G06F13/42 (Advanced/Non-invention); G06F13/00 (Core/Invention); G06F13/42 (Core/Non-invention)
CPC: G06F9/4411 G06F13/387 G06F13/4282 G06F11/2289 G06F11/267 G06F13/385
European: G06F13/38A2
US: 710/104 710/104P 710/105 710/105S 710/106 710/12 710/8



Family:

Publication number	Publication date	Application number	Application date
US2010169523 AA	20100701	US20090454155	20090513
US2013046908 AA	20130221	US20120655916	20121019
US2016062934 AA	20160303	US20150709249	20150511
US8296469 BB	20121023	US20090454155	20090513
US9032105 BB	20150512	US20120655916	20121019

Priority:

US20080196719P 20081231 US20090454155 20090513 US20120655916 20121019
US20150709249 20150511

Probable Assignee: INTEL CORP

Assignee(s): (std): BHATT AJAY ; DUNSTAN ROBERT ; INTEL CORP ; QUIET DUANE

Inventor(s): (std): BHATT AJAY ; DUNSTAN ROBERT ; QUIET DUANE

Agent(s): INTEL C O CPA GLOBAL CORP; INT IP LAW GROUP PLLC

Title: AUTHENTICATED DEBUG ACCESS FOR FIELD RETURNS

Abstract: Under the direction of a first party, an integrated circuit (IC) device is configured to temporarily enable access to a debug interface of the IC device via authentication of the first party by a challenge/response process using a key of the IC device and a challenge value generated at the IC device. The first party then may conduct a software evaluation of the IC device via the debug interface. In response to failing to identify an issue with the IC device from the software evaluation, the first party can permanently enable open access to the debug interface while authenticated and provide the IC device to a second party. Under the direction of the second party, a hardware evaluation of the IC device is conducted via the debug interface that was permanently opened by the first party.

Classifications:

International (IPC 8-9): G06F11/36 G06F21/00 G06F21/22

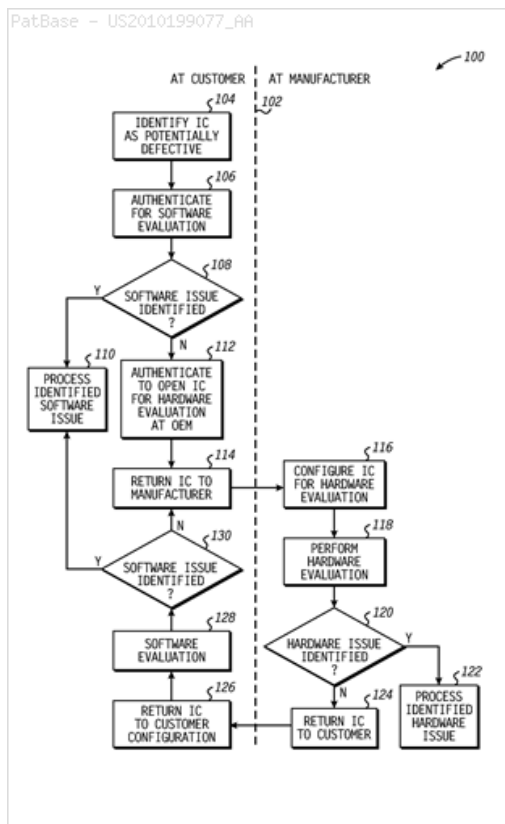
G06F21/44 G06F9/00 H04L9/32 (Advanced/Invention);

G06F11/36 G06F21/00 G06F9/00 (Core/Invention)

CPC: H04L9/3247 H04L9/3271 G06F11/3656

European: G06F11/36B7H

US: 713/1 713/168 713/182 713/182S 713/185 713/1P 726/2



Family:

Publication number	Publication date	Application number	Application date
CN102301375 A	20111228	CN201080006319	20100113
CN102301375 B	20140910	CN201080006319	20100113
EP2391969 A2	20111207	EP20100736189	20100113
EP2391969 A4	20120627	EP20100736189	20100113
EP2391969 B1	20170802	EP20100736189	20100113
KR101587309 B1	20160120	KR20117020042	20100113
KR20110114687 A	20111019	KR20117020042	20100113
US2010199077 AA	20100805	US20090363259	20090130
US8332641 BB	20121211	US20090363259	20090130
WO10088043 A2	20100805	WO2010US20855	20100113
WO10088043 A3	20100923	WO2010US20855	20100113

Priority:

US20090363259 20090130 WO2010US20855 20100113

Probable Assignee: NXP USA INC

Assignee(s): (std): MUIR ALISTAIR N ; HARTLEY DAVID H ; MACKIE TROY E ; COVEY CARLIN R ; FREESCALE SEMICONDUCTOR INC ; ASHKENAZI ASAF ; CASE LAWRENCE L ; CHHABRA RUCHIR ; VAGLICA JOHN J ; TKACIK THOMAS E ; ZIOLKOWSKI RODNEY D ; REDMAN MARK D ; NXP USA INC

Assignee(s): NXP BV ; NXP F K A FREESCALE SEMICONDUCTOR INC BV ; CITIBANK NA ; CITIBANK NA NOTES COLLATERAL AGENT AS ; MORGAN STANLEY SENIOR FUNDING INC

Inventor(s): (std): ASHKENAZI ASAF ; CASE LAWRENCE L ; CHHABRA RUCHIR ; COVEY CARLIN R ; HARTLEY DAVID H ; MACKIE TROY E ; MUIR ALISTAIR N ; REDMAN MARK D ; TKACIK THOMAS E ; VAGLICA JOHN J ; ZIOLKOWSKI RODNEY D

Agent(s): FERRO FRODO NUNES; FREESCALE LAW DEPARTMENT EMEA PATENT OPS; LARSON NEWMAN AND ABEL LLP; KING ROBERT L ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: BUFFERED CROSSBAR SWITCH SYSTEM

Abstract: Described embodiments provide for transfer of data between data modules. At least two crossbar switches are employed, where input nodes and output nodes of each crossbar switch are coupled to corresponding data modules. The i th crossbar switch has an N_i -input by M_i -output switch fabric, wherein N_i and M_i are positive integers greater than one. Each crossbar switch includes an input buffer at each input node, a crosspoint buffer at each crosspoint of the switch fabric, and an output buffer at each output node. The input buffer has an arbiter that reads data packets from the input buffer according to a first scheduling algorithm. An arbiter reads data packets from a crosspoint buffer queue according to a second scheduling algorithm. The output node receives segments of data packets provided from one or more corresponding crosspoint buffers.

Classifications:

International (IPC 8-9): G06F11/30 G06F12/00 G06F12/02
G06F12/06 G06F12/08 G06F12/14 G06F13/00 G06F13/14 G06F13/36
G06F13/38 G06F15/00 G06F15/167 G06F15/173 G06F15/76
G06F15/78 G06F17/00 G06F17/30 G06F7/00 G06F7/38 G06F7/68
G06F9/00 G06F9/02 G06F9/26 G06F9/30 G06F9/312 G06F9/38
G06F9/44 G06F9/455 G06F9/46 G06F9/48 G06F9/52 G06F9/54
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H04Q3/00 (Advanced/Invention);
G06F12/08 H04L12/861 H04L12/863 H04L12/931
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G06F13/00 H04L12/28 H04L12/56 (Core/Non-invention)

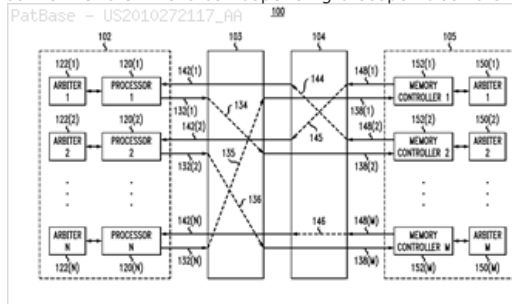
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European: G06F12/02D2 G06F12/02D4 G06F12/08B2 G06F12/08B4P4 G06F12/08B4S G06F12/08B4T G06F12/08B6
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Family:

Publication number	Publication date	Application number	Application date
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Probable Assignee: LSI CORP

Assignee(s): (std): HASTING JOSEPH ; KING LARRY ; HAKAMI MOHAMMED REZA ; LSI CORP ; POLLOCK STEVEN ; MITAL DEEPAK ; MUNOZ ROBERT J ; MA TE KHAC ; NEMAWARKAR SHASHANK ; PEET JR CHARLES EDWARD ; MANZELLA JOSEPH A ; MANGIONE MICHAEL T ; PEET JR CHARLES EDWARDS ; PEACHEY RITCHIE J ; SONNIER DAVID P ; SUNDARARAMAN BALAKRISHNAN ; VANGATI NARENDER R ; VANGATI NARENDER ; PIROG JERRY ; SONNIER DAVID ; VESTAL ALLEN ; PEKCAN HAKAN I ; POLLOCK STEVEN J ; VORA NILESH S ; STONE CHRIS RANDALL ; ROSIN EYAL ; ROPER WALTER A ; WU EPHREM ; ZHOU TING ; INTEL CORP ; BURROUGHS WILLIAM G ; BURROUGHS WILLIAM ; FLOOD RACHEL ; CLEE JAMES T ; CLEE JAMES ; DOSH ERAN ; AGERE SYSTEMS LLC ; AULAKH SHAILENDRA ; BETKER MICHAEL ; BETKER MICHAEL R ; BROWN DAVID ; BROWN DAVID A

Assignee(s): DEUTSCHE BANK NEW YORK BRANCH COLLATERAL AG AS ; IP LEGAL SERVICES

Inventor(s): (std): EPHREM WU ; POLLACK STEVEN ; STEVEN POLLOCK ; TING ZHOU ; VORA NILESH S ; VESTAL ALLEN ; VANGATI NARENDER R ; VANGATI NARENDER ; SUNDARARAMAN BALAKRISHNAN ; STONE CHRIS RANDALL ; SONNIER DAVID P ; SONNIER DAVID ; ROSIN EYAL ; ROPER WALTER A ; POLLOCK STEVEN J ; PIROG JERRY ; PEKCAN HAKAN I ; PEET JR CHARLES EDWARDS ; PEET JR CHARLES EDWARD ; PEACHEY RITCHIE J ; NEMAWARKAR SHASHANK ; MUNOZ ROBERT J ; MITAL DEEPAK ; MANZELLA JOSEPH A ; MANGIONE MICHAEL T ; MA TE KHAC ; KING LARRY ; HASTING JOSEPH R ; HASTING JOSEPH ; HAKAMI MOHAMMED REZA ; HAKAMI MOHAMMAD REZA ; GUO ZHONG ; FLOOD RACHEL ; DOSH ERAN ; CLEE JAMES T ; CLEE JAMES ; BURROUGHS WILLIAM G ; BURROUGHS WILLIAM ; BROWN DAVID A ; BROWN DAVID ; BETKER MICHAEL R ; BETKER MICHAEL ; AULAKH SHAILENDRA ; ZHOU TING ; WU EPHREM ; POLLOCK STEVEN

Agent(s): WILLIAMS DAVID JOHN; RUMMLER FELIX; OKABE YUZURU; KATO NOBUAKI; ASAHINO BUMITSU; IP LEGAL SERVICES; SMITH RISLEY TEMPEL SANTOS LLC; DANIEL J; NICHOLSON DE VOS WEBSTER AND ELLIOTT LLP

Designated states: AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

Title: DATA PROCESSING APPARATUS AND RELATED METHODS OF DEBUGGING PROCESSING CIRCUITRY

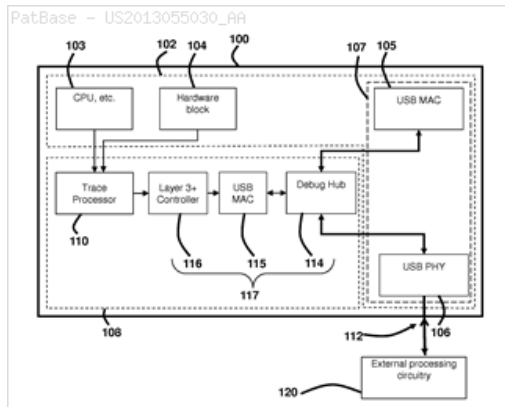
Abstract: A data processing apparatus, comprising processing circuitry, which in use, generates data and debug circuitry arranged to debug operation of the processing circuitry. The processing circuitry includes bus circuitry arranged to pass data at least one of into and out of the processing apparatus over a communication bus. The debug circuitry comprises monitoring circuitry arranged to monitor the data generated, in use, by the processing circuitry and generate a stream of trace elements. An interface unit is arranged to interface, using the bus circuitry, the trace elements generated by the monitoring circuitry onto the communication bus to be output, in use, from the processing apparatus using the communication bus. The interface unit comprises a controller which is arranged to control operation of the interface unit independently of the operation of the processing circuitry.

Classifications:

International (IPC 8-9): G06F11/07 G06F11/273 G06F11/30 G06F11/34 G06F11/36 (Advanced/Invention)

CPC: G06F11/364 G06F11/3466 G06F11/3636 G06F11/348 G06F11/3656

US: 714/27 714/30 714/37 714/39 714/45 714/E11.024

**Family:**

Publication number	Publication date	Application number	Application date
GB201114715 A0	20111012	GB20110014715	20110825
GB201208613 A0	20120627	GB20120008613	20120516
GB2489838 A1	20121010	GB20120008613	20120516
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US8826081 BB	20140902	US20120690923	20121130

Priority:

GB20110014715 20110825 US20110244023 20110923 GB20120008613 20120516
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Probable Assignee: ULTRASOC TECHNOLOGIES LTD

Assignee(s): (std): BARLOW STEPHEN JOHN ; HOPKINS ANDREW BRIAN THOMAS ; KRASIC CONSTANTINE ; ULTRASOC TECHNOLOGIES LTD

Inventor(s): (std): BARLOW STEPHEN JOHN ; HOPKINS ANDREW BRIAN THOMAS ; KRASIC CONSTANTINE

Inventor(s): STEPHEN JOHN BARLOW ; CONSTANTINE KRASIC ; ANDREW BRIAN THOMAS HOPKINS

Agent(s): FENWICK AND WEST LLP

Title: NON-INTRUSIVE DEBUGGING FRAMEWORK FOR PARALLEL SOFTWARE BASED ON SUPER MULTI-CORE FRAMEWORK

Abstract: A non-intrusive debugging framework for parallel software based on a super multi-core framework is composed of a plurality of core clusters. Each of the core clusters includes a plurality of core processors and a debug node. Each of the core processors includes a DCP. The DCPs and the debug node are interconnected via at least one channel to constitute a communication network inside each of the core clusters. The core clusters are interconnected via a ring network. In this way, the memory inside each of the debug nodes constitutes a non-uniform debug memory space for debugging without affecting execution of the parallel program, such that it is applicable to current diversified dynamic debugging methods under the super multi-core system.

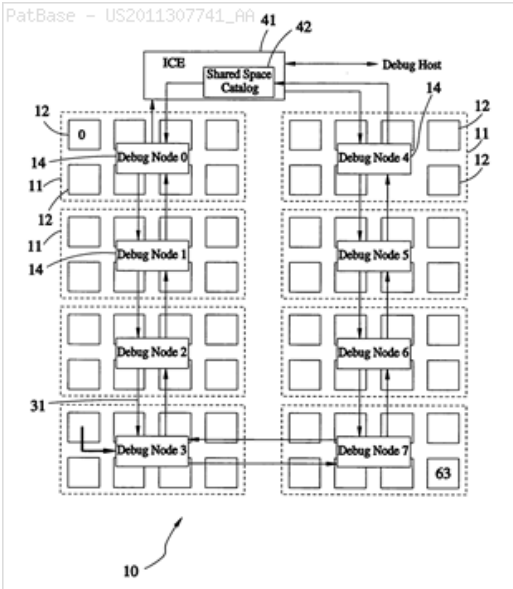
Classifications:

International (IPC 8-9): G06F11/36 (Advanced/Invention)

CPC: G06F11/3636 G06F11/3648

European: G06F11/36B5 G06F11/36B7

US: 714/38.1 714/38.100P 714/E11.208 714/E11.208S



Family:

Publication number	Publication date	Application number	Application date
TW201145016 A	20111216	TW20100119529	20100615
US2011307741 AA	20111215	US20100923913	20101014

Priority:

TW20100119529 20100615

Probable Assignee: NATIONAL CHUNG CHENG UNIV

Assignee(s): (std): CHEN TIEN FU ; CHOU SHU HSUAN ; HSU YEN LAN ; NAT UNIV CHUNG CHENG ; WEN CHE NENG

Assignee(s): NATIONAL CHUNG CHENG UNIV ; NATIONAL CHUNG CHENG UNIVERSITY

Inventor(s): (std): CHEN TIAN FU ; CHEN TIEN FU ; CHOU SHU HSUAN ; HSU YEN LAN ; WEN CHE NENG ; WEN QI NENG ; XU YAN LAN ; ZHOU SHU XUAN

Title: PROGRAMMABLE INPUT/OUTPUT CIRCUIT

Abstract: A apparatus, having a processing system and an input buffer coupled with both the processing system and one of two IO pads, and a reference buffer coupled to both the input buffer and the second of the IO pads such that the reference generator controls the input threshold of the input buffer in response to an analog voltage received from an external circuit on the second of the IO pads.

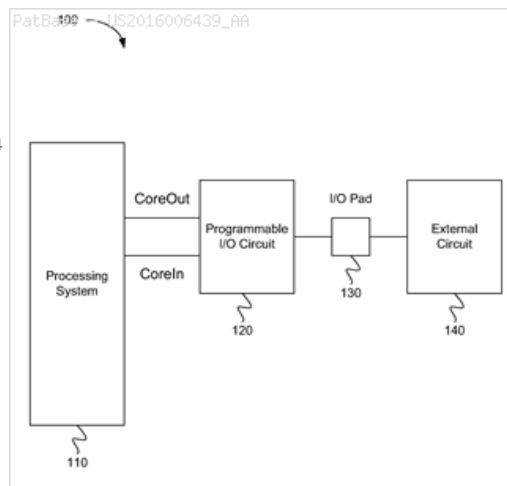
Classifications:

International (IPC 8-9): G01R31/317 G01R31/3177 G06F12/02 G06F13/28 G06F5/06 G11C16/10 G11C7/10 H03K19/0175 H03K19/094 H03K19/173 (Advanced/Invention); G06F13/40 (Advanced/Non-invention)

CPC: G06F13/4072 G06F13/28 H03K19/017581 G06F12/0246 G11C16/102 G06F2212/7201 G06F5/065 H03K19/01759 G11C7/1084 G11C7/1057 G01R31/3177 G01R31/31721 H03K19/173

European: H03K19/0175R

US: 1/1 326/38 326/82 326/83 326/86 327/109 327/112 710/302

**Family:**

Publication number	Publication date	Application number	Application date
US2016006439 AA	20160107	US20150690106	20150417
US2017194963 AA	20170706	US20160369674	20161205
US8179161 BA	20120515	US20100753657	20100402
US8487655 BA	20130716	US20100774680	20100505
US8558578 BA	20131015	US20120427264	20120322
US9013209 BA	20150421	US20130054657	20131015
US9143134 BA	20150922	US20130916386	20130612
US9515659 BB	20161206	US20150690106	20150417
US9952282 BA	20180424	US20150860515	20150921

Priority:

US20090175586P 20090505	US20090175856P 20090506	US20090176933P 20090510
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Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): CYPRESS SEMICONDUCTOR CORP ; HASTINGS MARK ; KOHAGEN NATHAN ; MAR MONTE ; KUTZ HAROLD ; SHUTT JAMES ; THIAGARAJAN EASHWAR ; SNYDER WARREN S ; SEGUINE DENNIS ; SULLAM BERT ; WILLIAMS TIMOTHY ; WRIGHT DAVID G ; VERGE GREGORY J ; WILLIAMS TIMOTHY J ; BYRKETT BRUCE ; BYRKETT BRUCE E

Assignee(s): CYPRESS SEMICONDUCTOR A OF DELAWARE CORP ; MORGAN STANLEY SENIOR FUNDING INC ; MORGAN STANLEY SENIOR FUNDING INC COLLATERAL AGENT AS

Inventor(s): (std): BYRKETT BRUCE ; BYRKETT BRUCE E ; HASTINGS MARK ; HASTINGS MARK E ; KOHAGEN NATHAN ; KOHAGEN NATHAN WAYNE ; KUTZ HAROLD ; KUTZ HAROLD M ; MAR MONTE ; SEGUINE DENNIS ; SEGUINE DENNIS R ; SEGUINE DENNIS RAYMOND ; SHUTT JAMES ; SHUTT JAMES H ; SNYDER WARREN S ; SULLAM BERT ; SULLAM BERT S ; THIAGARAJAN EASHWAR ; VERGE GREGORY J ; VERGE GREGORY JOHN ; WILLIAMS TIMOTHY ; WILLIAMS TIMOTHY J ; WILLIAMS TIMOTHY JOHN ; WRIGHT DAVID G

Title: DEBUG STATE MACHINES AND METHODS OF THEIR OPERATION

Abstract: Embodiments include methods for performing various operations in a computing system that includes an electronic module and a debug circuit. The method includes programming the debug circuit to monitor for pre-selected triggers produced by the computing system, and to perform actions in response to detecting the pre-select triggers. For example, in response to various pre-selected triggers, the debug circuit may, among other things: perform state transitions and log information indicating whether or not the state transitions were performed; monitor various signals when the debug circuit has determined that a test escape has occurred; and/or perform one or more actions that initiate stopping one or more clocks in response to certain pre-selected triggers.

Classifications:

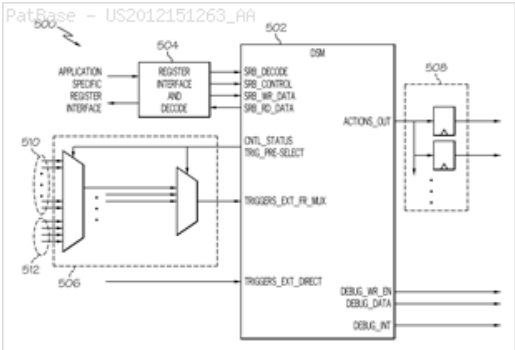
International (IPC 8-9): G06F11/00 G06F11/22

G06F11/267 (Advanced/Invention)

CPC: G06F11/267 G06F11/22

European: G06F11/267

US: 714/30 714/30P 714/34 714/E11.147 714/E11.147S



Family:

Publication number	Publication date	Application number	Application date
US2012151263 AA	20120614	US20110095627	20110427
US9037911 BB	20150519	US20110095627	20110427

Priority:

US20100421501P 20101209 US20110095627 20110427

Probable Assignee: ADVANCED MICRO DEVICES INC

Assignee(s): (std): ADVANCED MICRO DEVICES INC ; KOMMRUSCH STEVEN J ; NIXON SCOTT ; RENTSCHLER ERIC M

Inventor(s): (std): RENTSCHLER ERIC M ; NIXON SCOTT ; KOMMRUSCH STEVEN J

Agent(s): PARK VAUGHAN FLEMING AND DOWLER LLP

Title: DEBUG ARCHITECTURE

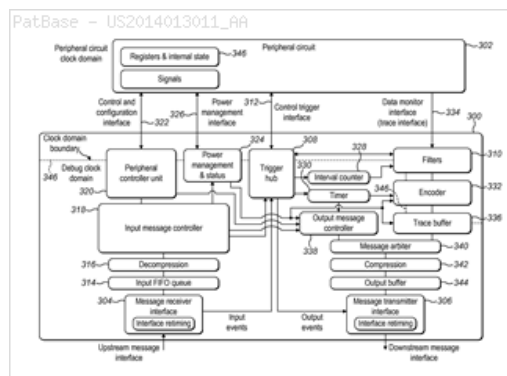
Abstract: Roughly described, an integrated circuit chip comprises a plurality of peripheral circuits, each peripheral circuit connected to a respective debug unit; a shared hub; and between each respective debug unit and the shared hub, a single physical interface configured to transport both configuration data and event data, wherein the interface is configured such that if an event occurs whilst the interface is transporting configuration data, the interface interrupts the transport of the configuration data in order to transport the event data.

Classifications:

International (IPC 8-9): G01R31/28 G01R31/317 G06F1/24 G06F1/26 G06F1/30 G06F1/32 G06F11/00 G06F11/22 G06F11/263 G06F11/267 G06F11/27 G06F11/34 G06F11/36 G06F12/00 G06F13/40 G06F21/44 G06F21/62 G06F21/70 G06F21/85 G06F3/00 G06F9/44 G11C7/00 H04L29/12 (Advanced/Invention); B01J23/04 B01J38/48 G06F11/34 G06F11/36 G06F12/14 G06F15/78 (Advanced/Non-invention)

CPC: G06F9/4411 G06F21/70 G06F13/404 G06F13/4022 H04L61/6004 H04L47/2408 H04L47/245 G06F11/3466 G06F15/7807 G06F11/2205 B01J23/04 B01J38/485 G06F11/3632 G06F11/3656 G06F1/24 G06F1/30 G06F1/32 G06F1/3203 G06F1/3206 G06F1/3234 G06F1/3246 G06F1/325 G06F1/3287 G06F11/263 G06F11/267 G06F11/36 G06F11/362 G06F11/3636 G06F11/3648 G01R31/31721 G06F1/26 G01R31/2884 G01R31/31719 G01R31/31705 G06F11/348 G06F21/44 G06F21/62 G06F21/85 G06F2201/835 G06F2201/86 G06F2201/88

US: 1/1 710/14 710/8 713/330 714/30 714/32 714/724 714/733 726/17

**Family:**

Publication number	Publication date	Application number	Application date
GB201212175 A0	20120822	GB20120012175	20120709
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GB2503881 B2	20140618	GB20120012178	20120709
GB2503882 A1	20140115	GB20120012179	20120709
GB2503882 B2	20140702	GB20120012179	20120709
US2014013011 AA	20140109	US20130938046	20130709
US2014013145 AA	20140109	US20130938077	20130709
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US2014013172 AA	20140109	US20130938088	20130709
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WO14009323 A3	20140417	WO2013EP64407	20130708

Priority:

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Probable Assignee: ULTRASOC TECHNOLOGIES LTD

Assignee(s): (std): ULTRASOC TECH LTD ; ULTRASOC TECHNOLOGIES LTD

Inventor(s): (std): BANERJEE ARNAB ; BARLOW STEPHEN JOHN ; HOPKINS ANDREW BRIAN THOMAS ; MCDONALD MAIER KLAUS DIETER

Inventor(s): STEPHEN JOHN BARLOW ; ANDREW BRIAN THOMAS HOPKINS ; ARNAB BANERJEE ; KLAUS DIETER MCDONALD MAIER

Agent(s): WARREN S; HAYNES DEFFEL AND WOLFELD LLP; HAYNES BEFFEL AND WOLFELD LLP; DEBORAH L; SLINGSBY PARTNERS LLP

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR

CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID
IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR
MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SC SD SE SG SI SK
SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW