

Search history

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Search [SP]: 1. a method of wireless communication, comprising: measuring, by a first device, a condition of a wireless channel; generating at least one channel side information feedback message that provides information on a relationship of a set of parameters based on the measured condition of the wireless channel, the set of parameters comprising a data rate parameter, an error probability parameter, and at least one of a deadline parameter or a transmission link parameter wherein at least a first parameter of the set of parameters is input to the first device and at least a second parameter of the set of parameters is output conditioned on at least the first parameter and transmitting the at least one channel side information feedback message to a second device, the at least one channel side information feedback message comprising at least the first parameter and at least the second parameter. 2. the method of claim 1, wherein generating the at least one channel side information feedback message comprises: estimating a value of each parameter in a first subset of the set of parameters based on a given value for each parameter in a remaining subset of the set of parameters. 3. the method of claim 2, further comprising: receiving over the wireless channel the given value for at least one parameter of the remaining subset. 4. the method of claim 2, further comprising: determining, by the first device, the given value for at least one parameter of the remaining subset. 5. the method of claim 2, wherein the at least one channel side information feedback message comprises an estimated value of at least one parameter of the first subset. 6. the method of claim 2, wherein the first subset comprises the data rate parameter and the remaining subset comprises the error probability parameter, the deadline parameter, and the transmission link parameter. 7. the method of claim 2, wherein the first subset comprises the error probability parameter and the remaining subset comprises the data rate parameter, the deadline parameter, and the transmission link parameter. 8. the method of claim 2, wherein the first subset comprises the deadline parameter and the remaining subset comprises the error probability parameter, the data rate parameter, and the transmission link parameter. 9. the method of claim 2, wherein the first subset comprises the transmission link parameter and the remaining subset comprises the error probability parameter, the deadline parameter, and the data rate parameter. 10. the method of claim 2, wherein the first subset comprises the data rate parameter and the remaining subset comprises the error probability parameter and the deadline parameter. 11. the method of claim 2, wherein the first subset comprises the data rate parameter, the deadline parameter, and the transmission link parameter, and the remaining subset comprises the error probability parameter. 12. the method of claim 2, wherein the remaining subset comprises the deadline parameter and a value of at least one parameter of the first subset is estimated for a plurality of different given values of the deadline parameter. 13. the method of claim 2, wherein the first subset comprises the error probability parameter and the value of the error probability parameter is estimated based on a plurality of different radio links. 14. the method of claim 13, further comprising: selecting the plurality of different radio links as a subset of all possible radio links. 15. the method of claim 13, wherein the error probability parameter is based on simultaneous transmission over the plurality of different radio links. 16. the method of claim 1, wherein the deadline parameter corresponds to a latency associated with a single retransmission of a signal. 17. a device for wireless communication, comprising: means for measuring a condition of a wireless channel; means for generating at least one channel side information feedback message that provides information on a relationship of a set of parameters based on the measured condition of the wireless channel, the set of parameters comprising a data rate parameter, an error probability parameter, and at least one of a deadline parameter or a transmission link parameter wherein at least a first parameter of the set of parameters is input to the device and at least a second parameter of the set of parameters is output conditioned on at least the first parameter and means for transmitting the at least one channel side information feedback message to another device, the at least one channel side information feedback message comprising at least the first parameter and at least the second parameter. 18. the device of claim 17, wherein the means for generating the at least one channel side information feedback message comprises: means for estimating a value of each parameter in a first subset of the set of parameters based on a given value for each parameter in a remaining subset of the set of parameters. 19. the device of claim 18, further comprising: means for receiving over the wireless channel the given value for at least one parameter of the remaining subset. 20. the device of claim 18, further comprising: means for determining the given value for at least one parameter of the remaining subset. 21. the device of claim 18, wherein the at least one channel side information feedback message comprises an estimated value of at least one parameter of the first subset. 22. the device of claim 18, wherein the first subset comprises the data rate parameter and the remaining subset comprises the error probability parameter, the deadline parameter, and the transmission link parameter. 23. the device of claim 18, wherein the first subset comprises the error probability parameter and the remaining subset comprises the data rate parameter, the deadline parameter, and the transmission link parameter. 24. the device of claim 18, wherein the first subset comprises the deadline parameter and the remaining subset comprises the error probability parameter, the data rate parameter, and the transmission link parameter. 25. the device of claim 18, wherein the first subset comprises the transmission link parameter and the remaining subset comprises the error probability parameter, the deadline parameter, and the data rate parameter. 26. the device of claim 18, wherein the first subset comprises the data rate parameter and the remaining subset comprises the error probability parameter and the deadline parameter. 27. the device of claim 18, wherein the first subset comprises the data rate parameter, the deadline parameter, and the transmission link parameter, and the remaining subset comprises the error probability parameter. 28. the device of claim 18, wherein the remaining subset comprises the deadline parameter and a value of at least one parameter of the first subset is estimated for a plurality of different given values of the deadline parameter. 29. the device of claim 18, wherein the first subset comprises the error probability parameter and the value of the error probability parameter is estimated based on a plurality of different radio links. 30. the device of claim 29, further comprising: means for selecting the plurality of different radio links as a subset of all possible radio links. 31. the device of claim 29, wherein the error probability parameter is based on simultaneous transmission over the plurality of different radio links. 32. the device of claim 17, wherein the deadline parameter corresponds to a latency associated with a single retransmission of a signal. 33. a device for wireless communication, comprising a processor, memory in electronic communication with the processor, and instructions stored in the memory, the instructions being executable by the processor to: measure a condition of a wireless channel; generate at least one channel side information feedback message that provides information on a relationship of a set of parameters based on the measured condition of the wireless channel, the set of parameters comprising a data rate parameter, an error probability parameter, and at least one of a deadline parameter or a transmission link parameter wherein at least a first parameter of the set of parameters is input to the device and at least a second parameter of the set of parameters is output conditioned on at least the first parameter and transmit the at least one channel side information feedback message to another device, the at least one channel side information feedback message comprising at least the first parameter and at least the second parameter. 34. the device of claim 33, wherein the instructions executable by the processor to generate the at least one channel side information feedback message comprise instructions executable by the processor to: estimate a value of each parameter in a first subset of the set of parameters based on a given value for each parameter in a remaining subset of the set of parameters. 35. the device of claim 34, wherein the instructions are executable (Results 0)

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Title: VOICE GATEWAY WITH DOWNSTREAM VOICE SYNCHRONIZATION

Abstract: A network gateway is configured to facilitate on line and off line bi-directional **communication** between a number of near end data and telephony **devices** with far end data termination **devices** via a hybrid fiber coaxial network and a cable modem termination system. The described network gateway combines a QAM **receiver**, a **transmitter**, a DOCSIS MAC, a CPU, a voice and audio **processor**, a voice synchronizer, an Ethernet MAC, and a USB controller to provide high performance and robust operation. It is emphasized that this abstract is provided to comply with the rules requiring an abstract which will allow a searcher or other reader to quickly ascertain the subject matter of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or the meaning of the claims.

Classifications:**International (IPC 8-9):** E05C1/00 G01R31/08 G06F11/00 G10L11/02

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E05C1/00 G10L21/02 H04L1/00 H04L12/28 H04L29/08

H04Q1/45 (Advanced/Non-invention);

G10L11/00 H04B3/23 H04J3/06 H04L12/28 H04L12/54 H04L12/66

H04L29/06 H04M11/00 H04M7/00 (Core/Invention);

E05C1/00 G10L21/00 H04L29/08 (Core/Non-invention)

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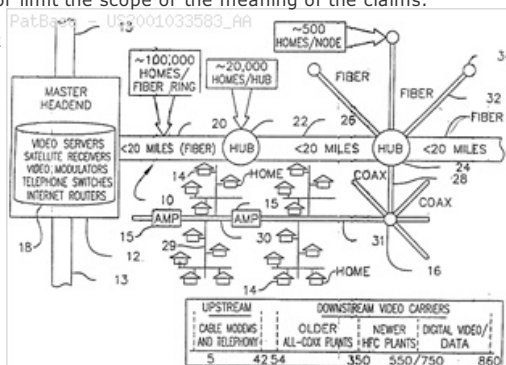
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Family:

Publication number	Publication date	Application number	Application date
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Probable Assignee: AVAGO TECHNOLOGIES LTD

Assignee(s): (std): THI JAMES C H ; THI JAMES C ; RABENKO THEODORE F ; LUKAS ROBERT M ; LANSING SHANE P ; LEE ROBERT J ; MILLER KEVIN L ; LI HENRY ; NICOL JORDAN J ; MITCHELL ROSS ; LEBLANC ; UNGER KEN ; PAYTON JOHN ; STEVENSON SHAWN ; TACKIN ONUR ; LEBLANC WILF ; LEBLANC WILFRID ; MITCHELL ROSE ; BOORA BILL ; BORAZJANI RAMIN ; BRANDEN SCOTT ; HARTMAN DAVID ; BROOKS TODD L ; ENNS DAVID M ; KWAN KENNY C ; BROADCOM CORP ; GRIFFITHS CHAD ; HENRY LI ; BROADCOM CORPROATION ; LEBLANC WILFRED ; NICOL JORDAN JAMES ; UNGER KENNETH J

Assignee(s): UNIV ; BROADCOM IRVINE CORP ; AVAGO TECHNOLOGIES GENERAL IP SINGAPORE PTE LTD ; AVAGO TECHNOLOGIES LTD ; BANK OF AMERICA NA COLLATERAL AGENT AS ; BROADCOM CORP IRVINE ; OF CALIFORNIA UNIV

Inventor(s): (std): BORAZJANI RAMIN ; BROOKS TODD L ; DAVID HARTMAN ; DAVID M ENNS ; BILL BOORA ; HARTMAN DAVID ; HENRY LI ; JAMES C H THI ; JOHN PAYTON ; JORDAN J NICOL ; KEN UNGER ; KENNY C KWAN ; LEBLANC WILFRID ; LEE ROBERT J ; LUKAS ROBERT M ; MILLER KEVIN L ; NICOL JORDAN JAMES ; ONUR TACKIN ; RABENKO THEODORE F ; ROSS MITCHELL ; SHAWN STEVENSON ; THEODORE F

RABENKO ; THI JAMES C ; LANSING SHANE P ; UNGER KENNETH J ; WILF LEBLANC ; UNGER KEN ; THI JAMES ; TACKIN ONUR ; STEVENSON SHAWN ; RABENKO THEODORE ; PAYTON JOHN ; NICOL JORDAN J ; LI HENRY ; LEE WING YEE WINNIE ; LEBLANC WILFRED ; MITCHELL ROSS ; MITCHELL ROSE ; LEBLANC WILF ; LEBLANC WIFRID ; LEBLANC WIFRED ; LEBLANC ; ENNS DAVID M ; BROOKS TODD LEE ; BRANDEN SCOTT ; KWAN KENNY C ; GRIFFITHS CHAD ; BOORA BILL ; THI JAMES C H

Inventor(s): ENNS DAVID M RICHMOND ; BOORA BILL RICHMOND V6V 2Z8 ; KWAN KENNY C RICHMOND ; LEBLANC WIFRID V6E 1J9 VANCOUVER ; LI HENRY RICHMOND ; LEBLANC WILF RICHMOND ; MITCHELL ROSS RICHMOND ; NICOL JORDAN J RICHMOND ; PAYTON JOHN RICHMOND ; STEVENSON SHAWN RICHMOND ; TACKIN ONUR RICHMOND ; THI JAMES CH ; UNGER KEN RICHMOND ; LEBLANC RICHMOND ; THI JAMES C H IRVINE ; RABENKO THEODORE F DULUTH ; NICOL JORDAN ; KWAN KENNY ; HARTMAN DAVID IRVINE ; BOORA BILL RICHMOND ; ENNS DAVID

Agent(s): BOSCH JEHL PATENTANWALTSGESELLSCHAFT MBH; JEHL VOLKER ARMIN; JEHL VOLKER ARMIN ET AL; CHRISTIE PARKER AND HALE LLP; MCANDREWS HELD AND MALLOY LTD; STERNE KESSLER GOLDSTEIN AND FOX PLLC; MCANDREWS HELD AND MALLOY; THOMAS KAYDEN HORSTEMEYER AND RISLEY LLP; THOMAS HORSTEMEYER LLP; STERNE KESSLER GOLDSTEIN FOX PLLC

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CR CU CY CZ DE DK DM DZ EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Title: SYSTEM AND **METHOD** FOR THE SYNCHRONIZATION AND DISTRIBUTION OF TELEPHONY TIMING INFORMATION IN A CABLE MODEM NETWORK

Abstract: A **method** for synchronizing clocks in a packet transport network. The **method** comprises, receiving an external network clock at a central packet network node and **transmitting** timing information to a plurality of packet network **devices**, the timing information based upon the external network clock. The **method** further comprises, **transmitting** and receiving data that is synchronized to the timing information to a plurality of connected packet network **devices**. And finally, delivery of packets to an external interface via a packet network that contains data synchronized to the external network clock.

Classifications:

International (IPC 8-9): H04J3/06 H04L12/28

H04N7/173 (Advanced/Invention);

H04J3/06 (Core/Invention)

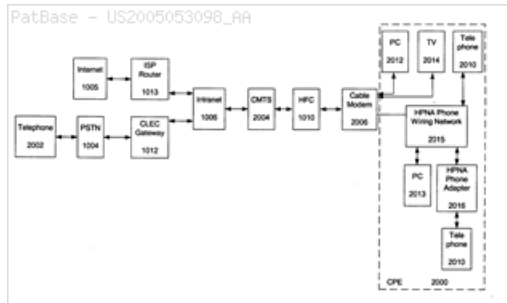
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European: H04J3/06C1 H04J3/06C1B H04J3/06C1P2A T04J3/06C1B T04J3/06C1D2 T04J3/06C1P2A T04J3/06C1P4

US: 370/352 370/356 370/401 370/503 370/503P 379/93.01

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Family:

Publication number	Publication date	Application number	Application date
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Priority:

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Probable Assignee: AVAGO TECHNOLOGIES LTD

Assignee(s): (std): BROADCOM CORP ; DENNEY LISA V ; RABENKO THEODORE F

Assignee(s): AVAGO TECHNOLOGIES GENERAL IP SINGAPORE PTE LTD ; AVAGO TECHNOLOGIES LTD ; BANK OF AMERICA NA COLLATERAL AGENT AS

Inventor(s): (std): DENNEY LISA ; DENNEY LISA V ; RABENKO THEODORE ; RABENKO THEODORE F

Inventor(s): THEODORE F RABENKO ; LISA V DENNEY

Agent(s): CHRISTIE PARKER AND HALE LLP; STERNE KESSLER GOLDSTEIN AND FOX PLLC

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BY BZ CA CF CG CH CI CM CN CR CU CY CZ DE DK DM DZ EE ES FI FR GA GB GD GE GH GM GN GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Title: CACHE UPDATING METHOD AND APPARATUS

Abstract: A method of updating a cache in an integrated circuit comprising: the cache; a processor connected to the cache via a cache bus; a memory interface connected to the cache via a first bus and to the processor via a second bus, the first bus being wider than the second bus or the cache bus; and memory connected to the memory interface via a memory bus; the method comprising the steps of: (a) following a cache miss, using the processor to issue a request for first data via a first address, the first data being that associated with the cache miss; (b) in response to the request, using the memory interface to fetch the first data from the memory, and sending the first data to the processor; (c) sending, from the memory interface and via the first bus, the first data and additional data, the additional data being that stored in the memory adjacent the first data; (d) updating the cache with the first data and the additional data via the first bus; and (e) updating flags in the cache associated with the first data and the additional data, such that the updated first data and additional data in the cache is valid.

Classifications:

International (IPC 8-9): B23P17/00 B41J2/01 B41J2/015 B41J2/05 B41J2/135 B41J2/155 B41J2/165 B41J2/175 B41J2/21 B41J29/38 B41J29/393 G06F1/00 G06F1/08 G06F12/00 G06F12/02 G06F12/10 G06F13/00 G06F13/28 G06F19/00 G06F21/00 G06F9/36 H03K19/00 H04L9/00 H04N1/40 H04N1/405 (Advanced/Invention); B41J2/01 B41J2/05 G06F12/10 G06F13/20 G06F21/00 H04L9/00 H04N1/40 H04N1/405 (Core/Invention)

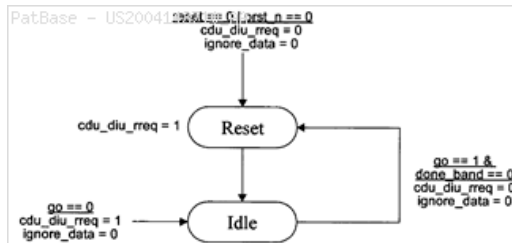
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**Family:**

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Inventor(s): GARY SHIPTON ; KIA SILVERBROOK ; JACKSON PULVER MARK SILVERBROOK RESEACH PTY LTD ; PLUNKETT RICHARD T SILVERBROOK RESEARCH PTY LTD ; PLUNKETT RICHARD ; PAUL LAPSTUN ; MARK JACKSON PULVER ; LAPSTUN PAUL SILVERBROOK RESEARCH PTY LTD ; RICHARD THOMAS PLUNKETT ; SHIPTON GARY SILVERBROOK RESEARCH PTY LTD ; WALMSLEY SIMON R SILVERBROOK RESEARCH PTY LTD ; SIMON ROBERT WALMSLEY ; SILVERBROOK KIA SILVERBROOK RESEARCH PTY LTD ; JACKSON PULVER MARKAU ; LAPSTUN PAULAU ; PLUNKETT RICHARD THOMASAU ; SHIPTON GARYAU ; SILVERBROOK KIAAU ; WALMSLEY SIMON ; WALMSLEY SIMON ROBERTAU

Agent(s): SILVERBROOK RESEARCH PTY LTD; PIZZEYS PATENT AND TRADE MARK ATTORNEYS; PIZZEYS PATENT AND TRADE MARK ATTORNEYS PTY LTD; OYEN WIGGS GREEN AND MUTALA LLP; MOORE BARRY

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LI LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NE NI NL NO NZ OM PG PH PL PT RO RU SC SD SE SG SI SK SL SN SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Title: RELATIVELY UNIQUE ID IN INTEGRATED CIRCUIT

Abstract: A **method** of manufacturing a series of integrated circuits having related functionality, the **method** including the steps of: (a) determining an identifier; (b) permanently storing the identifier on one of the integrated circuits; (c) repeating steps (a) and (b) for each integrated circuit in the series; and wherein the identifiers for the series are determined in such a way that knowing the identifier of one of the integrated circuits does not improve the ability of an attacker to determine the identifier of any of the other integrated circuits.

Classifications:

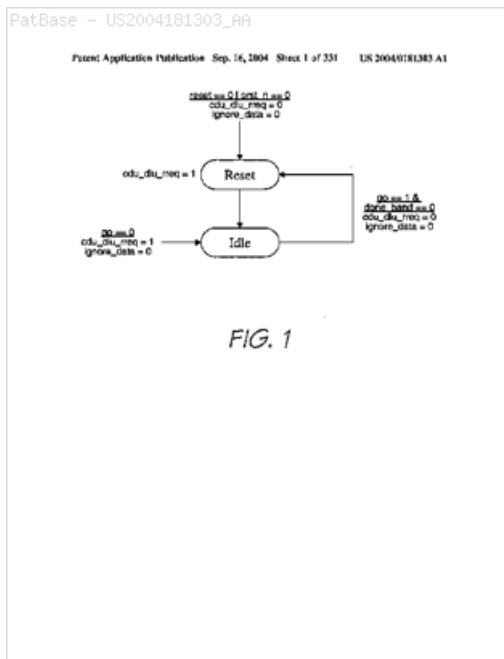
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International (IPC 1-7): B41J2/015 B41J2/04 B41J29/38 B41J29/393 G06F12/00 G06F12/14 G06F13/00 G06F17/60 G06F19/00 G06F9/44 G06F9/46 G06K9/00 H01L29/00 H02H5/04 H03K4/06 H04L9/00

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**Family:**

Publication number	Publication date	Application number	Application date
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Priority:

AU20020953134 20021202	AU20020953135 20021202	US20030727210 20031202
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US20050212702 20050829	US20060442131 20060530	US20060474278 20060626
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Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD ; WALMSLEY SIMON R

Assignee(s): ZAMTEC LTD ; WALMSLEY SIMON ROBERT ; JACKSON PULVER MARK ; MEMJET TECHNOLOGY LTD ; PLUNKETT RICHARD THOMAS ; ROBERT WALMSLEY SIMON ; SILVERBROOK KIA ; SILVERBROOK RESEARCH PTY LTD

Inventor(s): (std): PLUNKETT RICHARD T ; PLUNKETT RICHARD THOMAS ; ROBERT WALMSLEY SIMON ; SHIPTON GARY ; SILVERBROOK KIA ; JACKSON PULVER MARK ; WALMSLEY SIMON R ; WALMSLEY SIMON ROBERT

Inventor(s): PLUNKETT RICHARD ; WALMSLEY SIMON

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: DATA RATE EQUALISATION TO ACCOUNT FOR RELATIVELY DIFFERENT PRINthead WIDTHS

Abstract: A printer controller configured to generate dot data for supply to a printhead that includes at least first and second longitudinally extending printhead chips that are positioned adjacent each other either side of a join region such that a printing width of the printhead is wider than the length of either printhead chip, the printer controller being configured such that, in the event that the printhead chips to which dot data is being supplied are of sufficiently unequal relative length, the dot data is supplied more frequently, or at a higher rate, to the longer of the two printhead chips.

Classifications:

International (ipc 8-9): B41J2/05 B41J2/155 B41J29/38 G06F21/00 H04L9/00 H04N1/405 (Advanced/Invention); B41J2/05 G06F21/00 H04L9/00 H04N1/405 (Core/Invention)

International (ipc 1-7): B41J29/38

CPC: Y10S707/99933 Y10S707/99939 Y10T29/49401 G06F21/73 B41J2/04505 B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405

European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20

US: 347/13 347/40 347/42 347/5 347/6 347/6P 347/9

PatBase - US2004223010_AA

Patent Application Publication Nov. 11, 2004 Sheet 1 of 331 US 2004/0223010 A1

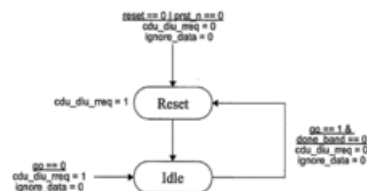


FIG. 1

Family:

Publication number	Publication date	Application number	Application date
US2004223010 AA	20041111	US20030727204	20031202
US7121639 BB	20061017	US20030727204	20031202

Priority:

AU20020953134 20021202 AU20020953135 20021202

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD ; PLUNKETT RICHARD THOMAS

Inventor(s): (std): PLUNKETT RICHARD THOMAS

Title: MECHANISM FOR REDUCING WRITE PROBLEMS BY CONTROLLING CHARGE PUMPS FOR FLASH **MEMORY**

Abstract: An integrated circuit comprising a **processor**, a **memory** that the **processor** can access, a **memory** access unit for controlling accesses to the **memory**, an input for receiving power for the integrated circuit from an external power source, and a power detection unit, the power detection unit being configured to: monitor a quality of power supplied to the input; and in the event the quality of the power drops below a predetermined **threshold**, disabling a power supply to circuitry for use in writing to the **memory**, such that the **memory** access unit's ability to alter data in the **memory** is disabled prior to address or data values to be written to the **memory** becoming unreliable due to failing power.

Classifications:

International (IPC 8-9): B41J2/05 G06F21/00 H04L9/00

H04N1/405 (Advanced/Invention);

B41J2/05 G06F21/00 H04L9/00 H04N1/405 (Core/Invention)

International (IPC 1-7): H02H3/05

CPC: Y10S707/99933 Y10S707/99939 G06F21/73 B41J2/04505

B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543

B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554

G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74

G06F21/75 G06F21/78 H03K5/1252 H04N1/405 Y10T29/49401

European: B41J2/045D12 B41J2/045D14 B41J2/045D15

B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47

B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B

G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78

H03K5/1252 H04N1/405 L41J202/20

US: 713/300 714/22 714/22P

PatBase - US2005160316_A1

Patent Application Publication Jul. 21, 2005 Sheet 1 of 331 US 2005/0160316 A1



FIG. 1

Family:

Publication number	Publication date	Application number	Application date
US2005160316 AA	20050721	US20030727238	20031202

Priority:

AU20020953134 20021202 AU20020953135 20021202

Probable Assignee: SILVERBROOK RES PTY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): SHIPTON GARY

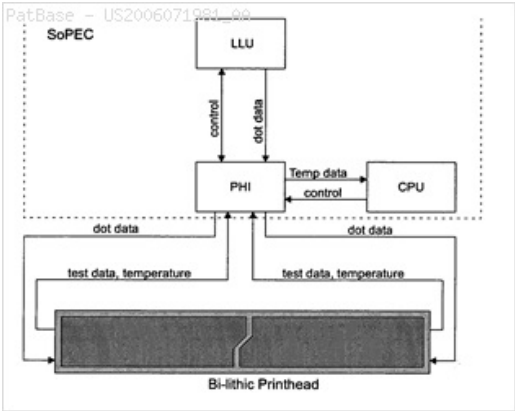
Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: DATA RATE SUPPLY PROPORTIONAL TO THE RATIO OF DIFFERENT PRINthead LENGTHS

Abstract: A printer controller configured to generate dot data for supply to a printhead which includes at least a first printhead integrated circuit and a second printhead integrated circuit positioned adjacent each other either side of a join region, the printer controller configured to transfer dot data to each of the first printhead integrated circuit and the second printhead integrated circuit at a rate proportional to the relative lengths of the first printhead integrated circuit and the second printhead integrated circuit.

Classifications:

International (IPC 8-9): B41J2/05 B41J2/155 B41J29/38 G06F21/00 H04L9/00 H04N1/405 (Advanced/Invention); G06F21/00 H04L9/00 H04N1/405 (Core/Invention)
CPC: Y10S707/99933 Y10S707/99939 G06F21/73 B41J2/04505 B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 Y10T29/49401
European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20
US: 347/13 347/49 347/5 347/59 347/59P



Family:

Publication number	Publication date	Application number	Application date
US2006071981 AA	20060406	US20050272491	20051114
US7278697 BB	20071009	US20050272491	20051114

Priority:

AU20020953134 20021202 AU20020953135 20021202 US20030727204 20031202
US20050272491 20051114

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): PLUNKETT RICHARD THOMAS ; PLUNKETT RICHARD T

Inventor(s): PLUNKETT RICHARD

Agent(s): SILVERBROOK RESEARCH PTY LTD

Title: CONTROLLER FOR PRINthead HAVING ARBITRARILY JOINED NOZZLE ROWS

Abstract: A controller for a printhead is provided. The printhead has rows of printing nozzles with each nozzle row formed by adjacent sub-rows of printing nozzles of adjacently disposed printhead modules. Each nozzle row is arranged such that the join of the respective adjacent sub-rows is arbitrarily located relative to the other nozzle rows thereby forming an arbitrarily shaped join region. The controller being configured to determine the arbitrary shape of the join region and to supply dot data to the printhead which compensates for the determined arbitrary shape.

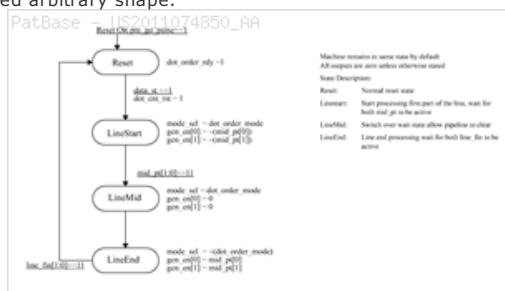
Classifications:

International (IPC 8-9): B41J2/05 B41J2/14 B41J29/38 G06F21/00 H04L9/00 H04N1/405 (Advanced/Invention)

CPC: Y10S707/99933 Y10S707/99939 G06F21/73 B41J2/04505 B41J2/04508 B41J2/0451 B41J2/04528 B41J2/04541 B41J2/04543 B41J2/04563 B41J2/04573 B41J2/04586 B41J2202/20 G06F21/554 G06F21/57 G06F21/575 G06F21/64 G06F21/71 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 Y10T29/49401

European: B41J2/045D12 B41J2/045D14 B41J2/045D15 B41J2/045D26 B41J2/045D34 B41J2/045D35 B41J2/045D47 B41J2/045D53 B41J2/045D61 G06F21/55B G06F21/57 G06F21/57B G06F21/64 G06F21/71 G06F21/73 G06F21/74 G06F21/75 G06F21/78 H03K5/1252 H04N1/405 L41J202/20

US: 347/12 347/12P 347/14 347/49 347/5

**Family:**

Publication number	Publication date	Application number	Application date
US2011074850 AA	20110331	US20100958968	20101202
US8038239 BB	20111018	US20100958968	20101202

Priority:

AU20020953134 20021202 AU20020953135 20021202 US20030727162 20031202
US20100958968 20101202

Probable Assignee: MEMJET TECHNOLOGY LTD

Assignee(s): (std): SILVERBROOK RES PTY LTD

Assignee(s): SILVERBROOK RESEARCH PTY LTD ; ZAMTEC LTD ; MEMJET TECHNOLOGY LTD

Inventor(s): (std): PLUNKETT RICHARD THOMAS ; WALMSLEY SIMON ROBERT