

[SS 1] ..fi epodoc

 Database: EPODOC

[EPODOC: SS 1] hummidity

Results in EPODOC 2

[SS 2] moisture and detection

Results in EPODOC 7.163

[SS 3] electronic and ss3

Results in EPODOC 7

[SS 4] ..li



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PN - [JP2016026594](#) A 20160218

PR - JP20150171767 20150901

AP - JP20150171767 20150901

DT - I

CT - || STSE (A)  
[JP2009142304](#) A 20090702 [  
] (DAIICHI SHOKAI KK);  
[JP2007319608](#) A 20071213 [  
] (TAKEYA KK);  
[JP5450766B](#) B1 20140326 [ ];  
[JP2007236675](#) A 20070920 [  
] (SANKYO CO)

FI - A63F7/02&304Z;  
A63F7/02&315Z;  
A63F7/02&326Z; A63F7/02&334

FT - 2C088/BC56; 2C088/CA13;  
2C088/EA10

PA - FUJISHOJI CO LTD

TI - GAME MACHINE

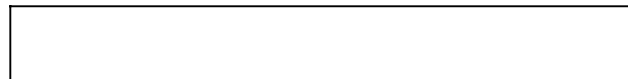
AB - PROBLEM TO BE SOLVED: To  
provide a game machine  
capable of executing a proper  
control operation without



wasting a memory space or a circuit space.SOLUTION: A main control part 21 comprises: an **electronic** element 21A incorporating, besides a CPU, an abnormality accommodation circuit REV that makes the CPU a reset state, when receiving no clear data until reaching a monitoring time; standby means **SS3** preventing the abnormality accommodation circuit REV from being functioned until a lapse of the standby time; and starting means ST3 that, when the standby operation is completed, causes the abnormality accommodation circuit REV to function on the basis of operation of a control program. The control program has circuit processing ST21 of outputting clear data for each prescribed time. The monitoring time is set longer than the lapse time from when the starting means is functioned until avoidance processing is executed first.SELECTED DRAWING: Figure 8

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PN - [JP2015114699](#) A 20150622  
 PR - JP20130254074 20131209  
 AP - JP20130254074 20131209  
 DT - I  
 FI - G06F3/041&380J;  
 G06F3/041&380R;  
 G06F3/041&550;  
 G06F3/041&595;  
 G06F3/048&651A;  
 G06F3/0484&120; G06F3/0488  
 FT - 5B068/AA05; 5B068/AA25;  
 5B068/BC02; 5B068/BD02;  
 5B068/BD17; 5E555/AA13;  
 5E555/BA03; 5E555/BA67;



5E555/BD07; 5E555/CA14;  
5E555/CB44; 5E555/DA01;  
5E555/DB41; 5E555/DD07;  
5E555/EA24; 5E555/FA14

- PA - BROTHER IND LTD
- TI - WRITING DATA PROCESSING PROGRAM
- AB - PROBLEM TO BE SOLVED: To make writing contents correspondent to a schedule event during which the writing contents were created, while performing correction without separating description items as determined by schedule time divisions on a prepared schedule table on the condition that a predetermined correction condition is satisfied.  
SOLUTION: A writing data processing program implements a division processing step (step **SS3**) and a correction processing step (step **SS4**). In the division processing step (step **SS3**), stroke data transmitted from an **electronic** writing device 20 are acquired by a notebook-sized PC 10 together with corresponding time information and in accordance with the corresponding time information, the acquired stroke data are made correspondent to a description item into one relevant division among a plurality of time divisions on the schedule table. In the correction processing step (step **SS4**), in the case where the stroke data acquired by the notebook-sized PC 10 are spread over preceding and following time divisions which are neighboring to each other, in the timing when the predetermined correction

condition is satisfied,  
correspondence is corrected to  
a description item only to any  
one of the preceding and  
following time divisions.

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PN - [KR20010091237](#) A 20011023  
PR - KR20000012729 20000314  
AP - KR20000012729 20000314  
DT - I  
PA - VERTICAL KOREA INC [KR]  
TI - **ELECTRONIC** COMMERCE  
INTERMEDIATION METHOD  
AB - PURPOSE: An **electronic**  
commerce intermediation  
method is provided to network  
purchasing enterprises and  
sales enterprises engaged in a  
textile fashion field one another  
and supply a consistent service  
so that users can obtain  
necessary information at a  
necessary time. CONSTITUTION:  
A purchasing enterprise(or a  
selling enterprise) applies for a  
free homepage to an  
intermediary system through its  
terminal(SS1). The enterprise  
inputs associated company  
information, including its ID,  
password, e-mail address and  
company name, and transmits  
the data to the intermediary  
system(S22). The intermediary  
system sends the transmitted  
data to a credit appraisal  
institute. The credit appraisal  
institute decides the  
enterprise's credit rating, and  
transmits a result to the  
intermediary system in order to  
judge whether the enterprise  
can be registered as a member  
company(**SS3**). In case that it is  
judged that the company is  
qualified for membership



registration, the intermediary system registers the company as a member company(SS4). If the enterprise reconfirms and selects the application of the free homepage through its terminal(SS5), the intermediary system constructs the free homepage according to the enterprise's relevant information(SS6). Then the intermediary system makes out an **electronic** catalogue for the sales goods of the enterprise (SS7), and stores it in a database(SS8).

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PN - [JP2004309846](#) A 20041104

PNFP - JP4333189B B2 20090916

PR - JP20030104122 20030408

AP - JP20030104122 20030408

DT - I

FI - G02F1/133&505; G02F1/133&550; G09G3/20&611A; G09G3/20&621M; G09G3/20&623L; G09G3/20&623R; G09G3/20&641C; G09G3/20&641E; G09G3/20&680G; G09G3/36

FT - 2H093/NA16; 2H093/NB07; 2H093/NB11; 2H093/NC13; 2H093/NC23; 2H093/NC34; 2H093/NC49; 2H093/NC58; 2H093/ND39; 2H193/ZA04; 2H193/ZA20; 2H193/ZH21; 5C006/AA01; 5C006/AA14; 5C006/AA16; 5C006/AC21; 5C006/AF13; 5C006/AF42; 5C006/AF44; 5C006/AF45; 5C006/AF46; 5C006/AF50; 5C006/AF51; 5C006/AF52; 5C006/AF53; 5C006/AF54; 5C006/AF64; 5C006/AF69; 5C006/AF71; 5C006/AF83; 5C006/BB16; 5C006/BC11; 5C006/BC20; 5C006/BC23; 5C006/BF11; 5C006/BF14; 5C006/BF24; 5C006/BF25; 5C006/BF34; 5C006/EB05; 5C006/FA47; 5C006/FA56; 5C080/AA10; 5C080/BB05; 5C080/DD26; 5C080/EE29; 5C080/FF11; 5C080/JJ02; 5C080/JJ03; 5C080/JJ04; 5C080/JJ05; 5C080/JJ06

PA - (A)  
SEIKO EPSON CORP

TI - (A)  
ELECTRO-OPTIC DEVICE, ITS DRIVING METHOD, AND **ELECTRONIC** EQUIPMENT

AB - (A)  
PROBLEM TO BE SOLVED: To reduce the electric power consumption of a liquid crystal display device.  
- SOLUTION: A sampling circuit 140 is equipped with (n) pieces of transistor (TR) groups U1 to Un. Each of the TRs groups U1 to Un has three TRs Tr1 to Tr3 of different sizes. The respective TRs Tr1 to Tr3 are selected based on selection signals SS1 to **SS3** supplied through control lines L1 to L3. The selection signals SS1 to **SS3** are so

determined that a potential change of a data line 114 is reflected based on gradation data. As a result, the changing of the sizes of the TRs according to the driving load condition of the data line 114 is made possible.

- COPYRIGHT: (C)2005,JPO&NCIPI

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PN - [GB1325341](#) A 19730801

PR - DE19702034451  
19700711; DE19702034452  
19700711

AP - GB19700038075 19700806

DT - \*; Rep

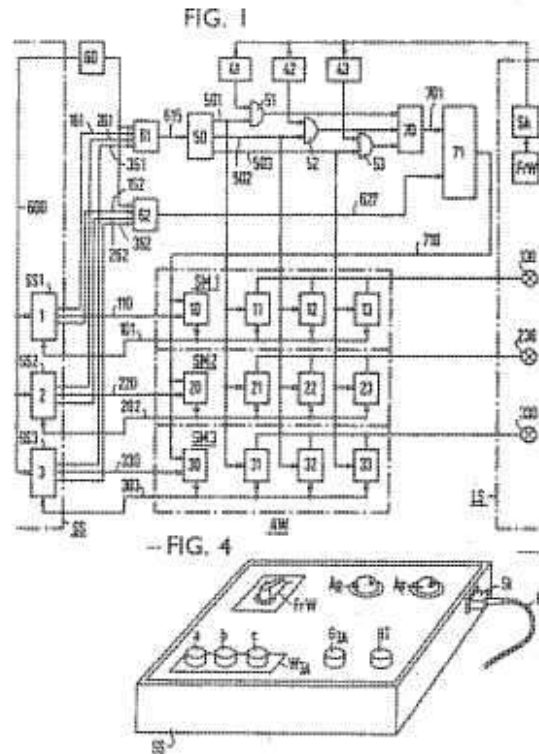
CCI - [G09B7/073](#)

IDT - 42N6

PA - SIEMENS AG

TI - EDUCATIONAL TESTING  
APPARATUS

AB - 1325341 Question and answer teaching system; selective signalling SIEMENS AG 6 Aug 1970 [7 Aug 1969 11 July 1970 (2)] 38075/70 Headings G4H and G5G The invention relates to a question and answer teaching system wherein actual (i.e. pupil) answers are automatically compared with desired (i.e. teacher) answers, the marks (correct or incorrect indications) are stored and indicators in the teaching station and optionally in the corresponding pupil station are operated. A first embodiment for individual instruction is illustrated in Fig. 1 with provision for one teacher station LS, three pupil stations SS1- SS3, and 3 question stores 41-43. The teacher initially stores the desired answers in stores 41-43 using desired question transmitter SA and question selector FrW. Each pupil position SS is provided (Fig. 4) with a question selector



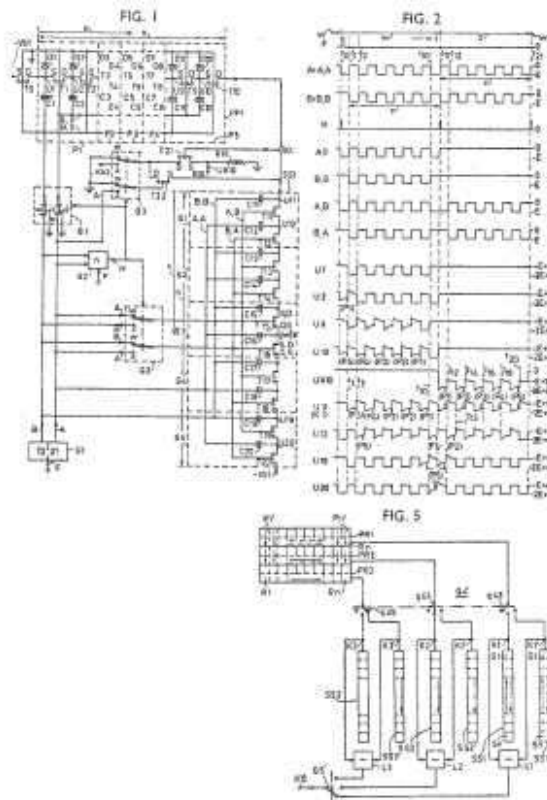
FrW, an actual answer selector  
W VA , an actual answer  
transmitter G VP , an auxiliary  
button HT for calling the  
teacher and lamps A R and A F  
for correct and incorrect  
answer indications and for  
calling signals from the  
teacher. Cyclically, under  
control of a clock 60 the  
question numbers for the pupil  
positions SS1- SS3 are sampled  
by distributor 61 and decoded  
by decoder 50 into a one-out-of  
n outputs whereby selected  
ones of the desired answer  
signals from store 41-43 are  
gated together with  
corresponding actual answer  
signals from distributor 62 to a  
comparator 71. Actual answer  
transfer signals on lines 110,  
220, 330, open corresponding  
ones of gates 10, 20, 30 in  
evaluating unit AW to pass  
marked answer signals (the  
correct/incorrect output signals  
from comparator 71) to the row  
of stores 11-13, 21-23, 31-33  
corresponding to the pupil  
station currently being  
evaluated. At the same time, one  
or other of lines 501-503 is  
energized whereby the marked  
answer signal is stored in one  
of the stores 11-13, 21-23, 31-  
33 corresponding to the pupil  
and question and a lamp such  
as 130 is illuminated in the  
teacher position. A lamp is  
provided in the teacher station  
for each pupil station. Lamps at  
the pupil stations may similarly  
be illuminated unless blocked  
by operation of a switch at the  
teacher position. Single lamps  
which flash or shine  
continuously or pairs of  
alternatively illuminable lamps

may be provided to indicate correct and incorrect markings. The stores 11, &c. may be composed of NAND gates as illustrated in Fig. 2 (not shown) which also illustrates the flash generator connection BG for the lamps 130 &c. Where collective instruction only is required (i.e. all pupils progressing together from question to question, then the arrangement can be simplified (Figs. 6-8, not shown) by combining the desired answer transmitter and desired answer store as a set of simple changeover contacts or **electronic** presettable counters in the teacher station and by providing only a single store per pupil station. In this embodiment, a counter is provided at the teacher station for each pupil station whereby the number of correct and incorrect answers can be recorded. Class total counters are also provided (see below) and print-out means may be provided. There is a delay in the operation of the circuitry following clearing of modules between questions whereby any faulty setting of the desired answer transmitter can be corrected by the teacher depressing an error button (to prolong the delay) before the counters register. The stores are cross-coupled so that only the first answer given by pupils is stored. Indications may be given on the lamps before the marking is stored, at the end of the delay period. In a modification (Fig. 11, not shown) questions with alternative answers can be dealt with. The answer selectors

or transmitters may be formed as buttons (Fig. 4) or as rotary switches. Where buttons are used, recessed lamps may be provided to indicate which have been operated. Integrated circuit techniques may be used. The questions and answers may be projected from film, or displayed by television, blackboard &c. Two class counters are provided for respectively counting the totals of correct and incorrect answers to each question in turn.

6/7 © EPODOC / EPO

- PN - [GB1489191](#) A 19771019
- PR - NL19730011429 19730820
- AP - GB19740036188 19740816
- DT - \*\*
- CCI - [G11C19/186](#) ; [G11C19/188](#) ; [G11C27/04](#) ; [H01L27/14831](#) ; [H04N5/37213](#)
- PA - PHILIPS ELECTRONIC ASSOCIATED
- TI - RADIATION PICK-UP ARRANGEMENT COMPRISING A SERIES OF RADIATION-RESPONSIVE CHARGE STORAGE ELEMENTS INTERCOUPLED TO FORM AN INFORMATION SHIFT REGISTER
- AB - 1489191 Television  
PHILIPS **ELECTRONIC & ASSOCIATED INDUSTRIES** Ltd 16 Aug 1974 [20 Aug 1973]  
36188/74 Heading H4F An analogue information pick-up arrangement comprises a series of pick-up elements D each associated with a respective stage P of a charge-transfer shift-register PP1 from which information may be shifted into a further (reversible) shift-register SS1 where it is shifted



$$2(n+1-x) + 2(2x-1)b$$

in one direction during an input period and in the opposite direction during an output period, the two shift-registers being designed such that the information undergoes degradation which is uniform and independent of place of origin. Thus, if the register PP1 operates with a total number  $n$  of different switching operations (two per stage), the information ( $P_x$ ) originating in the stage  $P_x$  undergoes  $2(n + 1 - x)$  switching operations before application to the terminal K1. The information is applied to register SS1 and is shifted therein to the stage  $S_x$  and then back to the terminal K1, thus undergoing  $(2x-1)$  switching operations. If the degradation factor in register PP1 is  $a$ , and that in register SS1 is  $b$ , the total degradation of information ( $P_x$ ) is: and this can be made independent of  $x$  by arranging that  $b = a/2$ . This is possible to arrange in practice, since the register SS1 is without the pick-up elements which constrain the design of register PP1. The register PP1 shown comprises five stages  $P1... P5$ , containing odd and even series of capacitors  $C1... C9$ ;  $C2 ... C10$ , odd and even series of transistors  $T1 ... T9$ ;  $T0 ... T10$ , and odd and even series of photo-diodes (pick-up elements)  $D1... D9$ ;  $D2... D10$ . The transistors are of the isolated-gate type. The register SS1 has similar odd and even series of elements, but the mode of interconnection of the elements (evident from the Figure) differs in the two registers such that the register SS1 may be reversed

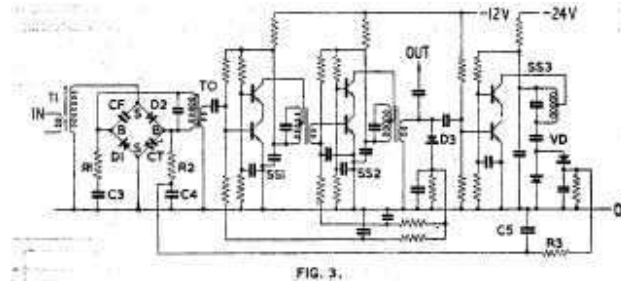
under control of a clock-pulse source G1 common to both registers. Information is read out under control of clock pulses during successive periods w, z, Fig. 2, which recur periodically and are spaced by much longer periods  $w \ll z$  during which the diodes D acquire information in the form of negative changes. At the end of each period  $w$ , signal F triggers a counter G1 which delivers two series A, B of  $2n$  pulses to terminals w, z of switches Q1, Q2, Q3 (the last receiver only pulses A). The switches are actuated by pulses H (from counter G2) which changes the movable contacts between terminals w and terminals z at the ends of periods  $w$  and z. The circuits T1, C2, &c. of register PP1 receive the signal A, O and the circuits T0, C1, T2, C3, &c. the signal B, O, through switch Q1, both these signals being zero during periods z and  $w \ll z$ . Thus, the information is shifted through successive stages P to the terminal K1 during periods w as is indicated by the voltages U1, U2, U9, U10, Fig. 2. Control signals A, A and B, B are fed to the register SS1 directly from the counter G1 and control signals A, B and B, A through the switch Q2. These cause the register to shift the information originating at terminal K1 forward during periods w and backwards during periods z whereby the signal U11, Fig. 2, appears at terminal K1. Switch Q3 is actuated at the end of periods w and causes

transistors T21 and T22 to  
 conduct during the periods z  
 wherein the output signal UK10  
 of the device appears at  
 terminal K10. During periods w,  
 the transistors T21, T22 are cut  
 off by virtue of the earth  
 connections made by the switch  
 Q3. The invention may be  
 applied to a bank of shift  
 registers PP1, PP2, ... PPm (see  
 Fig. 4, not shown) which are  
 read out in turn. Two reversible  
 registers SS1, SS2 are employed  
 and are connected to the  
 outputs of the bank PP1 ... PPm  
 by a commutator switch  
 actuated in such a manner that  
 reversible register SS2 is being  
 fed with information from an  
 even numbered member of the  
 bank PP whilst information  
 previously derived from an  
 oddnumbered member of bank  
 PP is being read out of register  
 SS1, and vice versa, the  
 registers SS1, SS2 operating in  
 opposite directions at any one  
 moment. Fig. 5 shows an  
 arrangement in which three  
 shift registers PR1, PR2, PR3  
 associated respectively with  
 pairs of reversible registers  
 SS1, SS1<SP>1</SP>; SS2,  
 SS2<SP>1</SP>; **SS3**,  
**SS3<SP>1</SP>**. In the shift  
 registers PR the diodes are  
 separated from the shift  
 elements when the information  
 is being fed out. Each register is  
 read out without information  
 being transferred from pick-up  
 to shift elements and  
 subsequently with such  
 information being thus  
 transferred. Each pair of  
 reversible registers SS is  
 connected to a respective  
 subtraction circuit L which

produces the difference of the two read-out signals whereby correction of the registers PR is achieved. A commutator switch Q4<SP>1</SP> is so actuated that information is being fed into one reversible register as it is being fed out of the next one.

7/7 © EPODOC / EPO

- PN - [GB969202](#) A 19640909
- PR - GB19600019522 19600602
- AP - GB19600019522 19600602
- DT - \*
- CCI - [H03G3/30](#) ; [H03G1/0064](#)
- PA - SECR AVIATION
- TI - Improvements in or relating to **electronic** amplifiers
- AB - 969,202. Gain Control.  
MINISTER OF AVIATION. Aug. 21, 1961 [June 2, 1960], No. 19522/60. Headings H3T and H4R. In order to control the gain of a transistor amplifier there is included in its signal path an attenuator in the form of a Wheatstone bridge having in at least one of its arms a variable capacitance, comprising a back-biased, semiconductor diode,- the effective value of which is dependent upon the amount of an applied D.C. bias derived from the output of the amplifier. As described; the arrangement is applied to, transistor amplifier comprising cascode stages SS1, SS2 in which the stage gain is controlled automatically by means of a gain control diode rectifier D3 feeding back a D.C. control.. voltage to these stages. In addition, a further cascode stage **SS3** is provided feeding a diode rectified the D.C. output of which is smoothed by filter



network R3, C5 and applied to vary the effective capacity of back-biased diodes D1, D2. The diodes D1, D2 comprise two arms of a capacity bridge network, the other arms of which comprise respectively a fixed capacitor CF and an adjustable capacitor CT by which the bridge balance may be adjusted. The bridge is fed with signal across one diagonal, by means of transformer T1 and the other diagonal feeds the signal to the amplifier input via transformer TO. The D.C. bias is applied to the diodes over resistor R2 and D.C. blocking condenser C4, a similar resistor R1 in series with corresponding condenser C3 being connected to the opposite corner of the bridge to maintain the balance.

**[SS 4]**