

Search history

Search 1: finite state machine (Results 14953)
Search 2: offset circuit compensator (Results 0)
Search 3: amplifier circuit with offset compensation (Results 8)

Title: ELECTRONIC TIMER CIRCUIT - HAS SERIES RESISTOR OPERATIONAL AMPLIFIERS WITH OFFSET COMPENSATION SCHMITT TRIGGER AND TRIAC

Abstract: The circuit has a very low resistance in series with the load. The voltage across this resistance, produced when current flows through the load, after amplification and rectification switches a triac via a schmitt trigger to energise an electric timer. The wire wound resistor (RM) which is in series with the load (RL) is of the order of 5 to 10 mohms. The voltage developed across it is amplified by an operational amplifier circuit with offset compensation (1) and rectified (2). When it exceeds a threshold value it operates a Schmitt trigger (3) which turns on a triac (4). This energises an electric timer (M).

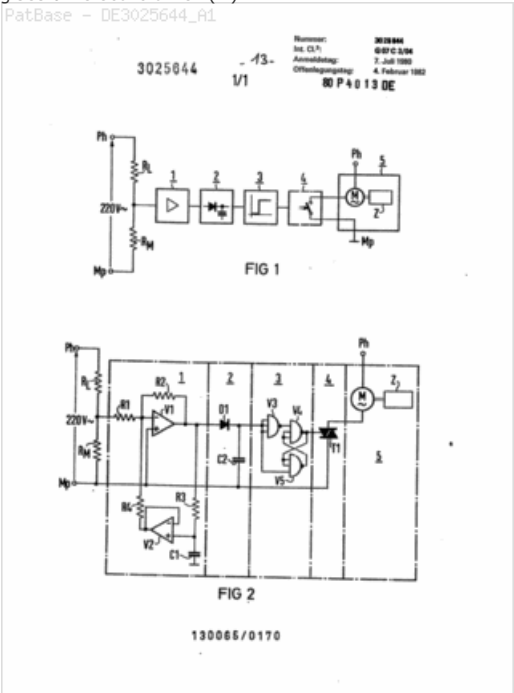
Classifications:

International (IPC 8-9): G07C3/04 (Advanced/Invention);
G07C3/00 (Core/Invention)

International (IPC 1-7): G07C1/04 G07C3/04

CPC: G07C3/04

European: G07C3/04



Family:

Publication number	Publication date	Application number	Application date
DE3025644 A1	19820204	DE19803025644	19800707

Priority:

DE19803025644 19800707

Probable Assignee: SIEMENS AG

Assignee(s): (std): SIEMENS AG

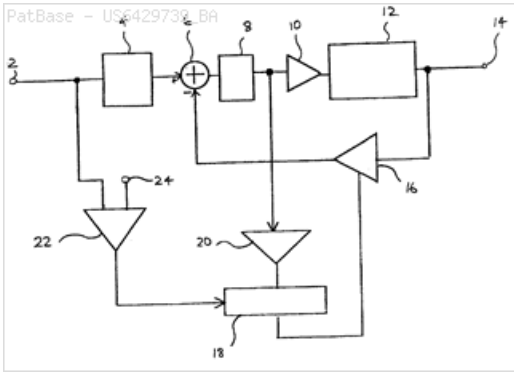
Inventor(s): (std): HARTMANN HANS HEINRICH DIPL ING ; KOEGLER GEORG ; SCHALK KARL ING GRAD

Inventor(s): SCHALK KARL ING ; HARTMANN HANS HEINRICH DIPL ING

Title: Amplifier with feedback power control loop offset compensation

Abstract: A power amplifier has a feedback loop to control the signal level thereof. A current sensing amplifier in the feedback loop is controlled to remove any offset. The input signal is compared with a reference level. When the input signal is below the reference level, an offset compensation value for the current sensing amplifier is stored. When the input signal is above the reference level, the previously stored offset compensation value continues to be applied. The circuit is of particular application in a TDMA radio transmitter.

Classifications:
International (IPC 8-9): H03F1/34 H03F3/34 H03G1/04 H03G3/30 H04B1/04 (Advanced/Invention);
H03F1/34 H03F3/34 H04B1/04 (Advanced/Non-invention);
H03F1/34 H03F3/34 H03G1/00 H03G3/30 H04B1/04 (Core/Invention)
International (IPC 1-7): H03F1/30 H03F1/34 H03F3/34 H03G3/20 H04B1/04
CPC: H03G1/04 H03G3/3047
European: H03G1/04 H03G3/30D2B
US: 330/129 330/136



Family:

Publication number	Publication date	Application number	Application date
AT239323 E	20030515	AT20000956490T	20000825
AU200068411 A1	20010410	AU20000068411	20000825
AU200068411 A5	20010410	AU20000068411D	20000825
CN1373929 A	20021009	CN20008012695	20000825
DE60002494 D1	20030605	DE20006002494	20000825
DE60002494 T2	20040408	DE20006002494T	20000825
EP1219024 A1	20020703	EP20000956490	20000825
EP1219024 B1	20030502	EP20000956490	20000825
GB2354125 A1	20010314	GB19990021344	19990909
GB9921344 A0	19991110	GB19990021344	19990909
JP2003509887 T2	20030311	JP20010522662T	20000825
US6429739 BA	20020806	US20000658272	20000908
WO0118957 A1	20010315	WO2000EP08348	20000825

Priority:

GB19990021344 19990909 WO2000EP08348 20000825

Probable Assignee: OPTIS WIRELESS TECHNOLOGY LLC

Assignee(s): (std): ERICSSON TELEFON AB L M ; ERICSSON TELEFON AB LM ; ERICSSON TELEFON L M AB

Assignee(s): HIGHBRIDGE PRINCIPAL STRATEGIES LLC COLLATERAL AGENT AS ; OPTIS WIRELESS TECHNOLOGY LLC ; TELEFON AB LM ERICSSON ; TELEFON LM ERICSSON AB ; TELEFONAKTIEBOLAGET LM ERICSSON SE ; TELEFONAKTIEBOLAGET LM ERICSSON ; TELEFONAKTIEBOLAGET L M ERICSSON ; TELEFONAKTIEBOLAGET L M ERICSSON PUBL ; TELEFONAKTIEBOLAGET LM ERICSSON STOCKHOLM ; TELEFONAKTIEBOLAGET LM ERICSSON (PUBL) ; TELEFONAKTIEBOLAGET LM ERICSSON PUBL ; WILMINGTON TRUST NATIONAL ASSOCIATION ; CLUSTER LLC

Inventor(s): (std): OLSSON T ; OLSSON TORBJOERN ; OLSSON TORBJORN

Inventor(s): T OLSSON ; TORBJORN OLSSON

Agent(s): ASAMURA KIYOSHI; ASAMURA HAJIME; HAYASHI SEKIZO

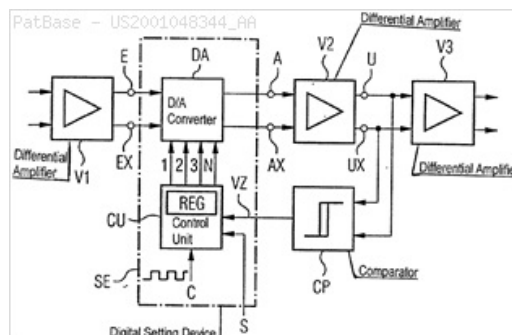
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Abstract: An offset voltage at an output of a differential amplifier is compensated for by a control circuit having a digital setting device. The control circuit has a control device which is controlled by an offset voltage of the differential amplifier and which feeds an offset compensation signal into the differential amplifier. Compared with analog compensation with an external storage capacitor, temporal drift effects do not distort the offset compensation on the differential 10 amplifier. The described principle can be applied, for example, in radio frequency receiver circuits.

International (IPC 8-9): H03F1/30 H03F3/45 (Advanced/Invention);
H03F1/30 H03F3/45 (Core/Invention)

European: H03F3/45S1A1 H03F3/45S3A3A1 H03F3/45S3A3C1
T03F203/45624 T03F203/45696

US: 330/259 330/9 330/9P



Publication number	Publication date	Application number	Application date
DE10023114 A1	20011129	DE20001023114	20000511
DE50115223 D1	20091231	DE20015015223	20010411
EP1154565 A2	20011114	EP20010109054	20010411
EP1154565 A3	20060719	EP20010109054	20010411
EP1154565 B1	20091118	EP20010109054	20010411
US2001048344 AA	20011206	US20010853471	20010511
US6710645 BB	20040323	US20010853471	20010511

DE20001023114 20000511

Probable Assignee: INTEL CORP

Assignee(s): (std): INFINEON TECHNOLOGIES AG ; SCHMAL JOSEF ; TRANKLE GUNTHER

Assignee(s): MEMMLER BERND ; ISKEN MARTIN ; INTEL MOBILE COMMUNICATIONS TECHNOLOGY GMBH ; INFINEON TECHNOLOGIES DELTA GMBH ; INTEL CORP ; INTEL DEUTSCHLAND GMBH ; INTEL MOBILE COMMUNICATIONS GMBH

Inventor(s): (std): ISKEN MARTIN ; MEMMLER BERND ; SCHMAL JOSEF ; TRAENKE GUENTHER ; TRAENKLE GUENTHER ; TRANKLE GUNTHER

Agent(s): VIERING JENTSCHURA AND PARTNER

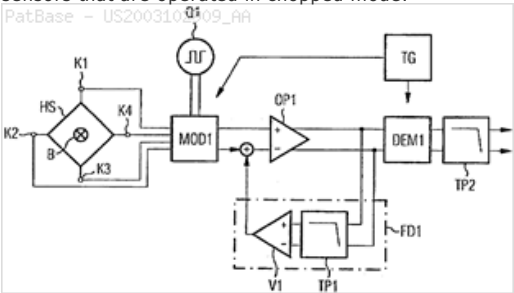
Designated states: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

Title: **Amplifier circuit with offset compensation**

Abstract: An **amplifier circuit with offset compensation** is particularly suited for a Hall element. In addition to the useful signal demodulation that is normally present and connected downstream of an amplifier, an error signal demodulator provides an error signal demodulation. The measured signals that are tapped off at the Hall sensor are coupled out at the input or output of the amplifier, and a demodulated error signal is fed back to the input of the amplifier. This makes it possible to reduce the drive range of the amplifier. The amplifier circuit is suitable in particular for Hall sensors that are operated in chopped mode.

Classifications:

International (IPC 8-9): G01R33/07 H03F1/30 H03F3/38 H03F3/45 H03H11/12 (Advanced/Invention); H03F1/30 (Advanced/Non-invention); H03F3/38 H03H11/04 (Core/Invention)
International (IPC 1-7): G01D5/20 G01R33/07 H03F1/02 H03F1/30 H03F1/34 H03F3/38 H03F3/45 H03H11/12
CPC: G01R33/07 G01R33/075 H03F3/38 H03F3/45973 H03F3/45977 H03F3/45995 H03F2200/261
European: G01R33/07 G01R33/07A1 H03F3/38 H03F3/45S3K3A H03F3/45S3K3A1 H03F3/45S3K3C1 T03F200/261
US: 324/251 327/124 330/6 330/9 330/9P



Family:

Publication number	Publication date	Application number	Application date
DE10032530 A1	20020124	DE20001032530	20000705
DE10032530 C2	20021024	DE20001032530	20000705
DE50108250 D1	20060105	DE20015008250	20010629
EP1297349 A1	20030402	EP20010953830	20010629
EP1297349 B1	20051130	EP20010953830	20010629
KR100508619 B1	20050817	KR20037000145	20010629
KR20030014750 A	20030219	KR20037000145	20010629
US2003102909 AA	20030605	US20030337194	20030106
US6674322 BB	20040106	US20030337194	20030106
WO0203087 A1	20020110	WO2001DE02438	20010629

Priority:

DE20001032530 20000705 DE20015008250 20010629 WO2001DE02438 20010629
WO2001DE002438 20010629

Probable Assignee: INFINEON TECHNOLOGIES AG

Assignee(s): (std): INFINEON TECHNOLOGIES AG ; MOTZ MARIO

Assignee(s): INFINEON TECHNOLOGIES PATENTABTEILUNG AG

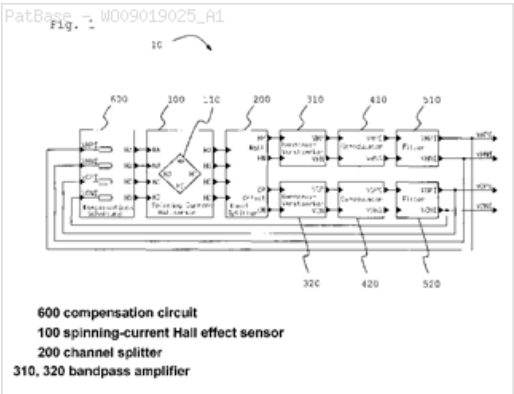
Inventor(s): (std): MOTZ MARIO

Designated states: AT BE CH CY DE DK ES FI FR GB GR IE IT JP KR LU MC NL PT SE TR US

Title: MEASURING INSTRUMENT COMPRISING A SPINNING-CURRENT HALL EFFECT SENSOR

Abstract: In order to increase the accuracy of measurements by means of a spinning-current Hall effect sensor and particularly reduce the influence of disturbance variables on the measurement, the invention relates to a measuring instrument comprising a spinning-current Hall effect sensor element (100) with at least one Hall effect sensor (110), and a channel splitter (200) which is connected to the outputs of the sensor element (100) and is used for supplying at least one first (HP-HN) and/or second (OP-ON) amplitude-modulated signal, the first signal encompassing a Hall voltage of the Hall effect sensor (110) caused by the Hall effect and the second signal encompassing an offset voltage as a useful signal. Said measuring instrument further comprises means (310) for the band-limited amplification of the first and/or second amplitude-modulated signal and a first demodulator (410) for demodulating the first amplified signal and/or a second demodulator (420) for demodulating the second amplified signal. An output of the first and/or second demodulator can be connected to the inputs of the sensor elements (100) by means of a compensation circuit (600) in such a way that the Hall voltage and/or the offset voltage of the Hall effect sensor (110) is/are substantially compensated. The invention further relates to a method for measuring a physical variable, especially by means of such a measuring instrument.

Classifications:
International (IPC 8-9): G01D5/14 G01R33/07
H03F1/34 (Advanced/Invention);
G01R33/06 (Core/Invention)
CPC: G01R33/07 G01R33/075 G01R33/10
European: G01R33/07 G01R33/07A1 G01R33/10



Family:

Publication number	Publication date	Application number	Application date
AT513226 E	20110715	AT20080785438T	20080807
DE202007010962 U1	20081218	DE200720010962U	20070807
DE502008003887 D1	20110721	DE200850003887T	20080807
EP2179299 A1	20100428	EP20080785438	20080807
EP2179299 B1	20110615	EP20080785438	20080807
WO09019025 A1	20090212	WO2008EP06534	20080807

Priority:

DE200720010962U 20070807 EP20080785438 20080807 WO2008EP06534 20080807

Probable Assignee: IC HAUS GMBH

Assignee(s): (std): HERZ MANFRED ; IC HAUS GMBH

Inventor(s): (std): HERZ MANFRED

Agent(s): BLUMBACH ZINNGREBE PATENT U RECHTSANWAELTE; KAMPFENKEL KLAUS

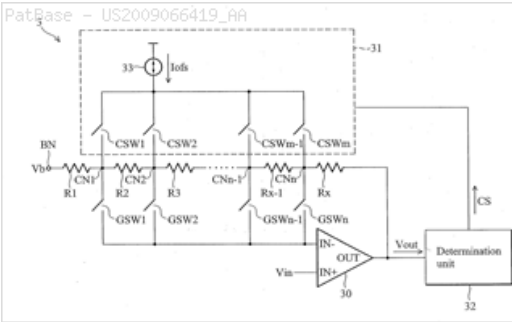
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Title: VARIABLE GAIN AMPLIFIER CIRCUITS

Abstract: A variable gain amplifier circuit has a variable gain amplifier (VGA), a string of resistors, a plurality of gain switches, a current source, and at least two current switches. A first input terminal of the VGA receives an input voltage signal. The string of resistors are coupled between an output terminal of the VGA and a bias voltage input terminal. Each of the gain switches is coupled between a second input terminal of the VGA and one of connection nodes between two of the resistors. Each of the current switches is coupled between the current source and one of the connection nodes. The current source provides a current through the turned-on current switch.

Classifications:

International (IPC 8-9): H03F1/36 H03G3/00 H03G3/20
H03G9/06 (Advanced/Invention);
H03G3/00 (Core/Invention)
CPC: H03F3/45475 H03F3/45941 H03F2203/45212 H03F2203/45528
H03F2203/45534 H03G1/0088
European: H03F3/45S1K H03F3/45S3K1A1 H03G1/00B8 T03F203/45212
T03F203/45528 T03F203/45534
US: 330/254 330/278 330/278P 330/282 330/86



Family:

Publication number	Publication date	Application number	Application date
CN101383596 A	20090311	CN200810215320	20080905
TW200913472 A	20090316	TW20080133568	20080902
US2009066419 AA	20090312	US20080056328	20080327
US7602239 BB	20091013	US20080056328	20080327

Priority:

US20070970268P 20070906 US20080056328 20080327

Probable Assignee: MEDIATEK INC

Assignee(s): (std): MEDIATEK INC

Inventor(s): (std): CHEN CHIEN MING ; HUANG CHIH CHIEN ; LEE WEI LIANG

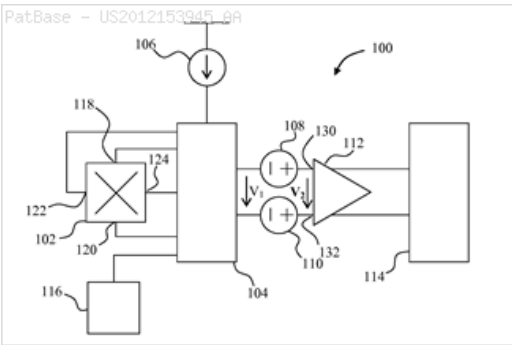
Agent(s): THOMAS KAYDEN HORSTEMEYER AND RISLEY LLP; THOMAS KAYDEN HORSTEMEYER AND RISLEY

Title: HALL EFFECT SENSOR WITH REDUCED OFFSET

Abstract: A Hall element sensor circuit in one embodiment includes a Hall element, a Hall element source, a switch matrix operatively connected to the Hall element and the Hall element source to establish a spinning current in the Hall element and to receive a Hall element signal from the Hall element based upon the spinning current, a front end amplifier including a first input operatively connected to a first switch matrix output and a second input operatively connected to a second switch matrix output, and at least one voltage source operatively connected to the front end amplifier at a location in the Hall element sensor circuit between the switch matrix and the front end amplifier.

Classifications:

International (IPC 8-9): G01R19/00 G01R33/00 G01R33/06
G01R33/07 (Advanced/Invention)
CPC: G01R33/0023 G01R33/0029 G01R33/07 G01R33/075
European: G01R33/00E G01R33/00E2 G01R33/07 G01R33/07A1
US: 324/123.00RS 324/123R 324/207.2 324/251 324/251P



Family:

Publication number	Publication date	Application number	Application date
DE602011009714 D1	20141016	DE201160009714T	20111210
DE602011024210 D1	20160428	DE201160024210T	20111210
EP2656091 A1	20131030	EP20110802618	20111210
EP2656091 B1	20140903	EP20110802618	20111210
EP2837946 A1	20150218	EP20140183049	20111210
EP2837946 B1	20160316	EP20140183049	20111210
EP3064954 A1	20160907	EP20160160426	20111210
US2012153945 AA	20120621	US20100974239	20101221
US8633687 BB	20140121	US20100974239	20101221
WO12087623 A1	20120628	WO2011US64294	20111210

Priority:

US20100974239 20101221 EP20110802618 20111210 EP20140183049 20111210
WO2011US64294 20111210

Probable Assignee: ROBERT BOSCH GMBH

Assignee(s): (std): BOSCH GMBH ROBERT ; EZEKWE CHINWUBA DAVID

Assignee(s): ROBERT BOSCH GMBH

Inventor(s): (std): EZEKWE CHINWUBA DAVID ; EZEKWE CHINWUBA

Inventor(s): EZEKWE CHINWUBA ALBANY

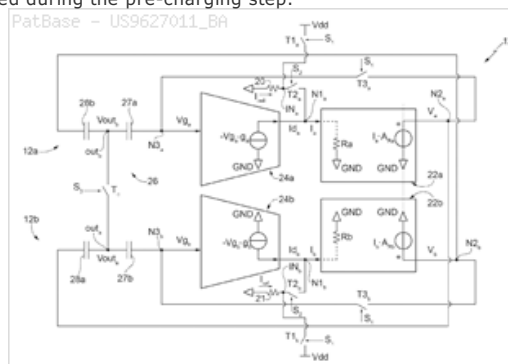
Agent(s): ISARPATENT PATENTANWELTE BEHNISCH BARTH CHARLES HASSA PECKMANN AND PARTNER MBB; BARTH STEPHAN MANUEL; ISARPATENT; MAGINOT MOORE AND BECK; MAGINOT PAUL J

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT QA RO RS RU RW SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Abstract: A method for operating a non-volatile memory device uses a sense amplifier that includes a first branch and a second branch. During a pre-charging step, a bit line of a memory array of the non-volatile memory device is biased in order to pre-charge the bit line. During the pre-charging step, an offset between the first branch and the second branch is detected and stored. During a reading step subsequent to the pre-charging step, a cell current is received from the bit line at the first branch and a reference current is received from a current-reference structure at the second branch. During the reading step, and amplified voltage is generated as a function of the cell current and the reference current. During the reading step, an output voltage is generated based on the amplified voltage compensated by the offset stored during the pre-charging step.

International (IPC 8-9): G11C13/00 G11C16/26 G11C7/02 G11C7/08
G11C7/12 H03F3/45 (Advanced/Invention)

CPC: G11C7/08 G11C7/12 H03F3/45968 H03F2203/45212 H03F3/45475
G11C7/062 G11C16/28 G11C16/26 G11C13/004



Publication number	Publication date	Application number	Application date
■ CN106782652 A	20170531	CN201610363597	20160526
■ CN205789124 U	20161207	CN201620499943U	20160526
■ EP3174200 A1	20170531	EP20160170438	20160519
■ EP3174200 B1	20180822	EP20160170438	20160519
■ ITUB20155867 A1	20170524	IT2015UB05867	20151124
■ US9627011 BA	20170418	US20160212211	20160716

IT201510000076148 20151124 IT2015UB05867 20151124

Assignee(s): (std) ST MICROELECTRONICS ROUSSET ; ST MICROELECTRONICS SRL ; STMICROELECTRONICS ROUSSET SAS ; STMICROELECTRONICS ROUSSET S A S ; STMICROELECTRONICS S R L

Inventor(s): (std): A CONTE ; F LAROSA ; LA ROSA FRANCESCO ; CONTE ANTONINO

Agent(s): NANNUCCI LORENZO; SLATER MATSIL LLP

Designated states: AL AT BA BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT
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