

11 Documents

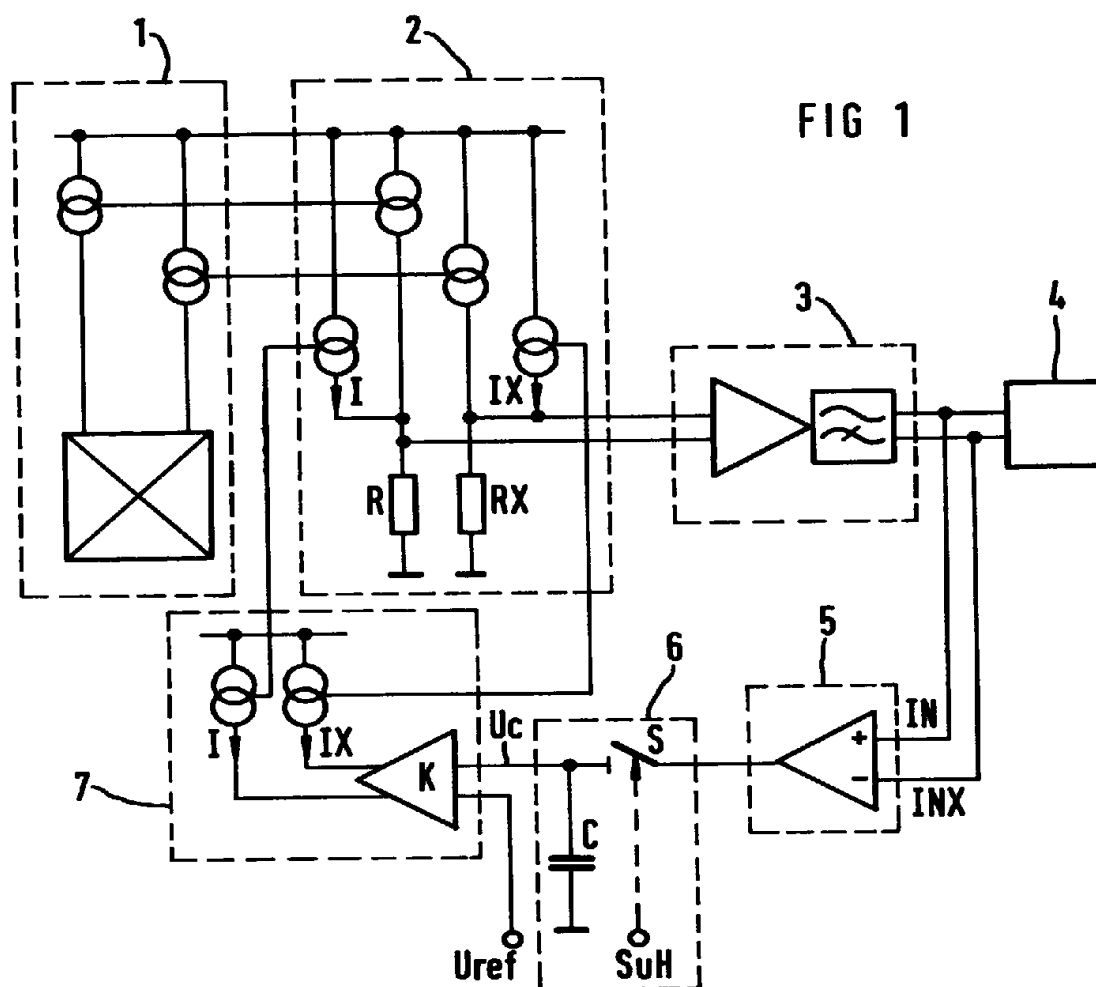
Publication numbers	Title	Current assignees
EP-693823 A1	Circuit especially for digital modulation apparatuses	INFINEON TECHNOLOGIES
FR2473810 A1	Method for compensating the drift voltage of an operational amplifier and resulting macro cell.	IBM
JP11088071 A	Offset voltage correction circuit	DENSO
US6069866 A	System and method for coarse gain control of wide band amplifiers	CIRRUS LOGIC
US5821795 A	Circuit for cancelling the DC offset in a differential analog front end of a read channel	IBM
NO9504729 D0	Sensor circuit and method for compensation	MOTOROLA
US5606320 A	Method and apparatus for micropower analog-to-digital conversion in an implantable medical device	PACESETTER
JP03034711 A	Self-zeroing amplifier	FAIRCHILD SEMICONDUCTOR
JP61039625 A	Analogue-to-digital converting apparatus for video signals	JAPAN VICTOR COMPANY
US4490682 A	Instrumentation amplifier having automatic offset adjustment	ANALOGIC
JP55108077 A	Zero reference and offset compensation circuit	VARIAN ASSOCIATES

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Title

(EP-693823)

Circuit especially for digital modulation apparatuses

Images**Publication data including kind & date**

EP0693823	A1	1996-01-24	EP-693823
EP0693823	B1	2001-04-18	EP-693823
DE59509199	D1	2001-05-23	DE59509199

**Abstract**

(EP-693823)

The circuit has a difference amplifier circuit (1), coupled to a filter circuit (3) via an output stage (2). The offset voltage for the filter circuit controls a regulating circuit (5, 6, 7) for providing an offset compensation signal (I, IX) for the output stage. Pref., the offset voltage and the offset compensation signal are provided as differential values, the offset voltage coupled to an amplifier (5), connected via a sample-and-hold stage (6) to the circuit (7) providing the offset compensation signal for the output stage. <IMAGE>

Inventors

FENK JOSEF DIPL-ING

SEHRIG PETER ING GRAD

Latest standardized assignees - inventors removed

INFINEON TECHNOLOGIES

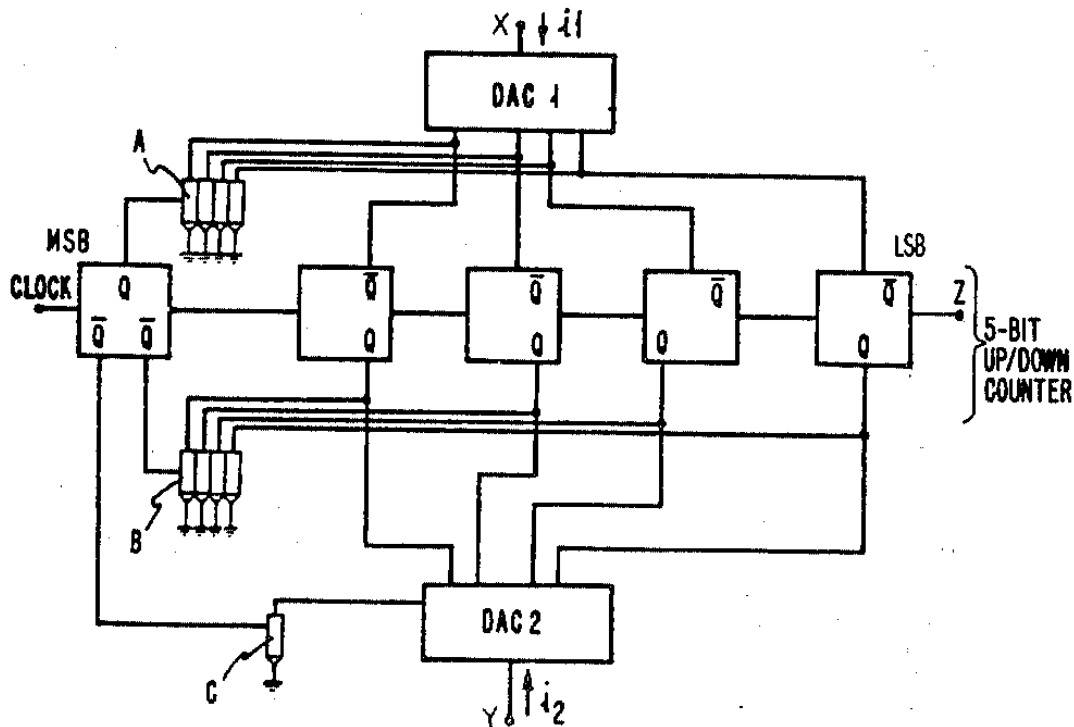
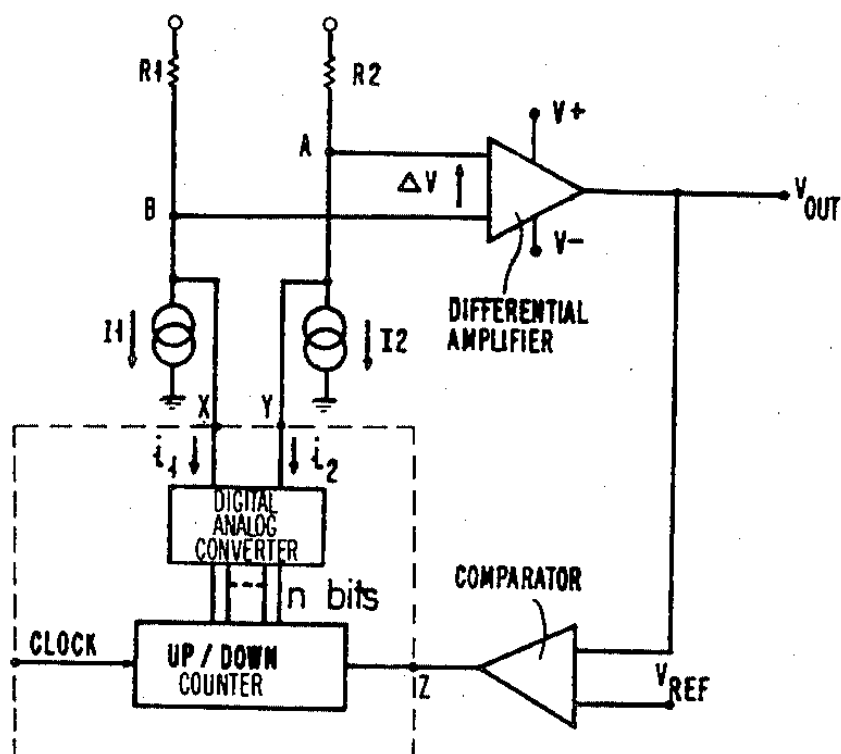
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Title

(EP--32551)

Method for compensating the drift voltage of an operational amplifier and resulting macro cell.

Images



Publication data including kind & date

FR2473810	A1	1981-07-17	FR2473810
EP0032551	A1	1981-07-29	EP--32551
FR2473810	B1	1982-04-09	FR2473810
US4395681	A	1983-07-26	US4395681



Abstract

(EP--32551)

A system is disclosed for compensating for the offset voltage problem which occurs in certain types of differential amplifiers; a differential amplifier, in the form of an operational amplifier, is provided with two generators of input signals whose difference is to be amplified; further included is an offset voltage compensation loop comprising a comparator, an n-bit up/down counter and a digital analog converter means; the output of said means being connected to said generators of input signals so as to modulate the input signals; and said digital analog converter means including first and second n-1 bit digital analog converters.

(From US4395681 A)

Inventors

HORNUNG ROBERT

LEBESNERAIS GERARD

Latest standardized assignees - inventors removed

IBM

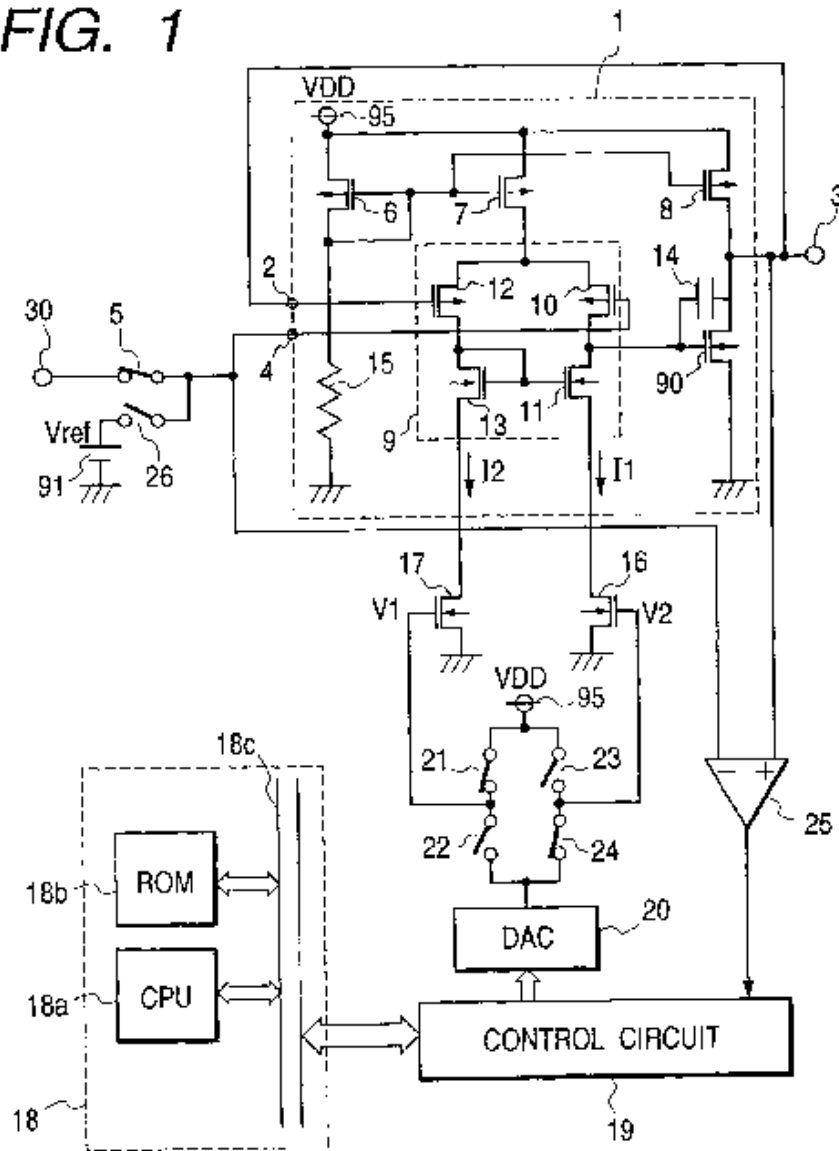
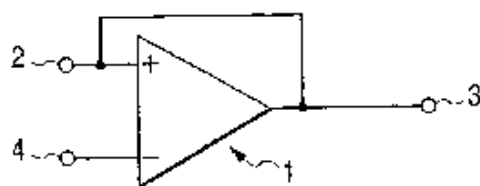
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Title

(US6054887)

Offset voltage correction circuit

Images

FIG. 1**FIG. 2****Publication data including kind & date**

JPH1188071	A	1999-03-30	JP11088071
US6054887	A	2000-04-25	US6054887
JP3514111	B2	2004-03-31	JP3514111

**Abstract**

(US6054887)

An offset voltage correction circuit for an operational amplifier (1) includes an offset voltage varying device (16, 17, 20, 21-23) for varying an offset voltage in the operational amplifier (1) in response to an offset voltage control value. A comparing device (25) operates for comparing an output voltage from the operational amplifier (1) with a prescribed reference voltage. A control device (19, 300) operates for outputting the offset voltage control value to the offset voltage varying device, for changing the offset voltage control value, for storing, in response to a result of the comparing by the comparing

device (25), a digital signal representative of the offset voltage control value at which the output voltage from the operational amplifier (1) and the prescribed reference voltage are equal, and for correcting the offset voltage in the operational amplifier (1) in response to the stored digital signal.

Inventors

HORIE MASAKIYO

HARADA TAKUYA

Latest standardized assignees - inventors removed

DENSO

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Title

(US6069866)

System and method for coarse gain control of wide band amplifiers

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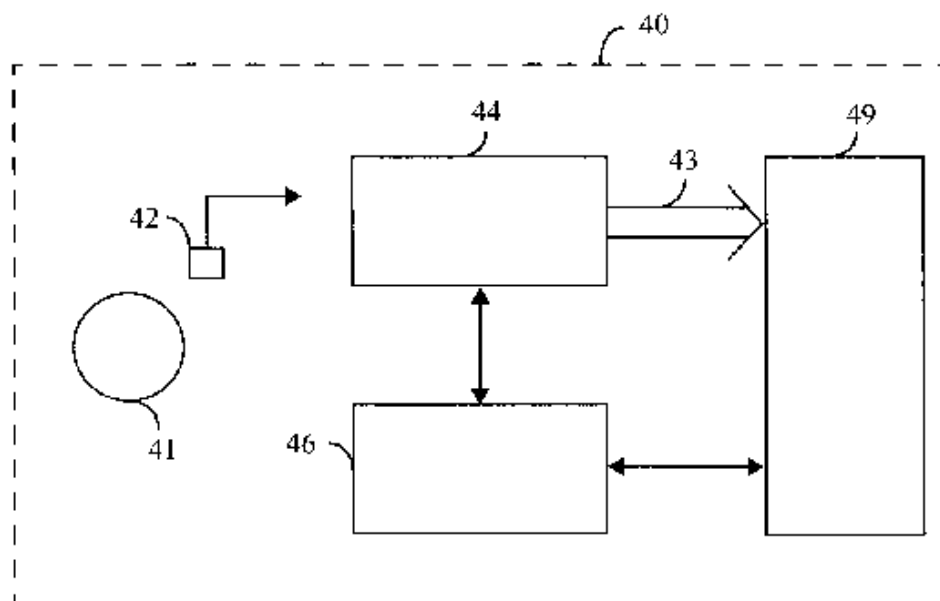


Fig. 1

Publication data including kind & date[US6069866](#)

A 2000-05-30 US6069866

**Abstract**

(US6069866)

A system and method for a data detection circuit is provided in which separate coarse gain amplifiers and fine gain amplifiers are utilized. The coarse gain amplifiers may include drain switching of transistors in order to modify the amplifier gain. More particularly, drain switching may be utilized to selectively switch in and out different differential input transistor pairs and/or different current sources. In this manner the gain of the amplifier may be adjusted to one of a variety of different coarse gain control levels. The coarse gain control provided allows for gain adjustments without significantly decreasing the bandwidth of the amplifier. In a preferred embodiment the system and method may be utilized for data detection circuits utilized in conjunction with optical disks.

Inventors

PIETRUSZYNSKI DAVID M

TESU ION CONSTANTIN

Latest standardized assignees - inventors removed

CIRRUS LOGIC

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Title

(US5821795)

Circuit for cancelling the DC offset in a differential analog front end of a read channel

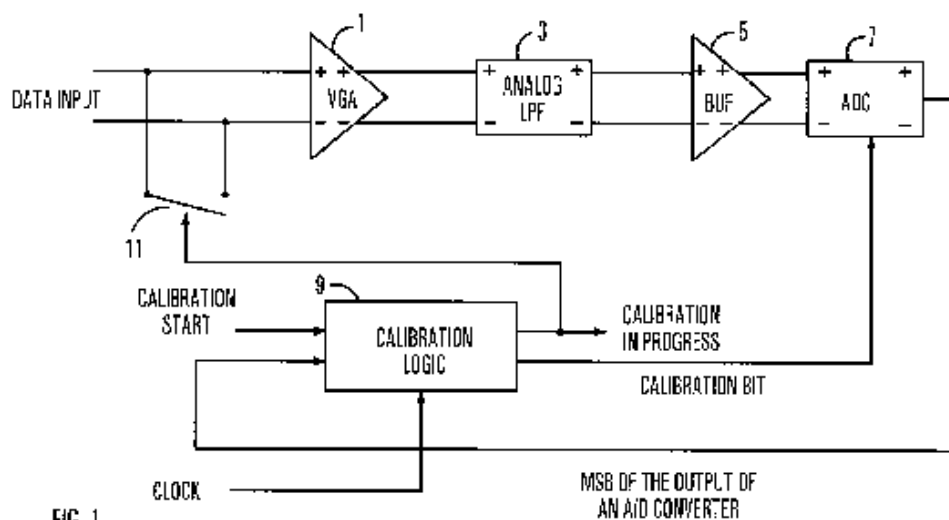
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FIG. 1
PRIOR ART

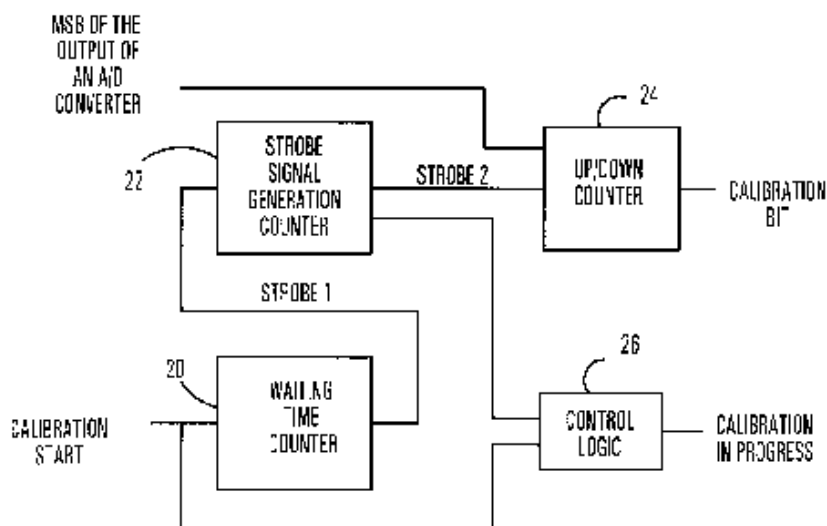


FIG. 2
PRIOR ART

Publication data including kind & date

US5821795

A 1998-10-13 US5821795

**Abstract**

(US5821795)

An analog front end for signal processing circuit such as a hard-disk data read channel having a calibration circuit for canceling DC offset is described. First, the DC offset is cancelled from a positive phase input to an A/D converter (ADC). Second, a DC offset is cancelled separately from a negative phase input to the A/D converter. The combined positive and negative phases form an amplified analog signal that is used as the differential input to the A/D converter. Finally, the DC offset in a path that encompasses the system analog input through the system digital output is cancelled. Controlling the buffer amplifier bias makes trimming unnecessary. It also enables faster calibration. Further, the two differential phase lines, i.e., the positive phase line and the negative phase line, are each calibrated in turn. As such, a common calibration circuit may be used, thereby avoiding circuit duplication.

Inventors

YASUDA TAKEO

ANDOH HAJIME

Latest standardized assignees - inventors removed

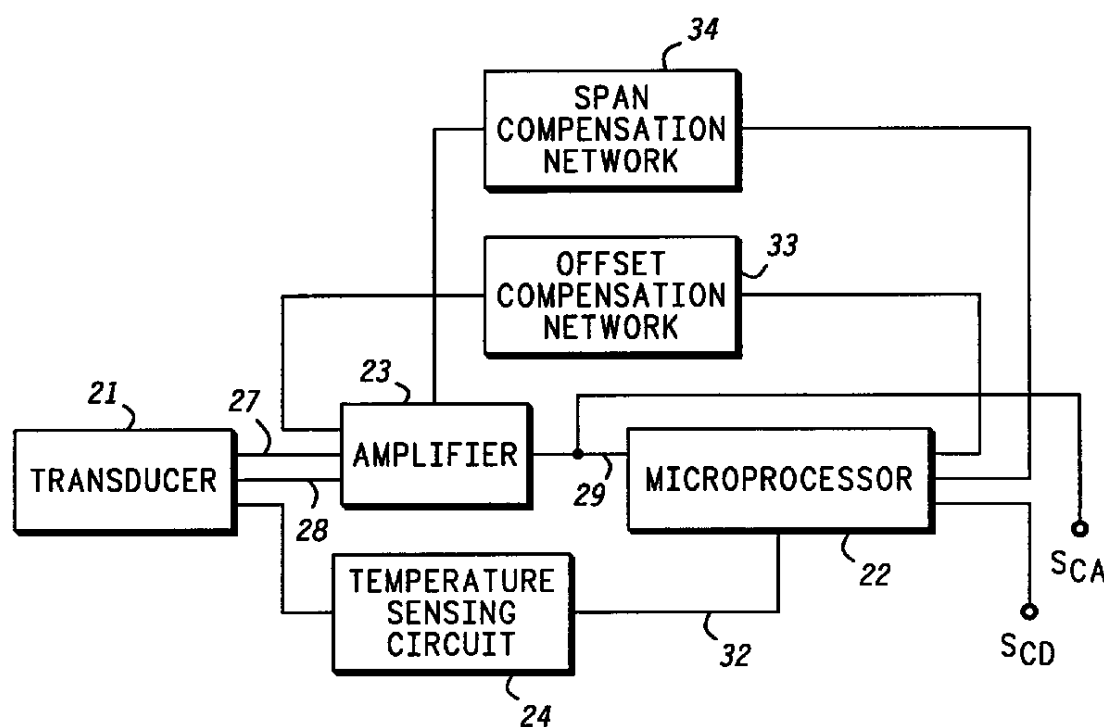
IBM

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Title

(EP-721099)

Sensor circuit and method for compensation

Images20**FIG. 2****Publication data including kind & date**

NO954729

D0 1995-11-23 NO954729

NO954729

A 1996-07-04 NO954729

EP0721099



(US5606320)

A micropower analog-to-digital converter (ADC) for use in an implantable medical device is disclosed. The ADC achieves a high conversion speed at micropower levels through a number of timing and circuit improvements over the conventional implementation of the successive approximation ADC architecture. The ADC includes a digital-to-analog converter (DAC) that preferably is implemented as a binary-weighted, switched capacitor array that employs top plate charging and performs bipolar conversion. The DAC provides an analog output signal representing array charge to a comparator. During a comparator latch phase, the DAC asynchronously determines a bit of the ADC digital output signal in response to the comparator output, and initiates a test of the next least significant bit during the same latch phase. Further, the DAC analog output signal is timed to settle during the latch phase in response to both the bit update and the next bit test. In conjunction with increasing conversion speed, the DAC reduces power requirements by using a power gated buffer that selectively increases the power of the ADC input signal only when necessary to drive the ADC conversion circuitry. Further, the comparator includes a precharged static memory cell to avoid crossover currents. Finally, the ADC includes a digital offset correction DAC that corrects not only the cumulative offset voltage generated by components of the ADC, but also the offset voltage of any device that provides the ADC input.

Inventors

KLEKS JONATHAN A

Latest standardized assignees - inventors removed

PACESETTER

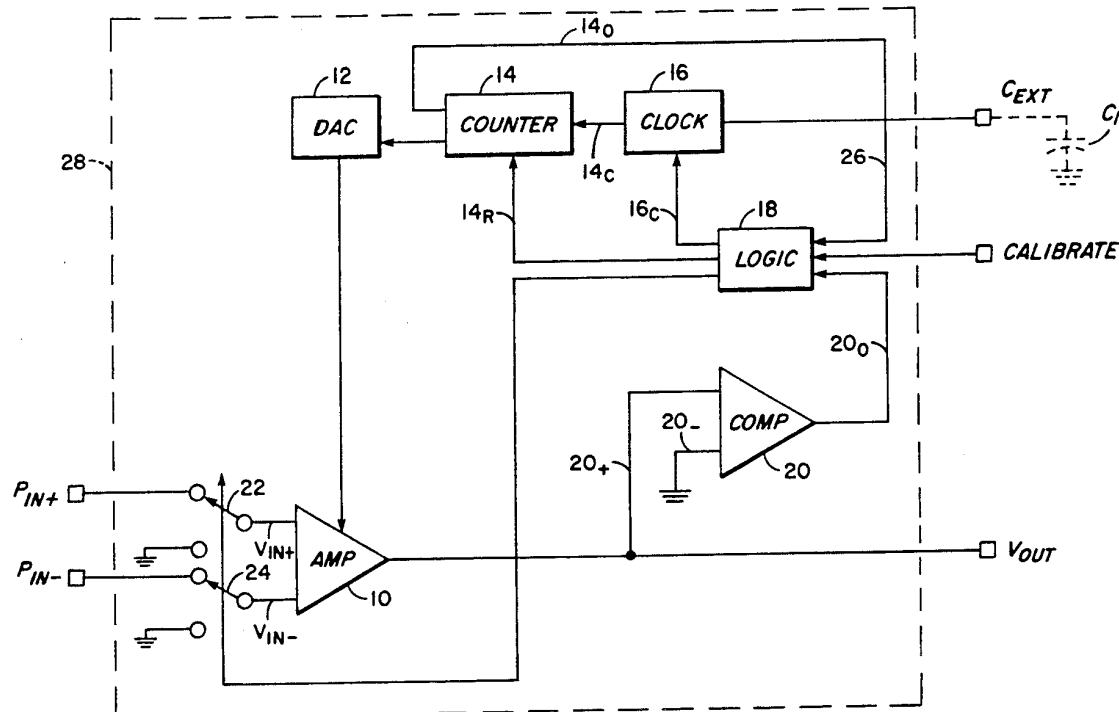
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Title

(US5061900)

Self-zeroing amplifier

Images



Publication data including kind & date

JPH0334711

A 1991-02-14 JP03034711

US5061900

A 1991-10-29 US5061900



Abstract

(US5061900)

A precision amplifier that, in response to digital inputs, zeros its offset voltage. The precision amplifier comprises a

traditional amplifier; a current source controlled by a counter; a comparator; test switches; and control logic. A digital input, such as might be generated from a microprocessor, initiates the offset adjustment. The test switches disconnect the amplifier inputs from external package connections and connect the inputs together. The counter begins to count, changing the current produced by the current source at each count. The current from the current source is applied to the offset adjust circuit of the amplifier which changes the offset voltage as the current changes. The counter counts until the comparator indicates the offset voltage has been zeroed. Alternative embodiments allow the precision amplifier to adjust for offset introduced by circuitry connected to the input and the output of the precision amplifier.

Inventors

VINN CHARLES L

SEGARAM PARA K

Latest standardized assignees - inventors removed

FAIRCHILD SEMICONDUCTOR

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Title

(EP-178044)

Analogue-to-digital converting apparatus for video signals

Images

analog video signal supplied thereto, an amplifying circuit (33) for amplifying an output signal of the clamping circuit, an analog-to-digital converting circuit (34) for generating a digital video signal by subjecting an output signal of the amplifying circuit (33) to an analog-to-digital conversion, and a control signal generating circuit (35, 36) for generating at least for the duration of a horizontal synchronizing signal of the input analog video signal a control signal responsive to a difference between the value of the output digital video signal of the analog-to-digital converting circuit (34) and the value of a preset reference signal. The control signal is supplied to one or two out of the clamping circuit (32), the amplifying circuit (33), and the analog-to-digital converting circuit (34) to variably control one or two out of a clamping voltage of the clamping circuit (32), an offset voltage of the amplifying circuit (33), and a first reference voltage of the analog-to-digital converting circuit (34) so that the value of the difference becomes a minimum.

Inventors

FURUKI, TSUNEO

SUZUKI, FUJIO

Latest standardized assignees - inventors removed

JAPAN VICTOR COMPANY

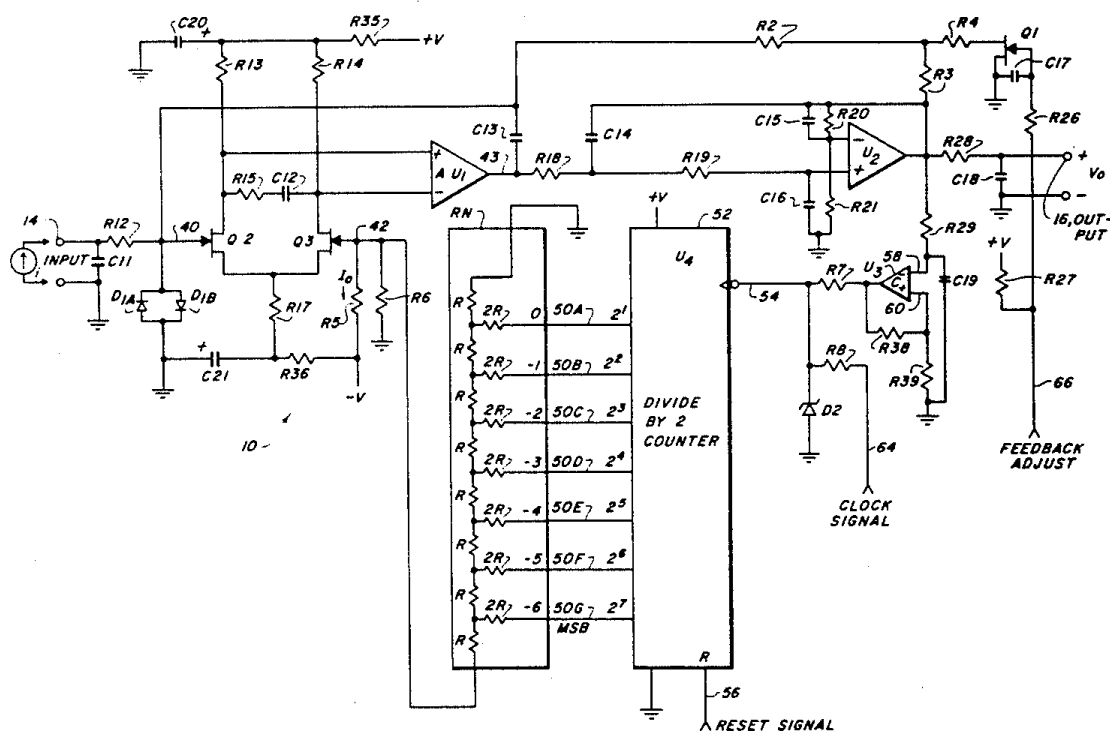
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Title

(US4490682)

Instrumentation amplifier having automatic offset adjustment

Images



Publication data including kind & date

US4490682

A 1984-12-25 US4490682



Abstract

(US4490682)

An instrumentation amplifier having automatic offset error adjustment to null unwanted DC output signals. The DC gain of the instrumentation amplifier is first increased by reducing the internal negative feedback which increases the amplitude of unwanted DC signals; thereafter, an offset correction signal is provided to reduce the unwanted DC signals. The normal operating DC gain is restored and the unwanted DC output signal is further reduced.

Inventors

POULO LOUIS

Latest standardized assignees - inventors removed

ANALOGIC

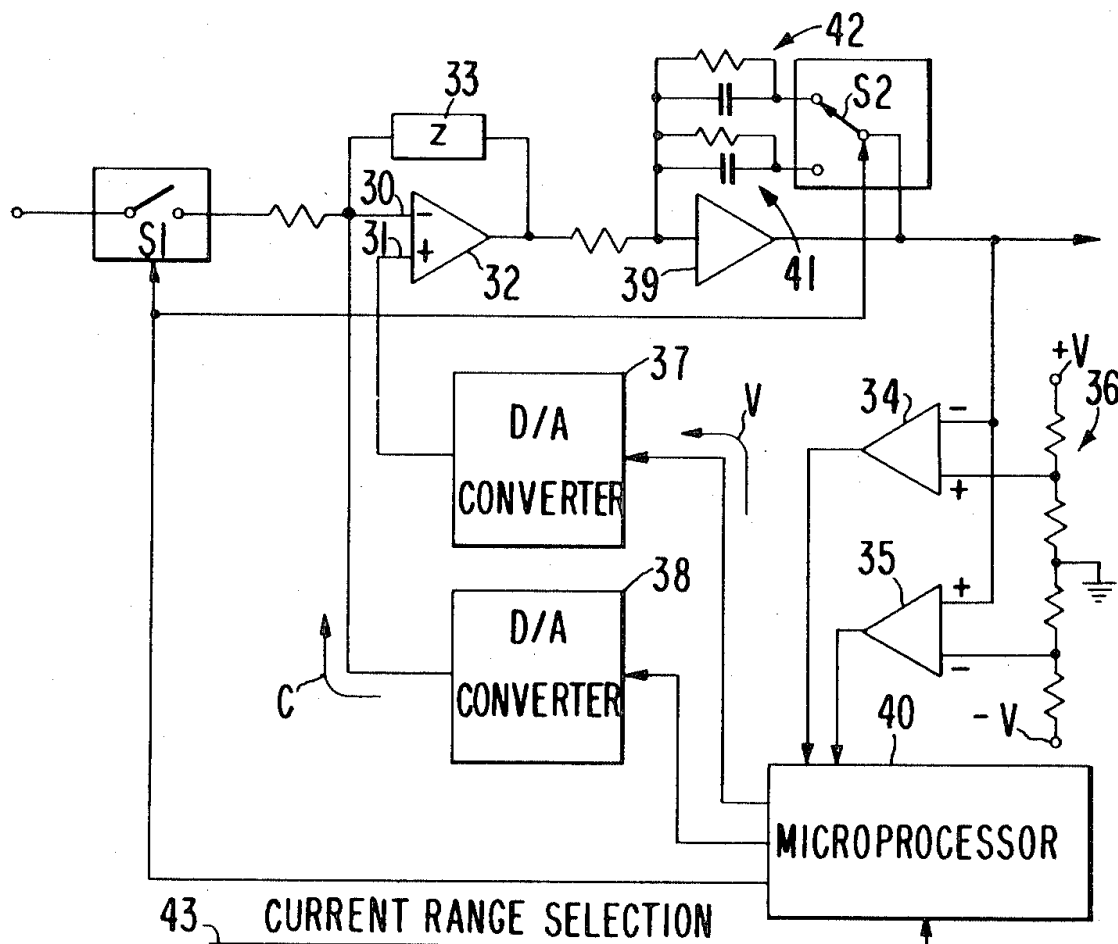
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Title

(US4229703)

Zero reference and offset compensation circuit

Images



Publication data including kind & date

JPS55108077

A 1980-08-19 JP55108077

US4229703

A 1980-10-21 US4229703



Abstract

(US4229703)

A zero reference and offset compensation circuit for an operational amplifier operating in the inverting mode in order to correct for both current and voltage offset errors. The zero reference and offset compensation circuit includes comparators for comparing the zero condition output of the operational amplifier with representations of lower and upper boundary signal levels, a pair of digital-to-analog converters having their respective analog outputs connected through appropriate scaling networks to the inverting input terminal and to the non-inverting input terminal of the operational amplifier, a microprocessor connected to the output of the comparators for providing an input to the associated digital-to-analog converter so it produces an incremented digital signal whenever the comparators indicate the zero condition signal output exceeds either boundary signal level, the incremented digital signal being incremented in a direction to drive the associated digital-to-analog converter in a direction to bring said zero condition signal within the boundary which has been exceeded. The microprocessor has a current range selection capability so that the digital-to-analog converter connected to the inverting terminal is incremented for nanoampere range signal currents and the digital-to-analog converter associated with the non-inverting terminal is incremented for signal currents in the microampere range and above.

Inventors

BUSTIN RAPHAEL

Latest standardized assignees - inventors removed

VARIAN ASSOCIATES