



New connection on: : 28-09-2018 : 00:15:27 - Last disconnection on: : 27-09-2018 : 02:08:26

V 4.0.0.44358(LP,U,linux) (Rev:43856 2017-04-27 09:03:29 +0200#(D201802)) (RPM D201802)

Welcome to EPOQUE Rebuild under the Production Environment

[No database/cluster active] ..fi epodoc

 Database: EPODOC

[EPODOC: SS 1] offset and circuit

Results in EPODOC **32.757**

[SS 2] 1 and compensation

Results in EPODOC **2.790**

[SS 3] 2 and digital

Results in EPODOC **526**

[SS 4] 3 and state

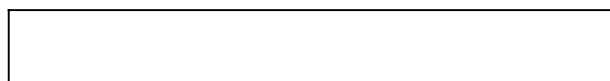
Results in EPODOC **24**

[SS 5] ..li



1/24 © EPODOC / EPO

PN - [CN107482722](#) A 20171215
PR - CN20171739758 20170825
AP - CN20171739758 20170825
DT - I
CNOI - [H02J7/0077](#)
PA - UNIV XIDIAN
TI - Constant current charger **circuit**
AB - The invention discloses a
constant current charger **circuit**,
solving the problems of charging



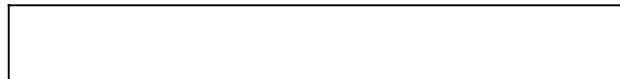
current precision and **circuit** stability caused by **offset** voltage in the process of lithium battery charging. The constant current charger **circuit** is characterized in that a sampling unit (2) samples a charging unit (1) to obtain a sampling current signal IBFETH; a switched capacitor **circuit** unit (3), a voltage **compensation** unit (4) and a signal conversion unit (5) form negative feedback to ensure the sampling precision. The sampling current signal IBFETH is converted into a sampling voltage by the signal conversion unit (5) and output to a charging current adjustment unit (6). The charging current adjustment unit (6) obtains the charging current adjusting signal according to the sampling voltage and feeds back the obtained signal to the charging unit (1) for controlling and adjusting the magnitude of the constant current charging current. A **digital** control unit (7) is used to switch the working **state** of the switched capacitor **circuit** unit (3) to eliminate the influence of the **offset** voltage of an operational amplifier. The constant current charger **circuit** makes the charging current maintain accurate and stable under different **offset** voltages, and can be used for a lithium battery charger.

2/24 © EPODOC / EPO
 PN - [CN107222227](#) A 20170929
 PR - CN20171506929 20170628
 AP - CN20171506929 20170628
 DT - I
 CNOI - [H04B1/005](#) ; [H04B1/16](#)
 PA - UNIV SCIENCE & TECHNOLOGY CHINA

TI	- Radio frequency receiving front end with digital auxiliary circuit
AB	- The invention discloses a radio frequency receiving front end with a digital auxiliary circuit for realizing a programming adjustment of conversion gain and input matching. The radio frequency receiving front end with the digital auxiliary circuit comprises a main transconductance module (1), a transconductance enhancement module (2), a matching compensation module (3), a switching tube and load module (4) and a digital auxiliary module (5). According to the radio frequency receiving front end, the transconductance enhancement module and the matching compensation module are added to the main transconductance module for respectively improving the total conversion gain and realizing input matching compensation . The digital auxiliary module is imported for performing dynamic offset on the transconductance enhancement module and the matching compensation module at different working state demands of the radio frequency front end. Therefore, the transconductance enhancement amount and the matching compensation amount of the radio frequency front end are dynamically controlled so as to realize the programming adjustment of conversion gain and input matching. The radio frequency receiving front end is simple in structure, easy to integrate and small in chip occupation area.

3/24 © EPODOC / EPO

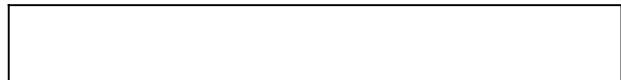
PN	- CN105699989 A 20160622
PR	- CN201511034552 20151231
AP	- CN201511034552 20151231
DT	- I
CNOI	- G01S19/235
PA	- TECHTOTOP MICROELECTRONICS TECH CO LTD
TI	- Method for Beidou RDSS terminal Doppler frequency compensation and terminal
AB	- The invention provides a method for Beidou RDSS terminal Doppler frequency compensation . The method includes the following steps: when the terminal is in a static state , local crystal oscillator frequency offset of the terminal is calculated; when the terminal moves at high speed, the local crystal oscillator frequency offset and a carrier frequency control word output by and a digital receiving circuit (4) are utilized to calculate an emitting code NCO frequency control word and emitting PLL parameters, the emitting code



NCO frequency control word is utilized to control emitting code NCO output, and the emitting PLL parameters are utilized to control BPSK modulation. After adoption of the abovementioned technical scheme, a user terminal radio frequency **circuit** is the same as an ordinary user terminal **circuit**, can use a market mainstream RDSS radio frequency chip, and a user terminal can stably and reliably realize an RDSS service request under a high dynamic condition only by modification of software. Compared with the prior art, the technical scheme has the advantages of simple **circuit** structure, strong universality, small size and low power consumption.

4/24 © EPODOC / EPO

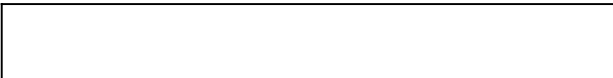
PN - [KR20150120197](#) A 20151027
 PR - KR20140046137 20140417
 AP - KR20140046137 20140417
 DT - I
 CNOI - [H04B1/18](#) ; [H04L7/0087](#) ;
[H04L25/026](#) ; [H04L25/0264](#) ;
[H04L27/0002](#) ; [H04L27/2338](#) ;
[H04L27/3881](#)
 PA - KOREA ASTRONOMY & SPACE
 SCIENCE INST [KR]
 TI - RADIO SIGNAL PROCESSING
 SYSTEM INVOLVED HIGH SPEED
 SAMPLER
 AB - According to the present
 invention, a control method of
 using two MPUs for parallel
 control is adopted for real-time
 control, and a reference
 sampling clock and the number
 of **digital** conversion bits can be
 varied remotely or on-board. In
 order to synchronize bits which
 are digitally converted at an



ultrahigh speed, functions of adjusting a delay time **compensation** algorithm and 256-level **digital** signal **offset** are designed. The radio signal processing system includes a variable bit distribution monitoring function for monitoring a **state** that a radio signal is converted into a **digital** signal. The present invention relates to a radio signal processing system having an ultrahigh speed sampler which includes a **circuit** design, configuration and production of a PCB, and a firmware.

5/24 © EPODOC / EPO

PN - [CN104283558](#) A 20150114
 PNFP - CN104283558B B 20170620
 PR - CN20131284696 20130708
 AP - CN20131284696 20130708
 DT - I
 CT - || STSE (A)
[CN101083451](#) A 20071205
 [X] (INST OF MICROELECTRONICS CAS [CN])
 [X] 1-4,7-10
 * 权利要求1-4,说明书第3页第3段 *;
[CN103023437](#) A 20130403
 [A] (UNIV TSINGHUA GRADUATE SCHOOL)
 [A] 1-10
 * 全文 *;
[CN103036512](#) A 20130410
 [A] (UNIV TSINGHUA GRADUATE SCHOOL)
 [A] 1-10
 * 全文 *
 PA - (A)
 UNIVTSINGHUA
 TI - (A)
 High-speed comparator direct-current **offset digital** auxiliary self-calibration system and



control method

AB - (A)

The invention discloses a high-speed comparator direct-current **offset digital** auxiliary self-calibration system and a control method. The system is formed by a configurable comparator comprising a **compensation** current source array, a self-calibration **digital** algorithm module and a time sequence signal generating **circuit**. The self-calibration **digital** algorithm module can generate two sets of **digital** signals in a symbolic coding mode according to output digits of the configurable comparator to control the opening and closing **state** of the **compensation** current source array, and thus the direct current **offset** voltage of the comparator can be calibrated to be within the adjustable precision range. The pre-amplifier stage bandwidth in the comparator can be configured so that power consumption under different sampling rates can be optimized.

6/24 © EPODOC / EPO

PN - [KR20140067408](#) A 20140605

PR - KR20120134595 20121126

AP - KR20120134595 20121126

DT - I

CCI - [H04N5/361](#) ; [H04N5/378](#)

PA - SAMSUNG ELECTRONICS CO LTD
[KR]

TI - SOLID **STATE** PICK-UP DEVICE AND
CONTROL METHOD THEREFORE

AB - A solid image pick-up device
having a dark **offset**
compensation circuit is
disclosed. The solid image pick-



up device comprises: a pixel array; an A/D conversion unit for converting a pixel signal corresponding to charges accumulated to a photoelectric conversion element into a **digital** signal; a ramp signal generator for generating a ramp signal in response to a control signal to be used for A/D conversion; and a dark **offset compensation circuit** for compensating dark **offset** by using a gain setting value and dark **offset** to perform processing of an input signal only in a full range of an input signal level by being connected to the A/D conversion unit and the ramp signal generator. Thereby, burden on the **circuit** can be reduced while the dark **offset compensation** is performed more efficiently.

7/24 © EPODOC / EPO

PN - [US2014146210](#) A1 20140529

PR - KR20120134595 20121126

AP - US201314067293 20131030

DT - *; Rep

CT - || R141 (A1)

[US2003202111](#) A1 [];

[US2012019697](#) A1 [];

[US2011279724](#) A1 [];

[US2008055432](#) A1 [];

[US2011025871](#) A1 [];

[US2011019047](#) A1 [];

[US2011205386](#) A1 [];

[US2012038809](#) A1 [];

[US2009021411](#) A1 [];

[US2008284886](#) A1 [];

[US2005057389](#) A1 []

CCI - [H04N5/361](#) ; [H04N5/378](#)

PA - SAMSUNG ELECTRONICS CO LTD
[KR]

TI - SOLID **STATE** IMAGING DEVICES
AND METHODS USING SINGLE
SLOPE ADC WITH ADJUSTABLE

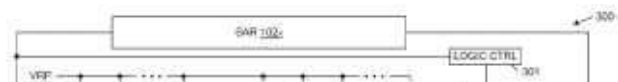


SLOPE RAMP SIGNAL

- AB - A solid **state** imaging device includes a pixel array comprising a plurality of photoelectric conversion devices and an analog to **digital** conversion (ADC) **circuit** configured to convert an image signal received from the pixel array to a **digital** signal responsive to a ramp signal and a gain setting. The solid **state** imaging device further includes a ramp signal generator **circuit** configured to generate the ramp signal with a slope that varies responsive to a control signal and a dark level **offset compensation circuit** configured to generate the control signal responsive to the gain setting and a dark level measurement.

8/24 © EPODOC / EPO

- PN - [US2011148675](#) A1 20110623
- PNFP - US8031099 B2 20111004
- PR - US20090645488 20091223
- AP - US20090645488 20091223
- DT - *; Rep
- CT - || STSE (B2)
[US5684487](#) A 19971104 [] (TIMKO MICHAEL P [US])
[US5745194](#) A 19980428 [] (NAKASHIMA KOHJI [JP], et al)
[US6255909](#) B1 20010703 [] (MUZA JOHN M [US])
[US6437720](#) B1 20020820 [] (YIN GUANGMING [US], et al)
[US6630834](#) B2 20031007 [] (MIN DONG-KI [KR], et al)
[US6977607](#) B2 20051220 [] (LEUNG KA Y [US], et al)
[US7821433](#) B2 20101026 [] (ABE AKIRA [JP])
[US2004257256](#) A1 20041223 [] (LEUNG KA Y [US], et al)
[US2009243901](#) A1 20091001 []

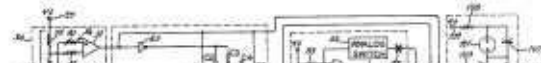


	] (ABE AKIRA [JP]) - R141 (A1) US5745194 A []; US6255909 B1 []; US6437720 B1 []; US6630834 B2 []; US2009243901 A1 []; US7821433 B2 []; US5684487 A []; US2004257256 A1 []; US6977607 B2 []
CCI	- H03M1/1033
CCA	- H03M1/468 ; H03M1/68
PA	- (A1 B2)
TI	INTEGRATED DEVICE TECH [US] - (A1 B2) Analog/Digital Or Digital/Analog Conversion System Having Improved Linearity
AB	- (A1 B2) A digital-to-analog converter (DAC) circuit includes a least significant bit (LSB) set of capacitors, each commonly coupled to an LSB node, and a most significant bit (MSB) set of capacitors, each coupled to an MSB node. A section-coupling capacitor couples the LSB and MSB nodes. The LSB node exhibits a parasitic capacitance, which tends to introduce a jump error voltage. Digital input signals are applied to the LSB and MSB capacitors, and in response, an analog output signal is developed on the MSB node. A compensation capacitor coupled to the MSB node has a compensation capacitance selected to offset the jump error voltage introduced by the parasitic capacitance. The compensation capacitor is enabled when all of the LSB capacitors are coupled to digital input signals having a logic '0' state. Otherwise,

the **compensation** capacitor is disabled (e.g., left in a floating **state**).

9/24 © EPODOC / EPO

- PN - [US4203095](#) A 19800513
- PR - US19770856278
19771201; US19760722409
19760913
- AP - US19770856278 19771201
- DT - *
- CT - [US3454787](#) A []; [US3582925](#) A [];
[US3641547](#) A []; [US3673588](#) A [];
[US3786501](#) A []; [US3801972](#) A [];
[US3976985](#) A []
- CCI - [G08B29/06](#) ; [G08B29/10](#)
- PA - POTTER ELECTRIC SIGNAL
- TI - Monitoring apparatus for direct wire alarm system
- AB - For monitoring the supervisory current in a communications line between a power source and a protected premises which forms a security protection **circuit**, monitoring apparatus utilizes sensitive solid **state** circuitry which appears transparent to the protection **circuit**. An operational amplifier input **circuit** protects the circuitry against component damage due to lightning, inherently rejects common mode errors due to noise, transients, and varying power supply voltage, and had an adjustable **offset** for line length **compensation** and **circuit** standardization. Voltage comparator circuitry indicates by **digital** signals the supervisory current level. After the operator conditions the apparatus for an abnormal current level which



has been signalled, a lamp which blinks at a discernable rate is used to serve as a reminder of this **state**. Filtering circuitry detects and indicates the presence of a predetermined frequency oscillating current imposed in the communications line at the protected premises, producing a **digital** output. A plurality of such **digital** outputs may be conveniently processed by a microprocessor.

10/24 © EPODOC / EPO

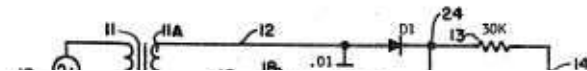
- PN - [US5179379](#) A 19930112
- PR - EP19910300417 19910118
- AP - US19910779679 19911021
- DT - **
- CT - [US4618848](#) A []; [EP0103468](#) A2 [];
[EP0201415](#) A1 []; [DE3202497](#) A1 []
- CCI - [G01G23/3714](#) ; [G01L1/2256](#) ;
[G06F3/0383](#) ; [H03M1/0607](#)
- CCA - [H03M1/12](#)
- PA - IBM [US]
- TI - Analog to **digital** convertor with drift **compensation**
- AB - An analog to **digital** convertor (20) comprises an amplifier (100) for amplifying an analog input signal to generate an amplified output signal. A conversion means (110) periodically samples the amplified output signal to generate a **digital** word as a function of each sample. A **compensation** means, preferably including a microcontroller logic **circuit** (130), compensates for drift in the output signal steady **state** level of the amplified output signal. The **compensation** means includes a tracking means (130)



for summing a **digital offset** value and the **digital** word in response to, and to compensate for, the drift in the output signal level between upper and lower limits. The **compensation** means also includes a bias means (130,140) for changing a bias signal level at the input of the amplifier (100) in response to, and to compensate for, the drift extending beyond the limits. The **compensation** means further includes a logic means (130,190) for modifying the **digital** word in response to, and to compensate for, the step change.

11/24 © EPODOC / EPO

- PN - [US3914689](#) A 19751021
- PR - US19740467581 19740506
- AP - US19740467581 19740506
- DT - *
- CT - [US1966047](#) A []; [US2137846](#) A []; [US2198226](#) A []; [US2294065](#) A []
- CCI - [G01R19/22](#) ; [G01R21/10](#)
- PA - WRIGHT CHARLES S
- TI - Self powering temperature compensated rectifier for measuring current
- AB - The current measuring device provides for measuring the power in radio frequency waves without requiring any source of power for the measuring device except the radio waves themselves, and the device includes a rectifier to change alternating current to direct current by a solid **state** diode, but a solid **state** diode has an **offset** voltage of approximately 0.4 volt and to provide **compensation** for this **offset** a second diode is used in opposed relation to the first diode and the second diode



is powered from the source of alternating current by a third diode so the resulting voltage from the device is linear and the extrapolation of the linearity passes through the origin of the graph thereby providing for measuring currents with extreme accuracy over a large temperature range without requiring an additional source of power and without requiring thermistors or bolometers. The output of the **circuit** can be directly applied to an analog/ **digital** converter (A/D converter) to obtain a **digital** reading of the analog of the **circuit**.

12/24 © EPODOC / EPO

PN - [US2003086516](#) A1 20030508
 PNFP - US6823024 B2 20041123
 PR - EP20000109738
 20000508; WO2001EP05218
 20010508
 AP - US20020291012 20021108
 DT - **
 CT - || STSE (B2)
[US4272845](#) A 19810609 [
] (FIUMANI FRANCESCO)
[US4779225](#) A 19881018 [
] (FUKASAWA ATSUSHI [JP], et al)
[US5187445](#) A 19930216 [
] (JACKSON H SPENCE [US])
[US5245646](#) A 19930914 [
] (JACKSON H SPENCE [US], et al)
[US5473278](#) A 19951205 [
] (SHIBATA HIROHIKO [JP])
[US5914633](#) A 19990622 [
] (COMINO VITTORIO [US], et al)
[US6118829](#) A 20000912 [
] (NORTH BRIAN B [US])
[US6181740](#) B1 20010130 [
] (YASUDA AKIRA [JP])
 - || R141 (A1)
[US6181740](#) B1 [];



[US5187445](#) A [];

[US4272845](#) A [];

[US5914633](#) A [];

[US5245646](#) A [];

[US6118829](#) A [];

[US4779225](#) A [];

[US5473278](#) A []

- CCI - [H04L25/063](#)
- PA - (B2)
INFINEON TECHNOLOGIES AG [DE]
- TI - (A1 B2)
Compensation circuit and
method for compensating for
an **offset**
- AB - (A1)
To demodulate an amplitude-
modulated signal having
an **offset**, two time constants are
provided in a filter unit. The
filter unit has two analog
or **digital** low-pass filters or high-
pass filters. A first switch is used
to change over between the two
time constants. If a plurality of
bits having the same **state**
succeed one another in a setting
mode, the first switch is used to
change over to a slower time
constant so as not to corrupt the
threshold voltage that is to be
ascertained. In a normal mode,
the stored threshold voltage is,
then, used to distinguish
between the states coded in an
input signal. In such a context,
the slower time constant is valid
in the normal mode.
- (B2)
To demodulate a frequency-
modulated signal having
an **offset**, two time constants are
provided in a filter unit. The
filter unit has two analog
or **digital** low-pass filters or high-
pass filters. A first switch is used
to change over between the two
time constants. If a plurality of
bits having the same **state**

succeed one another in a setting mode, the first switch is used to change over to a slower time constant so as not to corrupt the threshold voltage that is to be ascertained. In a normal mode, the stored threshold voltage is, then, used to distinguish between the states coded in an input signal. In such a context, the slower time constant is valid in the normal mode.

13/24 © EPODOC / EPO

- PN - [US6194941](#) B1 20010227
- PR - US19990290929 19990413
- AP - US19990290929 19990413
- DT - **
- CT - [US4912714](#) A []; [US5053877](#) A [];
[US5463410](#) A []; [US5644127](#) A [];
[US6038432](#) A []
- CCI - [H03F3/45605](#) ; [H03F3/45475](#)
- PA - DELPHI TECH INC [US]
- TI - DC **offset compensation circuit** for a signal amplifier
- AB - A DC **offset compensation circuit** (34) for compensating for a DC **offset** voltage of a signal amplifier (24) includes a first sample and hold **circuit** (40) having an input receiving an amplifier output signal (VOUT2) and an output supplying the sampled and held output signal (VOUT2) to a non-inverting input of a comparator 42. A first **digital-to-analog (D/A) circuit** (46) is responsive to a number of **digital** input signals to produce an analog DC target signal at an output (VD) thereof. The analog DC target signal is provided to an input of a second sample and hold **circuit** (50) having an output supplying the sampled and held



analog DC target signal to an inverting input of the comparator 42. The output of the comparator 42 is provided to an **offset** cancellation control **circuit** (56) including a **state** machine (66) and a counter **circuit** (68) operable to modify a count value (OFFDAC) thereof depending upon statuses of a number of input control signals (CLK1, CLK2, STRT, STP) and the comparator output signal (CO). A second D/A **circuit** has a number of **digital** inputs receiving the count value (OFFDAC) and producing at an output (VDCO) thereof an analog DC **compensation** signal corresponding thereto. The analog DC **compensation** signal is provided to a input (VDCO) of the signal amplifier (24) to thereby force the DC component of the amplifier output signal (VOUT2) near the analog DC target signal, thereby minimizing an aggregate DC **offset** voltage attributable to the signal amplifier (24).

14/24 © EPODOC / EPO
 PN - [US2006232335](#) A1 20061019
 PNFP - US7259616 B2 20070821
 PR - TW20050112330 20050419
 AP - US20050128250 20050513
 DT - *; Rep
 CT - || STSE (B2)
 [US6882218](#) B2 20050419 [
] (GUPTA SANDEEP K [US])
 - || R141 (A1)
 [US6882218](#) B2 []
 CCI - [H03F3/45192](#) ; [H03F3/45748](#)
 PA - (A1 B2)
 PRINCETON TECHNOLOGY CORP
 [TW]
 TI - (A1)



Method for single-end **offset compensation** of an operational amplifier

- (B2)

Method for single-ended **offset compensation** of an operational amplifier

AB

- (A1)

The present invention provides a method for single-end **compensation** of an operational amplifier, which comprises: designing an operational amplifier having a single-end **offset** style, preparing a common-mode **circuit**, a switch **circuit**, a comparator, a **digital circuit** and a **compensation** circuits. When a single-end **offset** voltage of the operational amplifier is converted, output of the comparator will change **state** and will be detected by the **digital circuit**, so that the **digital circuit** will fix a group of **digital** signals, and instruct the switch **circuit** to block an average signal of the common mode **circuit**, allowing a set of double-end input signals to be inputted to the operational amplifier directly.

- (B2)

The present invention provides a method for single-ended **compensation** of an operational amplifier, which comprises: designing an operational amplifier having a single-ended **offset** style, preparing a common-mode **circuit**, a switch **circuit**, a comparator, a **digital circuit** and a **compensation** circuits. When a single-ended **offset** voltage of the operational amplifier is converted, output of the comparator will change **state** and will be detected by the **digital**

circuit, so that the **digital circuit** will fix a group of **digital** signals, and instruct the switch **circuit** to block an average signal of the common-mode **circuit**, allowing a set of double-end input signals to be inputted to the operational amplifier directly.

15/24 © EPODOC / EPO

PN - [TW200638670](#) A 20061101

PNFP - TWI273767B B 20070211

PR - TW20050112330 20050419

AP - TW20050112330 20050419

DT - I

CCI - [H03F3/45192](#) ; [H03F3/45748](#)

PA - (A B)
PRINCETON TECHNOLOGY CORP
[TW]

TI - (A B)
Method for single-end **offset compensation** of operational amplifier

AB - (A)
The present invention provides a method for single-end **offset compensation** of an operational amplifier, where the operational amplifier is first designed to be apparently single-end **offset** before a common-mode **circuit**, a switch **circuit**, a comparator, a **digital circuit**, and a **compensation** circuits are applied. After being generated by the common-mode **circuit**, a set of average signals are transmitted via the switch **circuit** to the operational amplifier so that the output of the operational amplifier can generate a single-end **offset** voltage. The voltage is then inputted to the comparator to generate an initial output so as to trigger the **digital circuit**. According to time, the **digital**



circuit generates a set of **digital** signals and drives the **compensation circuit** to generate a corresponding **compensation** current, which is then provided to the operational amplifier. By means of the **compensation** of the **compensation** current, the single-end **offset** voltage of the operational amplifier is gradually approaching zero. Once the single-end **offset** voltage of the operational amplifier is reset to zero, the output **state** of the comparator changes. When the **digital circuit** detects such change, the **digital circuit** fixes the set of **digital** signals and instructs the switch **circuit** to block the average signals of the common-mode **circuit** while allowing a set of double-end input signals to be inputted to the operational amplifier directly.

- (B)

The present invention provides a method for single-end **offset compensation** of an operational amplifier, where the operational amplifier is first designed to be apparently single-end **offset** before a common-mode **circuit**, a switch **circuit**, a comparator, a **digital circuit** and a **compensation** circuits are applied. After being generated by the common-mode **circuit**, a set of average signals are transmitted via the switch **circuit** to the operational amplifier so that the output of the operational amplifier can generate a single-end **offset** voltage. The voltage is then inputted to the comparator to generate an initial output so as to trigger the **digital circuit**.

According to time, the **digital circuit** generates a set of **digital** signals and drives the **compensation circuit** to generate a corresponding **compensation** current, which is then provided to the operational amplifier. By means of the **compensation** of the **compensation** current, the single-end **offset** voltage of the operational amplifier is gradually approaching zero. Once the single-end **offset** voltage of the operational amplifier is reset to zero, the output **state** of the comparator changes. When the **digital circuit** detects such change, the **digital circuit** fixes the set of **digital** signals and instructs the switch **circuit** to block the average signals of the common-mode **circuit** while allowing a set of double-end input signals to be inputted to the operational amplifier directly.

16/24	© EPODOC / EPO
PN	- JP2007074329 A 20070322
PNFP	- JP4310298B B2 20090805
PR	- JP20050258703 20050907
AP	- JP20050258703 20050907
DT	- I
FI	- H03F3/34&A; H03F3/45&A; H03F3/45&Z
FT	- 5J500/AA01; 5J500/AA11; 5J500/AA47; 5J500/AA51; 5J500/AC13; 5J500/AF18; 5J500/AH10; 5J500/AH25; 5J500/AH39; 5J500/AK01; 5J500/AK17; 5J500/AK35; 5J500/AM21; 5J500/AT01; 5J500/AT06; 5J500/DN12
PA	- (A) PRINCETON TECHNOLOGY CORP
TI	- (A)



METHOD FOR SINGLE-END **OFFSET**
COMPENSATION OF
OPERATIONAL AMPLIFIER

AB

- (A)
PROBLEM TO BE SOLVED: To provide a method for single-end **offset compensation** of an operational amplifier.
- SOLUTION: The method for single-end **compensation** of an operational amplifier comprises an operational amplifier 1 designed in a single-end **offset** style, a common-mode **circuit 2**, a switch **circuit 3**, a comparator 4, a **digital circuit 5**, and a **compensation circuit 6**. A set of double-end input signals of the operational amplifier 1 are input to the common mode **circuit 2** and the switch **circuit 3**, and an average signal is generated by the common mode **circuit 2** and is input to the operational amplifier 1 by the switching **circuit 3**, and an output of the operational amplifier 1 generates a single-end **offset** voltage difference D. The voltage difference is input to the comparator, and an initial output is generated to trigger the **digital circuit 5**. The **digital circuit 5** generates a set of **digital** signals, on the basis of time to cause the **compensation circuit 6** to generate a corresponding **compensation** current. The **compensation** current of the **compensation circuit 6** is provided to the operational amplifier 1, to compensate the voltage difference D of the operational amplifier 1, so that the voltage difference D approaches zero. When the voltage difference D of the operational amplifier 1 is zero, the output of the

comparator 4 changes the **state** and is detected by the **digital circuit 5**; and the **digital circuit 5** fixes the set of **digital** signals and instructs the switch **circuit 3** to block the average signal of the common mode **circuit 2** and makes the set of double-end input signals to be input directly to the operational amplifier 1.

- COPYRIGHT: (C)2007,JPO&INPIT

17/24 © EPODOC / EPO

PN - [JPS63154927](#) A 19880628

PNFP - JPH0663882B B2 19940822

PR - JP19860301187 19861219

AP - JP19860301187 19861219

DT - I

CT - (A)
[JPS60154130](#) A []; [JPS60221288](#)
A []

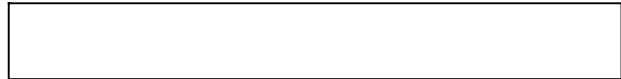
FI - B25J19/02; G01L1/00&K;
G01L5/00&101Z

FT - 2F051/AA10; 2F051/AB10;
2F051/AC01; 2F051/AC04;
3C007/KS30; 3C007/KS34;
3C007/KV06; 3C007/KW03;
3C007/KX07; 3C007/MT00;
3C707/KS30; 3C707/KS34;
3C707/KV06; 3C707/KW03;
3C707/KX07; 3C707/MT00;
3F059/DA05; 3F059/DC04;
3F059/DD06; 3F059/DE03;
3F059/DE08

PA - (A)
AGENCY IND SCIENCE TECHN

TI - (A)
OUTPUT SIGNAL PRE-PROCESSING
APPARATUS OF PRESSURE
SENSATION SENSOR

AB - (A)
PURPOSE:To measure pressure
distribution not only on a two-
dimensional surface but also on
a three-dimensional surface, by
a method wherein pressure



detection modules are arranged in a matrix **state** and the detection output in the selected module is swept, and **offset** temp. **compensation** and span temp. **compensation** are individually performed using the output of a temp. detection part and a microcomputer.

CONSTITUTION: After the transmission and reception of data in an address generation part 52 and an address regeneration part 51 are finished, decoders 23-25 are selected from the line groups 42-44 corresponding to address values to turn an analogue change-over device 19, switches S_x , S_y and a switch 22 ON and the pressure and temp. signals of a belonging pressure module 18 are outputted. By this mechanism, the detection output of the specific pressure detector of the address indicated by CPU 33 is amplified by an amplifying part 16 and converted to **digital** output by an A/D converter 26, and pressure and temp. are temporarily stored in a temporary storing RAM 27 and a compensated operation speed is made rapid by a multiplying processor 28 and a dividing processor 29 to be outputted through a signal output port 32 while corrected data is stored in corrected data storing RAM 31. Sweeping is successively performed to complete a pressure distribution data file in RAM 31. By this constitution, the number of **circuit** constitutional parts are reduced and miniaturization is achieved and pressure distribution can be economically measured.

18/24 © EPODOC / EPO

PN - [JPH0330156](#) A 19910208

PNFP - JP2714149B B2 19980216

PR - JP19890164048 19890628

AP - JP19890164048 19890628

DT - I

CT - (A)
[JPH02118979](#) A []

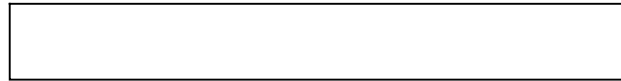
FI - G11B21/10&L; G11B21/10&V

FT - 5D096/AA03; 5D096/CC01;
5D096/EE01; 5D096/FF05;
5D096/FF10; 5D096/GG04;
5D096/GG10; 5D096/HH01;
5D096/KK03; 5D096/KK07;
5D096/KK12

PA - (A)
HITACHI LTD

TI - (A)
DISK DEVICE

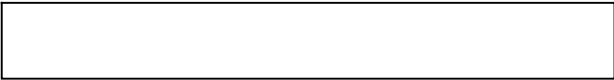
AB - (A)
PURPOSE:To perform external
force correction with high
accuracy and to contrive
improvement of head positioning
accuracy and curtailment of
access time by providing an
external force estimating means,
a storage means for storing
external force estimating value
and a correction means for
correcting a position control
signal by the stored external
force estimating value.
CONSTITUTION:Since a position
signal is deviated from zero by
an **offset** amt. of a head as well
when the head is pulled by
external force, the position
signal is fetched as a sample
position signal through an A/D
converter 9 by a **digital**
compensator to be executed in a
controller 15, and **compensation**
is carried out to make this signal
zero. That is, a phase
compensating calculation of
phase-lead-lag **compensation**,



etc., or a **state** feedback compensating calculation including a **state** estimator is performed on the sample position signal by the **digital** compensator, and a sample control signal obtained by adding up this calculation result and the external force correction value is inputted via a D/A converter 7 to a driving **circuit** 6, so as to make the magnetic head 3 follow the center of a track. By this method, since the external force can most suitably be compensated, the improvement of the positioning accuracy and the curtailment of the access time are contrived.

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PN - [JPH09294141](#) A 19971111
 PNFP - JP3131643B B2 20010205
 PR - JP19960107156 19960426
 AP - JP19960107156 19960426
 DT - I
 FI - H03K5/08&R; H04B10/00;
 H04B10/079; H04B10/2507;
 H04B9/00&B; H04B9/00&179;
 H04B9/00&251; H04L25/03&E;
 H04L25/06
 FT - 5J039/BC04; 5J039/BC06;
 5J039/DA12; 5J039/DB03;
 5J039/DB06; 5J039/DC02;
 5J039/MM02; 5J039/MM06;
 5J039/MM07; 5J039/NN01;
 5K002/AA03; 5K002/CA11;
 5K002/CA13; 5K002/DA05;
 5K029/AA03; 5K029/CC04;
 5K029/EE18; 5K029/HH08;
 5K029/HH11; 5K029/HH16;
 5K029/HH30; 5K029/JJ01;
 5K029/LL14; 5K102/AA01;
 5K102/AA41; 5K102/AA68;
 5K102/AH22; 5K102/KA12;
 5K102/KA40; 5K102/LA17;
 5K102/LA26; 5K102/LA38;



5K102/LA52; 5K102/MA02;
5K102/MB14; 5K102/MB15;
5K102/MC29; 5K102/MC30;
5K102/MH03; 5K102/MH14;
5K102/MH22; 5K102/MH26;
5K102/RD01; 5K102/RD02

- PA - (A)
JAPAN AVIATION ELECTRON
- TI - (A)
DIGITAL OPTICAL SIGNAL
RECEPTION **CIRCUIT**
- AB - (A)
PROBLEM TO BE SOLVED: To
surely recover the level change
of H/L even when a gradual loss
of light quantity is caused in a
received optical signal.
SOLUTION: A reception **circuit** of
an automatic threshold control
(ATC) system and a **circuit** of a
quasi fixed ATC system subjected
to temperature **compensation** are
used altogether and both outputs
are ANDed to obtain a receiver
output. An ATC **circuit** 5 generates
automatically a threshold level
Vr1 whose level is nearly a
middle level of a level of an
amplifier output V1. However,
when the amplifier output V1
changes slowly from L to H due
to a loss of luminous quantity, a
relation of $Vr1 > V1$ is established
at all times, then a 1st
comparator 4a does not detect
this change, an output V2a is
kept to an H level and a gate of
an AND **circuit** 9 is kept through.
However, this **state** change is
detected by a 2nd comparator 4b
of the ATC system and a receiver
output V3 is obtained. Since
an **offset** voltage $\Delta V1$ is
generated by an ambient
temperature change at an
amplifier 3, an **offset** voltage
 $\Delta V1'$ of a
temperature **compensation**

amplifier 7 to cancel it is added
to a fixed threshold voltage $V_{r2'}$
and the sum is given to the 2nd
comparator 4b.

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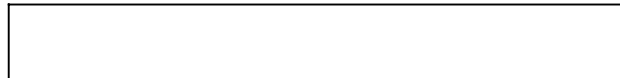
PN - [JPS5730414](#) A 19820218
PR - JP19800104591 19800730
AP - JP19800104591 19800730
DT - I
CCI - [H03K5/26](#)
FI - H03K5/26&Z; H03L7/08&D;
H03L7/089; H03L7/089&150
FT - 5J039/JJ07; 5J039/JJ10;
5J039/JJ18; 5J039/KK01;
5J039/KK10; 5J039/KK20;
5J039/KK28; 5J039/KK33;
5J039/MM16; 5J060/AA04;
5J060/BB01; 5J060/BB02;
5J060/BB03; 5J060/CC01;
5J060/CC24; 5J060/CC38;
5J060/CC41; 5J060/CC44;
5J060/DD06; 5J060/DD08;
5J060/DD13; 5J060/DD32;
5J060/DD33; 5J060/DD36;
5J060/DD46; 5J060/EE01;
5J060/EE19; 5J060/GG06;
5J060/GG15; 5J060/HH10;
5J060/JJ08; 5J060/KK05;
5J060/LL00; 5J060/LL04;
5J106/AA04; 5J106/BB01;
5J106/BB02; 5J106/BB03;
5J106/CC01; 5J106/CC24;
5J106/CC38; 5J106/CC41;
5J106/CC44; 5J106/DD06;
5J106/DD08; 5J106/DD13;
5J106/DD32; 5J106/DD33;
5J106/DD36; 5J106/DD46;
5J106/EE01; 5J106/EE19;
5J106/GG06; 5J106/GG15;
5J106/HH10; 5J106/JJ08;
5J106/KK05; 5J106/LL00;
5J106/LL04
PA - FUJITSU LTD
TI - **OFFSET** AUTOMATIC
COMPENSATING SYSTEM
AB - PURPOSE:To prevent the



production of **offset** current, by automatically balancing the current of the current source with a **compensation circuit**.
 CONSTITUTION: In the test mode, switching circuits SW2, SW4 are at off-**state** and SW1, SW3 are at no-stage, the current I1 of a current source 3 flows to a resistor 10 and the SW3 via the SW1, and the latter is the current I2 of a current source 4. In this case, if the currents I1, I2 are unbalanced, the current IR of the difference flows to the resistor 10 to generate a voltage VR. This voltage VR is detected at a voltage comparator 11 and after the output voltage Vt is converted into a **digital** signal ADt at an AD converter 12, it is outputted to a memory 13. The memory 13 produces an analog signal Mt corresponding to the ADt adjustment is made so that the current I2 of the current source 4 is equal to the I1. When the I1 is equal to the I2, the IR is zero and the VR=0 volt. A 0V detector 14 detects this **state** to produce a control signal Vs and to keep the memory 13 to the **state**.

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PN - [JPS63242027](#) A 19881007
 PR - JP19870074858 19870328
 AP - JP19870074858 19870328
 DT - I
 CT - [JPS5667442](#) A []; [JPS57203323](#) A []
 FI - H03M1/10&A
 FT - 5J022/AA01; 5J022/AB01;
 5J022/AC04; 5J022/BA03;
 5J022/BA05; 5J022/BA06;
 5J022/CA07; 5J022/CB01;
 5J022/CB06; 5J022/CD02;



5J022/CE08; 5J022/CF06;
5J022/CF07; 5J022/CF08

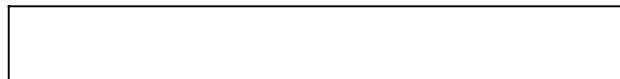
PA - TOSHIBA CORP; TOSHIBA MICRO
CUMPUTER ENG

TI - ANALOG PROCESSING **CIRCUIT**

AB - PURPOSE:To eliminate the need
for an external controller by
generating an output of an
analog filter means as an **offset**
voltage in selecting an analog
reference voltage and detecting a
voltage difference between an
output of the analog filter means
and the **offset** voltage so as to
apply **offset compensation** in
the **state** of an analog voltage.
CONSTITUTION:A switch **circuit**
11 selects an analog input
voltage Vin. An output voltage of
an analog filter **circuit** 12 in such
a case is fed to a voltage
subtraction **circuit** 18 in
an **offset compensation circuit**
13. A data corresponding to
an **offset** voltage stored in
an **offset** data latch **circuit** 16 is
read in advance from the **offset**
compensation circuit 13 and the
data is converted into an analog
voltage by a DA
conversion **circuit** 17 and fed to
the voltage subtraction **circuit**
18. Then the **offset** voltage is
subtracted from the output
voltage of the analog filter **circuit**
12 corresponding to the analog
input voltage and fed to the DA
converter **circuit** 14. Then the
voltage is AD-converted by the
DA converter **circuit** 14, where
a **digital** data Dout with an **offset**
component eliminated thereof is
obtained.

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PN - [JPH02184116](#) A 19900718
PR - JP19890004531 19890111
AP - JP19890004531 19890111



DT - I

CT - [JPS57203323](#) A []; [JPS5954321](#) A
[]

FI - H03M1/10&A

FT - 5J022/AA01; 5J022/BA03;
5J022/CA09; 5J022/CB06;
5J022/CF07

PA - MATSUSHITA ELECTRIC IND CO LTD

TI - ANALOG **DIGITAL**
CONVERSION **CIRCUIT**

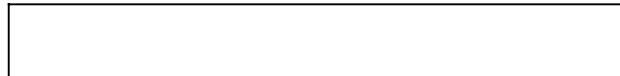
AB - PURPOSE:To eliminate a
DC **offset** component by latching
the DC **offset** component with
an **offset compensation** signal
output means when an
input **state** of a signal of an A/D
conversion **circuit** main body is
no signal **state** by a switch
means. CONSTITUTION:A switch
means 1 switches the input **state**
of an analog **digital**
conversion **circuit** 2 into the
analog signal input **state** and the
no signal **state**. Then an **offset**
compensation signal output
means 9 adds an inversion
signal of a **digital** output signal
of the analog **digital**
conversion **circuit** 2 in the no
signal **state** to an adder 6 as
an **offset compensation** signal,
and the adder 6 adds a **digital**
output signal of the
analog **digital** conversion **circuit**
at the input of the analog signal
and an **offset compensation**
signal of an **offset compensation**
signal output means. Then the
DC **offset** component included in
the **digital** output signal of the
analog **digital** conversion **circuit**
2 is cancelled by the adder 6.

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PN - [EP0495280](#) A1 19920722

PR - EP19910300417 19910118

AP - EP19910300417 19910118



DT	- *; Rep
CT	- STSE (A1) US4618848 A 19861021 [A] (PARFITT STEVEN P [US]); EP0103468 A2 19840321 [A] (DEERE & CO [US]); EP0201415 A1 19861112 [A] (INOVELF SA [FR]); DE3202497 A1 19830804 [A] (BIZERBA WERKE KRAUT KG WILH [DE])
CCI	- G01G23/3714 ; G01L1/2256 ; G06F3/0383 ; H03M1/0607
CCA	- H03M1/12
PA	- IBM [US]
TI	- Analog to digital convertor with drift compensation.
AB	- An analog to digital convertor (20) comprises an amplifier (100) for amplifying an analog input signal to generate an amplified output signal. Conversion means (110) periodically samples the amplified output signal to generate a digital word as a function of each sample. Compensation means preferably including a microcontroller logic circuit (130) compensates for a drift in the output signal steady state level of the amplified output signal. The compensation means includes tracking means (130) for summing a digital offset value and the digital word in response to and to compensate for the drift in the output signal level between upper and lower limits. The compensation means also includes bias means (130,140) for changing a bias signal level at the input of the amplifier (100) in response to and to compensate for the drift extending beyond the limits. The compensation means further

includes logic means (130,190)
for modifying the **digital** word in
response to and to compensate
for the step change.

24/24 © EPODOC / EPO

PN - [EP1045515](#) A2 20001018
PNFP - EP1045515 A3 20050720
PR - US19990290929 19990413
AP - EP20000200948 20000315
DT - *; Rep
CT - || STSE (A3)
[US5061900](#) A 19911029
[X] (VINN CHARLES L [US], et al)
[X] 1-3,8-11,13-15,19
* column 4, line 4 - line 52;
figures 1,4b *;
[US4490682](#) A 19841225
[X] (POULO LOUIS [US])
[X] 1,2,10-14,19
* column 2, line 2 - line 5;
figure 2 *
* column 3, line 44 - column 4,
line 60 *;
[US4356450](#) A 19821026
[X] (MASUDA EIJI)
[X] 1,8-11,13,14,19
* column 2, line 24 - column 3,
line 15; figures 1,4 *
* column 6, line 58 - column 7,
line 17 *;
[US4395681](#) A 19830726
[X] (HORNUNG ROBERT [FR], et al)
[X] 1-3,11,13,19
* figure 4 *;
[US4229703](#) A 19801021
[X] (BUSTIN RAPHAEL)
[X] 1,8-11,13,14,19
* figures 1,2 *;
[EP0794436](#) A1 19970910
[X] (DELCO ELECTRONICS CORP
[US])
[X] 1-3,11,13,14,19
* figure 4 *;
[US4063447](#) A 19771220
[X] (MATHISON LESLIE C)
[X] 1-3,11,13,19
* column 4, line 22 - column 5,



line 55; figure 2 *;
[EP0862058](#) A1 19980902
 [X] (TELEFUNKEN
 MICROELECTRON [DE])
 [X] 1-3,11,13,19
 * column 3, line 5 - column 4,
 line 22; figure 1 *;
[EP0379817](#) A1 19900801
 [A] (RADIOTECHNIQUE
 COMPELEC [FR], et al)
 [A] 1,13
 * figure 1 *

- CCI - [H03F3/45475](#) ; [H03F3/45605](#)
- PA - (A2 A3)
 DELPHI TECH INC [US]
- TI - (A2 A3)
 DC **offset compensation circuit**
 for a signal amplifier
- AB - (A2)
 A DC **offset compensation circuit**
 (34) for compensating for a
 DC **offset** voltage of a signal
 amplifier (24) includes a first
 sample and hold **circuit** (40)
 having an input receiving an
 amplifier output signal (VOUT2)
 and an output supplying the
 sampled and held output signal
 (VOUT2) to a non-inverting input
 of a comparator 42. A first **digital-**
 to-analog (D/A) **circuit** (46) is
 responsive to a number of **digital**
 input signals to produce an
 analog DC target signal at an
 output (VD) thereof The analog
 DC target signal is provided to
 an input of a second sample and
 hold **circuit** (50) having an output
 supplying the sampled and held
 analog DC target signal to an
 inverting input of the
 comparator 42. The output of the
 comparator 42 is provided to
 an **offset** cancellation
 control **circuit** (56) including
 a **state** machine (66) and a
 counter **circuit** (68) operable to
 modify a count value (OFFDAC)

thereof depending upon statuses of a number of input control signals (CLK1, CLK2, STRT, STP) and the comparator output signal (CO). A second D/A **circuit** has a number of **digital** inputs receiving the count value (OFFDAC) and producing at an output (VDCO) thereof an analog DC **compensation** signal corresponding thereto. The analog DC **compensation** signal is provided to a input (VDCO) of the signal amplifier (24) to thereby force the DC component of the amplifier output signal (VOUT2) near the analog DC target signal, thereby minimizing an aggregate DC **offset** voltage attributable to the signal amplifier (24).