

Nicolas Vargas

Search history

Search 1: FT=(distortion analyzer) (Results 158)
Search 2: TAC=(distortion analyzer) (Results 65)
Search 3: 2 and usb (Results 1)
Search 4: TA=(distortion analyzer) (Results 37)
Search 5: 4 and micro* (Results 6)
Search 6: 4 and filter (Results 16)

1) Family number: 4388061 (US4453827A)

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Title: OPTICAL **DISTORTION ANALYZER** SYSTEM

Abstract: An optical **distortion analyzer** system which is capable of automatically quantifying with a high degree of accuracy and repeatability the optical quality of transparencies such as windshields or windows. The analyzer system is made up of a platform adapted to support the transparency with two degrees of freedom. A probe beam of electromagnetic radiation emanating from, for example, a laser is passed through the transparency as the transparency is moved about a horizontal and vertical axis establishing a plurality of test points on the transparency. An analyzer unit receives the probe beam and therefrom establishes horizontal and vertical deviations in the transparency as well as determining the cylindrical and spherical lens power components and principal meridian angle of the transparency. A processor provides recognizable opthalmic parameters of the above characteristics of the transparency and correlates these parameters with the plurality of test points on the transparency.

Classifications:

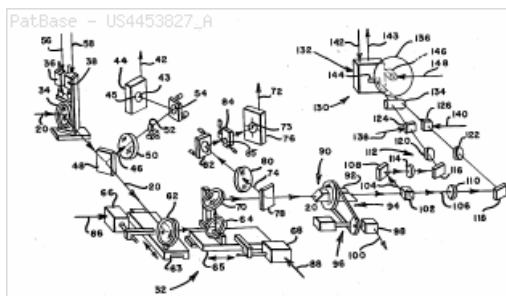
International (IPC 8-9): G01J9/02 G01M11/00 (Advanced/Invention);
G01J9/00 G01M11/00 (Core/Invention)

International (IPC 1-7): G01B9/02

CPC: G01N21/958 G01N2021/9586 G01J9/02 G01M11/00

European: G01J9/02 G01M11/00

US: 356/125 356/127 356/239 356/353 356/520 364/552



Family:

Publication number	Publication date	Application number	Application date
US4453827 A	19840612	US19810297527	19810828

Priority:

US19810297527 19810828

Probable Assignee: US AIR FORCE

Assignee(s): (std): US AIR FORCE

Assignee(s): SECRETARY OF AIR FORCE AS US GOV ; SECRETARY OF AIR FORCE US ; THE UNITED STATES OF AMERICA AS REPRESENTED BY THE SECRETARY OF THE AIR FORCE

Inventor(s): (std): TABOADA JOHN

2) Family number: 32024081 (ES2233193B)

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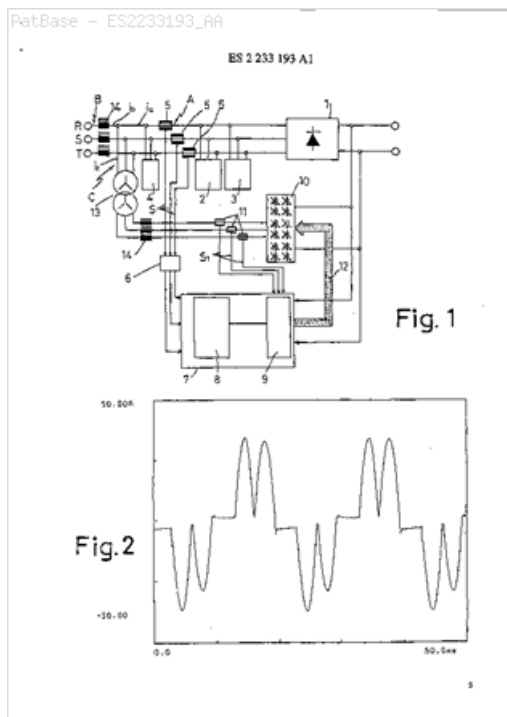
Title: FILTRO ACTIVO A UTILIZAR EN UNA RED CON UNA CARGA NO LINEAL

Abstract: Source: ES2233193B [ES] Filtro activo a utilizar en una red con una carga no lineal, que consta de unos primeros sensores de intensidad, cuya salida es proporcional a la intensidad de entrada a la carga no lineal; un puente inversor alimentando unos segundos sensores de intensidad; un procesador programado con una curva de intensidad prefijada, que consta de un bloque analizador que obtiene la distorsion real; y un bloque de logica que recibe la senal de salida de los segundos sensores de intensidad y que ordena las caracteristicas de disparo del puente inversor mientras la conjuncion de la senal de distorsion con la distorsion real no recompongan, con un diferencial prefijado, a la curva de intensidad prefijada. De aplicacion en la distribucion de electricidad.

Classifications:

International (IPC 8-9): H02J3/01 H02M7/48
H02M7/5387 (Advanced/Invention);
H02J3/01 H02M7/5387 (Core/Invention)

International (IPC 1-7): H02J3/01 H02M7/48



Family:

Publication number	Publication date	Application number	Application date
ES2233193 AA	20050601	ES20030002691	20031118
ES2233193 BA	20060316	ES20030002691	20031118

Priority:

ES20030002691 20031118

Probable Assignee:

ENERTRON S L

Assignee(s): (std):

ENERTRON S L

Assignee(s):

ENERTRON SL

Inventor(s): (std):

VISIERS GUIXOT MANUEL

3) Family number: 8596195 (US4340854A)

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Title: Distortion measurement system

Abstract: A type of Total-Harmonic-Distortion (THD) **distortion analyzer** is described in which the use of the State Variable (SV) circuit in both the oscillator and the **filter** sections confers several benefits and results in performance superior to previously available analyzers. In the SV oscillator, the traditional compromise in the automatic level control function between settling time, component tolerance and distortion is alleviated by the use of polyphase level detection, made possible by the SV circuit. The doubly-integrated output available from the SV circuit also minimizes distortion, especially that contributed by the level-setting AGC. The other property of the SV circuit, which is particularly valuable, is the connection of frequency-setting elements to virtual-ground points, which allows great simplification of wide-range tuning circuitry. Exploitation of this property is described both for manual and programmable cases. The SV circuit is also superior to many previously employed circuits in its tolerance of component inaccuracies. The simultaneous presence of high-pass, band-pass and low-pass outputs from the SV **filter** is shown to be advantageous also for its use as the **filter** on a **distortion analyzer**.

Classifications:

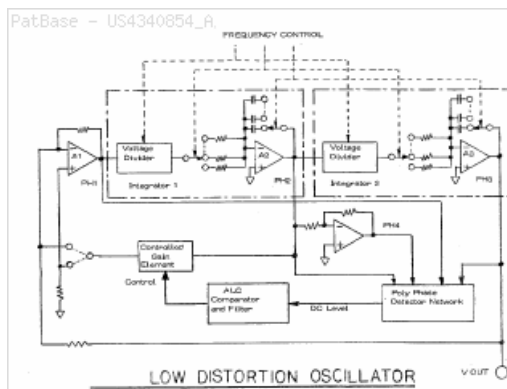
International (IPC 8-9): G01R23/20 (Advanced/Invention); G01R23/20 (Core/Invention)

International (IPC 1-7): G01R27/00

CPC: G01R23/20

European: G01R23/20

US: 324/57DE 324/623 324/76.12 324/76.71 327/100 331/135 455/67.13



Family:

Publication number	Publication date	Application number	Application date
US4340854 A	19820720	US19800139673	19800414

Priority:

US19800139673 19800414

Probable Assignee:

JONES WAYNE W

Assignee(s): (std): JONES WAYNE W ; STONE ROGER
Inventor(s): (std): JONES WAYNE W ; STONE ROGER

4) Family number: 11484233 (US5293449A)

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Title: ANALYSIS-BY-SYNTHESIS 2,4 KBPS LINEAR PREDICTIVE SPEECH CODEC

Abstract: A linear predictive speech codec arrangement including: a spectrum synthesizer for providing reconstructed speech generation in response to excitation signals; a **distortion analyzer** for comparing the reconstructed speech with an original speech, and providing a distortion analysis signal in response to such comparison; and an excitation model circuit for providing excitation signals to the spectrum synthesizer, with the excitation model circuit receiving and utilizing the distortion analysis signal in an analysis-by-synthesis operation, for determining ones of excitation signals which provide an optimal reconstructed speech. The excitation model circuit can include: a voiced excitation generator and a Gaussian noise generator, both of which should optimally provide a plurality of available excitation signal models. The voiced excitation generator and Gaussian noise generator can be in the form of a codebook of a plurality of possible pulse trains and Gaussian sequences, respectively, or alternatively, the voiced excitation generator can be in the form of a first order pitch synthesizer. The optimal excitation signal and/or the pitch value and the pitch **filter** coefficient are determined using an analysis-by-synthesis technique.

Classifications:

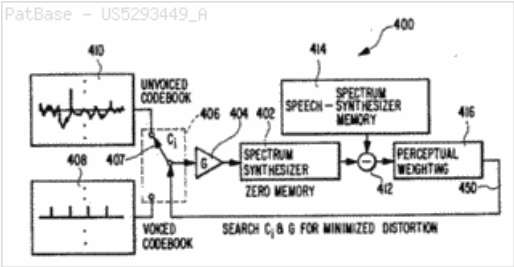
International (IPC 8-9): G10L19/10 G10L19/12 (Advanced/Invention);
G10L11/06 (Advanced/Non-invention);
G10L19/00 (Core/Invention);
G10L11/00 (Core/Non-invention)

International (IPC 1-7): G10L9/14

CPC: G10L19/12 G10L19/10 G10L25/24 G10L25/93

European: G10L19/10 G10L19/12 S10L25/24 S10L25/93
T05K999/99

US: 395/2.28 395/2.29 395/2.32 704/219 704/220 704/223
704/E19.032 704/E19.035



Family:

Publication number	Publication date	Application number	Application date
US5293449 A	19940308	US19920905239	19920629

Priority:

US19900617331 19901123 US19920905239 19920629

Probable Assignee: COMSAT CORP

Assignee(s): (std): COMSAT CORP

Inventor(s): (std): TZENG FORREST F

5) Family number: 11654256 (US5930414A)

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Title: Method and apparatus for automatic compensation of first-order polarization mode dispersion (PMD)

Abstract: The effect of polarization mode dispersion that an optical signal experiences as it propagates through an optical transmission fiber is compensated for at a receiver using a birefringent compensator, in which the compensator automatically and adaptively generates a level of differential time delay that substantially equals the differential time delay that the optical signal experiences, but of different sign, and, therefore, essentially cancels out the undesired delay.

Classifications:

International (IPC 8-9): H04B10/02 H04B10/135 H04B10/18

H04B3/06 (Advanced/Invention);

G02B6/00 H04B10/135 (Advanced/Non-invention);

H04B10/02 H04B10/135 H04B10/18 H04B3/06 (Core/Invention);

H04B10/135 (Core/Non-invention)

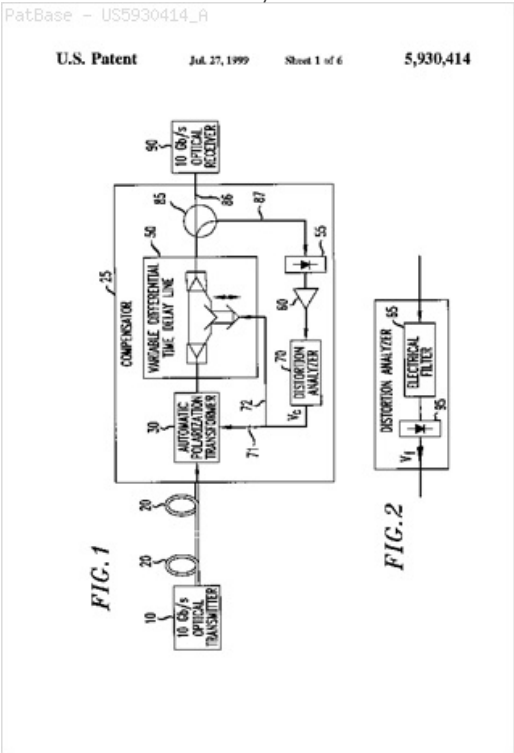
International (IPC 1-7): G02B6/00 G02F1/00 G02F1/01 H04B10/02

H04B10/135 H04B10/18 H04B3/06 H04J14/08

CPC: H04B10/2569

European: H04B10/2569

US: 385/11 385/123 385/24 385/27 385/28 398/1 398/147 398/152
398/161



Family:

Publication number	Publication date	Application number	Application date
CA2245303 AA	19990316	CA19982245303	19980819
CA2245303 C	20021210	CA19982245303	19980819
CN1211744 A	19990324	CN19981019194	19980915
DE69834787 D1	20060720	DE19986034787	19980908
DE69834787 D1	20060720	DE19986034787T	19980908
DE69834787 T2	20070516	DE19986034787T	19980908
EP0909045 A2	19990414	EP19980307225	19980908
EP0909045 A3	20040114	EP19980307225	19980908
EP0909045 B1	20060607	EP19980307225	19980908
JP11196046 A2	19990721	JP19980260738	19980916
JP3466486 B2	20031110	JP19980260738	19980916
KR19990029764 A	19990426	KR19980037743	19980914
NO322264 B1	20060904	NO19980004185	19980911
NO984185 A	19990317	NO19980004185	19980911
NO984185 A0	19980911	NO19980004185	19980911
US5930414 A	19990727	US19970931553	19970916

Priority:

US19970931553 19970916 CA19982245303 19980819 KR19980037743 19980914

Probable Assignee: WSOU INVESTMENTS LLC

Assignee(s): (std): LUCENT TECHNOLOGIES INC

Assignee(s): LUCENT TECHNOL INC ; WILSON DAVID L ; HEISMAN FRED LUDWIG ; OMEGA CREDIT OPPORTUNITIES MASTER FUND LP ; WSOU INVESTMENTS LLC ; ALCATEL LUCENT USA INC ; CHASE MANHATTAN BANK AS COLLATERAL AGENT ; CHASE MANHATTAN BANK COLLATERAL AGENT AS ; CREDIT SUISSE AG ; FISHMAN DANIEL A

Inventor(s): (std): FISHMAN DANIEL A ; FISHMAN DANIEL A ; HEISMAN FRED LUDWIG ; WILSON DAVID L

Inventor(s): FRED LUDWIG HEISMAN ; DANIEL A FISHMAN ; DAVID L WILSON

Agent(s): KIRBY EADES GALE BAKER; MOTOMIYA TERUHISA; FUJINO IKUO; TAKANASHI NORIMICHI; UBUKATA KAZUO; KATO NOBUAKI; TAKAHASHI SEIICHIRO; OCHI TAKAO; USUI SHINICHI; OKABE MASAO; YOSHIZAWA HIROSHI; ASAHU NOBUMITSU

Designated states: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

6) Family number: 22727320 (US3182254A)

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Title: INTERMODULATION **DISTORTION ANALYZER** FOR PLOTTING SECOND AND THIRD ORDER COMPONENTS

Abstract: (Claim 1) 1. In a system for measuring distortion of a device under test, a first mixer, a narrow band selective circuit connected in cascade with said first mixer, said selective circuit having a pass band centered on frequency IF, means for presenting a plot of signal output of said selective circuit as a function of frequency, said last means including a scanning local oscillator, and means for at will connecting said local oscillator to said mixer, said local oscillator scanning over a frequency range, means responsive to said local oscillator for generating two 40 synchronously scanning local signals f_a and $f_a \pm A_f$, where A_f is a fixed frequency, means for applying said scanning local signals jointly to said device under test, means for selecting the frequency A_f from the output of said device under test continuously in response to scanning of said 45 scanning local signals, means for applying said frequency A_f to said first mixer, and means applying a fixed frequency equal to $IF \pm A_f$ to said first mixer.

Classifications:

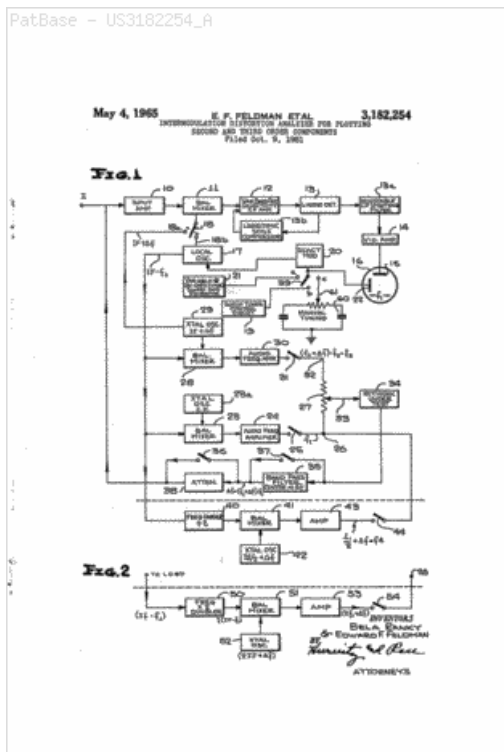
International (IPC 8-9): G01R27/32 (Advanced/Invention);

G01R27/00 (Core/Invention)

CPC: G01R27/32

European: G01R27/32

US: 324/624 324/76.26



Family:

Publication number	Publication date	Application number	Application date
US3182254 A	19650504	US19610143793	19611009

Priority:

US19610143793 19611009

Probable Assignee:

SINGER CO

Assignee(s): (std):

SINGER CO

Assignee(s):

THE SINGER COMPANY

Inventor(s): (std):

BELA RANKY ; FELDMAN EDWARD F

Inventor(s):

RANKY BELA

7) Family number: 30619445 (US2004105683A)

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Title: POLARIZATION MODE DISPERSION CONTROLLER DEVICE AND METHOD FOR ITS OPERATION

Abstract: A polarization mode dispersion (PMD) controller device for controlling the state of polarization of an optical light wave comprising a dispersion compensation unit (2; 25; 40) and an adaptation control unit (6; 28; 44), wherein the dispersion compensation unit (2; 25; 40) comprises a multitude of compensation stages processing the optical light wave, and wherein the adaptation control unit (6; 28; 44) controls the dispersion compensation unit (2; 25; 40) is characterized in that at least one feed-forward signal tap (4; 26a-26c, 73a-73c) is provided tapping the optical light wave inserted into one of the compensation stages, that the feed-forward signal(s) is(are) fed into a **distortion analyzer** unit (5; 27; 66) and that the **distortion analyzer** unit (5; 27; 66) provides the adaptation control unit (6; 28; 44) with information about the incoming optical light wave. It accelerates the adaptation speed and lowers the costs of a high-speed PMD controller device.

Classifications:**International (ipc 8-9):** H04B10/12 H04B10/18

H04B10/2569 (Advanced/Invention);

H04B10/12 H04B10/18 (Core/Invention)

International (ipc 1-7): H04B10/12 H04B10/18**CPC:** H04B10/2569**European:** H04B10/2569**US:** 398/147 398/147P 398/149 398/158

PatBase - US2004105683_RR

Patent Application Publication Jun. 3, 2004 Sheet 1 of 4 US 2004/0105683 A1

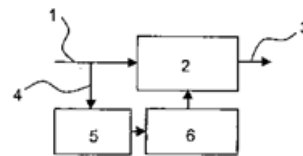


Fig. 1

Family:

Publication number	Publication date	Application number	Application date
AT289136 E	20050215	AT20020360332T	20021203
DE60202964 D1	20050317	DE20026002964	20021203
DE60202964 D1	20050317	DE20026002964T	20021203
DE60202964 T2	20050818	DE20026002964T	20021203
EP1427120 A1	20040609	EP20020360332	20021203
EP1427120 B1	20050209	EP20020360332	20021203
US2004105683 AA	20040603	US20030715557	20031119
US7289739 BB	20071030	US20030715557	20031119

Priority:

EP20020360332 20021203

Probable Assignee: WSOU INVESTMENTS LLC**Assignee(s):** (std): ALCATEL SA ; CIT ALCATEL**Assignee(s):** OMEGA CREDIT OPPORTUNITIES MASTER FUND LP ; WSOU INVESTMENTS LLC ; ALCATEL ; ALCATEL PARIS**Inventor(s):** (std): BUCHALI FRED ; BUELOW HENNING ; BULOW HENNING**Agent(s):** SUGHRUE MION PLLC**Designated states:** AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SI SK TR**8) Family number: 5119486 (US5140703A)**

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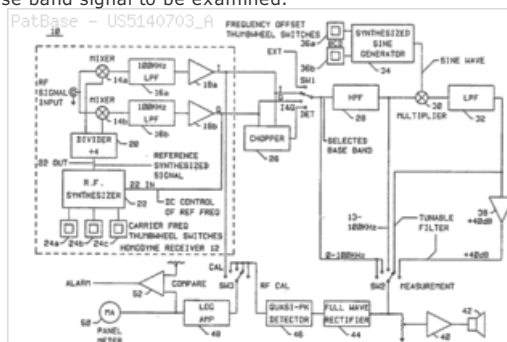
Title: MODULATION **DISTORTION ANALYZER**

Abstract: There is disclosed a method and apparatus for demodulating an R.F. modulated signal having a known carrier

frequency F_0 . A first reference signal of a frequency matching approximately the carrier frequency F_0 , is mixed with the input R.F. modulated signal to produce the demodulated signal. The first reference signal is generated by a reference oscillator which provides a second reference signal of a second distinct reference frequency, a voltage control oscillator for generating the first reference signal dependent upon the amplitude of an error signal applied thereto, a selectively variable divider circuit for receiving and dividing the first frequency by a selected number to provide a third divided signal, and a comparator for comparing the phase of the second reference signal with that of the third divided signal to generate and apply the error signal to the voltage control oscillator. The demodulated signal is applied to the reference oscillator, whereby the second frequency varies in accordance with the phase of the demodulated signal and the first frequency is phase-locked to the carrier frequency F_0 . A selected spectrum window of the demodulated signal is provided by generating a fourth reference signal of a frequency offset from the carrier frequency F_0 and by multiplying that offset reference signal by the demodulated signal to provide a difference signal indicative of the difference therebetween centered about the offset frequency. The difference signal is **filtered** to pass only those frequencies below a selected first frequency to provide a spectrum window whose bandwidth is limited to that segment of the demodulated or base band signal to be examined.

Classifications:

International (IPC 8-9): H03D1/22 H03J3/14 H04B1/30 H04B17/00 (Advanced/Invention);
H03D1/00 H03J3/00 H04B1/30 H04B17/00 (Core/Invention)
International (IPC 1-7): H04B1/10 H04B17/00
CPC: H04B1/30 H03D1/2254 H03J3/14 H04B17/15
European: H03D1/22E1 H03J3/14 H04B1/30 H04B17/00A2
US: 324/77B 455/226.1 455/295 455/324



Family:

Publication number	Publication date	Application number	Application date
US5140703 A	19920818	US19880257614	19881014

Priority:

US19880257614 19881014

Probable Assignee: PAYNE CHRISTOPHER P

Assignee(s): (std): PAYNE CHRISTOPHER P

Inventor(s): (std): PAYNE CHRISTOPHER P

9) Family number: 1191583 (US3916296A)

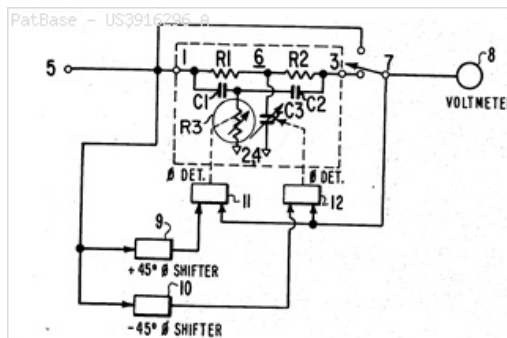
© PatBase

Title: **Distortion analyzer** with automatic tuning circuit

Abstract: An apparatus utilizing a parallel-T circuit bridge achieves improved low distortion measurements. To tune the bridge, two of the bridge components that do not interact with each other in the vicinity of the frequency to which the circuit is being tuned, are made variable. By adjusting these components, the bridge is easily adjustable without a large number of adjustments and readjustments. Since there is little interaction between these components, this circuit configuration is easily adaptable to automatic tuning.

Classifications:

International (IPC 8-9): G01R23/20 H03H7/06 H03H7/065 H03J3/02 (Advanced/Invention);
G01R23/20 H03H7/01 H03J3/00 (Core/Invention)
International (IPC 1-7): G01R17/00 G01R23/20 G05F1/00 H03H7/10
CPC: G01R23/20 H03J3/02
European: G01R23/20 H03J3/02
US: 323/219 323/64



Family:

Publication number	Publication date	Application number	Application date
JP50094956 A2	19750729	JP19740001451	19731221
JP53006065 B4	19780304	JP19740001451	19731221
US3916296 A	19751028	US19740532805	19741216

Priority:

JP19740001451 19731221

Probable Assignee: HEWLETT PACKARD CO A CORP OF CA

Assignee(s): (std): HEWLETT PACKARD YOKOGAWA

Assignee(s): YOKOGAWA HEWLETT PACKARD LTD ; HEWLETT PACKARD CO ; HEWLETT PACKARD CO A CORP OF CA

Inventor(s): (std): KITO SHIRO ; NARIMATSU YOH

10) Family number: 2021816 (GB2073895A)

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Title: AUTOMATIC INTERMODULATION **DISTORTION ANALYZER**

Abstract: A **distortion analyzer** is disclosed which automatically measures intermodulation distortion according to the SMPTE-IM method. Variations caused by gain or attenuation as function of frequency in the device under test are automatically compensated. This automation is accomplished by sensing the carrier level of the SMPTE-IM test signal and using this information in an automatic level control loop formed with a voltage controlled amplifier earlier in the signal processing path.

Classifications:

International (IPC 8-9): G01R23/20 G01R27/28

H04L1/00 (Advanced/Invention);

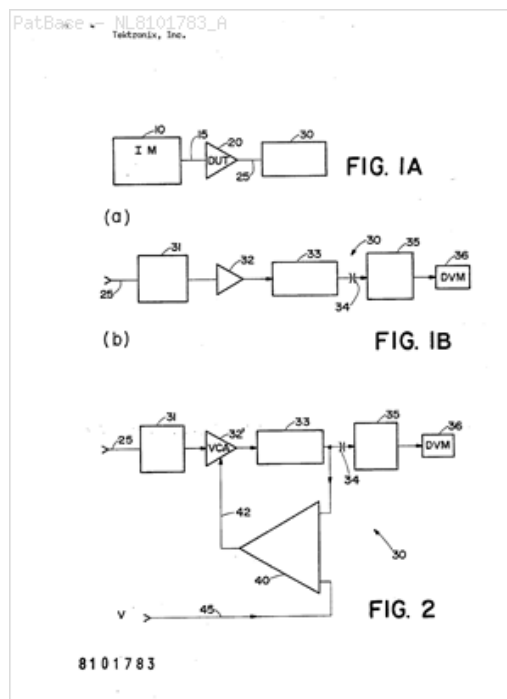
G01R23/20 G01R27/00 (Core/Invention)

International (IPC 1-7): G01R17/00 G01R23/00 G01R23/20

G01R27/28 G01R29/00 H04L1/00

CPC: G01R23/20

European: G01R23/20



Family:

Publication number	Publication date	Application number	Application date
CA1164066 A1	19840320	CA19810375085	19810409
DE3114244 A1	19820429	DE19813114244	19810408
DE3114244 C2	19851114	DE19813114244	19810408
FR2480438 A1	19811016	FR19810007641	19810410
FR2480438 B1	19840210	FR19810007641	19810410
GB2073895 A1	19811021	GB19810006636	19810303
GB2073895 B2	19831102	GB19810006636	19810303
JP1363704 C3	19870209	JP19810054926	19810410
JP56157869 A2	19811205	JP19810054926	19810410
JP61031426 B4	19860719	JP19810054926	19810410
NL8101783 A	19811102	NL19810001783	19810410

Priority:

US19800139940 19800411 CA19810375085 19810409

Probable Assignee: TEKTRONIX INC

Assignee(s): (std): TEKTRONIX INC

Assignee(s): TEKTRONIX INC BEAVERTON OREG US ; TEKTRONIX INC TE BEAVERTON OREGON VER ST V AM ; CABOT RICHARD C

Inventor(s): (std): CABOT RICHARD C ; CABOT RICHARD CORONA ; RICHAAO KORONA KABOTSUTO ; RICHIIYAADO KORONA KABOTSUTO

Inventor(s): RICHARD C CABOT ; CABOT RICHARD CORONA BEAVERTON OREG ; CABOT RICHARD CORONA BEAVERTON OREG US ; CORONA CABOT RICHARD

Agent(s): KIRBY EADES GALE BAKER

11) Family number: 9480865 (SU1449989A)

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Title: DEVICE FOR RECEIVING AND TRANSMITTING INFORMATION

Abstract: Source: SU1449989A **Machine translation:** 1. Since the first input of the AND gate 53 is set high level signal from porogovog block 3 (ogaibka exceeded the threshold of informativeness), the account is enabled. Next vtoln division is the current error recovery by recorded in the counter 54, divider 55, and remembering the value obtained in block 56 in the momentum synchronizer 18. Thus, a first input of comparator 57 is set threshold of informativeness, which in the next processing cycle next input vector is compared with a threshold of acceptable **distortion analyzer** determines emym 4 activity (initial threshold value for the first input vector is equal to 0). As indicated at the beginning of the next cycle of conversion of the vector in parallel with the frame latching input sample vector in frame memory unit 7, the signal at the second data inputs activity analyzer 4 also receives the input signal samples. At the end of the cycle frame reception unit 27 outputs differentiating (fig.2) is on the average value of the derivative vhdnog 10 449989. 8 according to the signal (1) and (2), the control unit 31 calculates the average value of the input signal to the adder 32. On the second cycle of operation of the transmitting side (recovery frame and comparing it with the original) unit 31 extracts the true background level value through said procedure (3) (average value of the subtraction signal is subtracted from ATel 33 samples the input signal and the resulting difference absolute values are summed by adder 34). Thus, the block 35 generates a known function depending on national 15 (4), the threshold to. admissible distortion. Thus, by the beginning of the operation of estimating the accuracy of information on the reduction of the analyzer outputs and 4 activity. 20 consequently, on the threshold corresponding to 5 inputs and 5 block formation Wathelet 1 value is set the desired level of allowable claim for zheny processed in 5 dannm time frame of the invention. If the error is less than the reduction "(0, installed analyzer 4, the comparison unit 57 and the switch 58 is formed threshold allowable distortion Eteh.ravny 0 E" n After conversion cycle synchronizer 18 sbrasshaet registers and adders 6,15,30,32,34 37, then samples the threshold blocks 3 and 5 and a transmission side is ready to process the next frame of the vector. On the receiving side using the input unit 21 decodes the information. ruets and is divided into the

coefficients, which are stored in the memory unit 23 coefficients, and counts error vector if they were transmitted. Further, the input unit 21 extracts the control signals from the received service information for 5 synchronizer 26 that configure the synchronizer 26 for receiving the corresponding mode, and executes it. After decryption of control and Ying-Q formational signalov.sinhronizator gates 26 of memory unit 22 signals basis analogous to the transmitting side unit 12, and multipliers 24, coordinate-wise multiplication occurs samples of signals on the basis of the values of the coefficients of the block 23, and the adder 25 - componentwise addition of digital signal values from all the multipliers samples from age-l 0 5 52 input unit 21, if they were transmitted. So there is a restoration of the transmitted signal. When allocating information neobhog conductivity recording unit memory 22 of the new basic service code signal from the input unit 21 parcels on-strivaet synchronizer 26 active receive mode, set mode; Recording unit 22 signals the memory base, and simultaneously with the reduction of input signal samples si drove the error output from the input section 21 receives a normalizer 20, which are normalized with respect to energy. Dp this synchronizer 26 sets the recording mode memory unit 36 and an adder 37 normalizer 20 generates lo-20 block 10 and the input unit 21. Tory strobe pulses equal Analyzer calculates Activity 4 - along the length of the number of samples in the vector is the threshold of allowable distortion for D, for which the memorizing-current input vector frame of input samples, errors in function block diagram of the analyzer 4 36 and compute the sum of squares of the quad-25 is shown in fig.Z. quadratic adder 37, Then synchronizer unit 26 converts 36 and adder 37 in read mode and in the same series of pulses on you by 20 strokes normalizer are normalized divisor of 39 input samples, which are recorded in the block memory 22 basis signals. Similarly works normalizer 11 transmitting side when recording new basic signal unit 12 memory. With receipt of the input signal samples are fed into the device by the second information input of the analyzer 4, wherein in the first series 30 biruyuschi strictly on Pulse adder 32 determined by the average value of counts and a differentiating unit 27, the current count is subtracted from the previous frame using the subtractor 28 delay element 29 and a one-step, the resulting difference is accumulated on a quadratic adder 30, which is calculated by mean-critical value of the first derivative Since section 22 is set to the recording mode, the bill allowed for the counter 60 (8) via the AND gate 59, and 40 for the input signal samples. In a series of corresponding selected MUX I reducing the input signal on pleksorom 61, entering read-write memory unit 62 also set the recording mode, with the remaining 62 blocks of memory are in read-only mode, so on a series of strobe pulses input samples from the normalizer 20 recorded in the k-th block of 62 memory, then sync signal is incremented contents of the bill, thus the next time for recording new basic signal is selected (A-I)-th block of 62 memory On a signal from the reset synchronizer unit 35 outputs 26 set input unit 21 is returned to the actual value of gg allowable distortion for the current input signal. On reset pulse at the end of the processing cycle registers are cleared adders 30,32 and 34 and the analyzer first 4 data inputs analyzer 4 again received samples of the input signal and a series of strobe pulses at 45 subtractor 33 vtoln - a subtraction from the original samples of their average value, and adder 34 - accumulation of absolute values obtained differences. At the end of the last strobe on the information outputs of block 31 is true on the magnitude of the background level, hence information on the initial state 50 and a write signal for the memory block 22 is released, the synchronizer 26 is returned to idle. forming a new entry shenii reference signal on the receiving side does not occur. After the reduction of the received signal or recording new basic signal synchronizer 26 48 resets the decoder input unit 21 and an adder 37 normalizer 20. This work cycle is complete and the receiving side is ready to receive the next input. Such an algorithm allows the work synchronously varied bases, both the transmitting and receiving sides on the device. Consider in more detail the analyzer 4 Activity output samples with the arrival of the input signal to the device, they are fed to the second input information analyzer 4, wherein in the first series 30 biruyuschi strictly on Pulse adder 32 determined by the average value of counts and a differentiating unit 27, the current count is subtracted of the previous frame by using a subtractor 28 and delay element 29 for one clock cycle, the resulting difference is stored on a quadratic adder 30, which calculates a mean-critical value of the first derivative 35 by 40 signal input samples. In the recovery cycle of the input signal at the output of 35 gg set actual value on allowable input signal samples. In the recovery cycle of the input signal at the output of the actual value of 35 set of admissible data inputs of the first analyzer 4 again received samples of the input signal and a series of strobe pulses on the subtractor 33 vtoln - a subtraction from the original sample i their average value, and an adder 34 - accumulation of absolute values obtained differences. By the end of the last strobe information on the outputs of block 31 is true for the value of the background level, hence on information again ready to receive input. Figure 5 is a functional block diagram of an output 10, which operates as follows: ra. The first case. E EOC, Threshold units 3 and 5 do not activate its outputs (0,0). Synchronizer 18 to zero level of control signal m-th channels tuned to transmit only to the coefficient generator 44 parcels service signals threshold blocks 3 and 5 is configured to operate in this mode. Synchronizer 18-15 ops you a series of strobe pulses - owls for generator 44, which then outputs a sluzhebduyu information posshku informing relatively transmitted coefficients and error vector samples. First, in the first case transmitted service information, setting up a receiving side in transition mode giving hand, followed by re-recording the number of counter 47 to the counter 41, then the synchronizer. In generates count pulse to the counter 42, the AND gate 43 but does not pass it to the input of counter 42 is generated after a series of strobe pulses for the encoder 46 and the block error memory 9 of the error, resulting in a communication channel 19 through the adder 47 is transmitted encoded samples of the error vector. Then, in the first case, transmitted koeffitsipriemnoy side of the transfer coefficients 20enty-premise and end of the cycle trans-tomers. Simultaneously with the transfer case-chi. After that you synchronizer 18-zhebnoy charge exchange of information takes place a full reset of the transmitting side and the number of pis counter 42 down counter 41 to pulse from the synchronizer 18 and then attempt to increase the threshold 25Vyhody blocks 3 and 5, is m - NIN contents of the counter 42 by pulse - with the active state. In this case, Su bills from synchronizer 18, but since the second input of AND gate 43 low level signal, then increasing. "" "" Of the counter 42 does not proizoydet.zozhimogo counter 42, since the transfer overhead vtoPosle informatsiirom input of the AND gate 43-high level on a series of strobe, pulse-hearth goes into an idle state. The third case. EVOS. case work output unit 10 is completely analogous to the second case, only an increase vtoln sodervaemyh sootvettvuyuschy to 45 encoder input coefficients and subtracting the input 41 of the counter, there is a serial poll the switch 40 of the groups of data inputs on which set of coefficients, and connect them to the data inputs of the encoder 45 coefficients, which encodes and sends them to the last through the adder 47 into the channel 19 communication. In establishing a zero value counter 41 and an active level signal at the output of synchronizer 18 Loan 41 to counter is active signal, which notifies the synchronizer 18 on the end of the transmission, thus synchronizing the torus 18 gates generator 44, CQ forming end signal transmission to the receiving side (11); and then resets the corresponding blocks ne-i Reda side and enters an idle state. signal level and the generator 44 produces in this case a parcel service codes for the receiving side, 35 containing information on the resolution of forming a new baseline signal at the receiving side. After the occurrence of the signal synchronizer 18 to Loan-recorded readings normalized vector error torus 40 in unit 12-j is then dumped by a corresponding blocks of the transmitting side, and enters an idle state. 45 55 Figure 6 shows the functional block diagram of the input block 21 receiving one-g hand. Decoder 48 extracts the official business; tion information of the input signal determines the mode of operation of the transmitting side, on the control signals adjusts the synchronizer 26 on the production of the corresponding mode and the reception timing of the strobe pulse sequence, and also triggers synchronizer 26, provided that the corresponding service code sequence. -Those - BoE second case. E, g - BOE - threshold level output blocks 3 and 5, respectively, or 1, and hence the coefficients of the samples are transmitted error vector. First, in the first case transmitted service information, setting up a receiving side in transition mode giving hand, followed by re-record number of 47 meter in the meter 41, then the synchronizer. In generates count pulse to the counter 42, the AND gate 43 but does not pass it to the input of counter 42 is generated after a series of strobe pulses for the encoder 46 and the block error memory 9 of the error, resulting in a communication channel 19 through the adder 47 is transmitted encoded samples of the error vector. Then, in the first case, the coefficients are transmitted and parcel of cycles before the end of the chi. Thereafter, the synchronizer 18 is fully-you reset the transmitting side and outputs the threshold blocks 3 and 5, is a t-active state. In this case, coefficients and parcel of the end of the cycle lane chi. Thereafter, the synchronizer 18 is full reset the transmitting side outputs of threshold units 3 and 5 with locat in the active state. This enters the idle state. The third case. EVOS. coefficients and parcel of cycles before the end of the chi. Thereafter, the synchronizer 18 is fully-you reset the transmitting side and outputs the threshold blocks 3 and 5, is a t-active state. In this case. "" "" Extensible counter 42, so as to work vtochae output unit 10 is completely analogous to the second case, only an increase vtoln soderrom input of the AND gate 43 high level of signal generator 44 generates in this case, the code official sending to the receiving side, containing information on the resolution of forming a new baseline signal at the receiving side. After the occurrence of the signal synchronizer 18 to Loan-writes the normalized samples of the vector error in a block 12-j is then dumped by a corresponding blocks of the transmitting side, and enters an idle state. In Figure 6 shows a functional block diagram of the input unit 21 receiving one-g hand.Decoder 48 extracts the official business; tion information of the input signal determines the mode of operation of the transmitting side, on the control signals adjusts the synchronizer 26 on the production of the corresponding mode and the reception timing of the strobe pulse sequence, and also triggers synchronizer 26, provided that the corresponding service code sequence. Thus, the baseband digital signal is input to the register 63sdviga clocked by the reference frequency f. Decoder 64 separates the two adjustment signal which is stored in the first flip-flop 68, and then the trigger 69 after this start signal 64formiruet decoder synchronizer 28. At the end of the information frame decoder 64 extracts the token transmitting end, which is stored in the trigger 70 and informs synchronizer 26 on the receiving end of a

cycle. At the end of processing frame synchronizer 68-70 flip-flops 26 resets to its initial state. In case of transfer of some coefficients decoder 48 outputs not active ized (0.0), the output of the synchronizer 26 is not active, so demultiplex-sor 42 connects the data inputs of the input unit 21 through the decoder 51 to the block 23 coefficients memory coefficients previously set to the recording mode, which is recorded by a series of clock pulses decoded by the decoder 51 counts the coefficients. If the number of coefficients. less than the maximum, after signal la transmission output of the decoder 51 is set zero, and synchronizer 26 fills the remaining memory cell unit 23 counts of zero and unit 23 translates to AA reading. Therefore, the received coefficients gstvuyuschih outputs of block 74 are coefficients for recorded always strogoupravl guides pulse sequence specific memory cell soglasnost. Three address input unit 74 of the sequence number. Upon completion of the control inputs are (switching cycle Sheni reducing synchronization liver sequences) sinhroni40 torus 26 sets decoder 48 in an initial state, and he goes into an idle state. If the samples were transferred to the error vector and the coefficients (0.1 setting levels), the decoder 48 and synchronizer 26 through demultiplex-sor 49, when mounted on its address input signal synchronizer 26 and the decoder 50 errors recorded samples of the error vector in the drive 52 errors for which the recording mode is set, and the guides are generated strobe pulses. Coefficients are then received similar consideration of the procedure. If the coefficient is less than the maximum number j, after the end of transmission of the signal synchronizer 26 zero-fills the remaining memory cell block 23. Congestion synchronizer 26 18 (26), controllable threshold unit 3 and 5, and the output unit 10 (the input unit 21 for the receiving side). Synchronizer 18 (26) generates control signals to those 45 long as the output unit 74 does not lock ustanovits low, prohibiting passage clock input of the counter 73. Switching (setting) sinhroni50 mash 18 (Y6) occurs by gating unit 72 memory ti corresponding to the write signal output unit 74. to the memory unit 72 is recorded while the signals 55 at its set input. Cleaning block 72 the contents of the memory is performed at start synchronizer 18 (26). Comparison of the efficiency of the device with the basic object-0 20 performed this mode does not generate a reception signal for reinforcing the normalizer 20, the control unit 21 to record samples of the error vector, so as to form a new reference signal is prohibited. After completion of 26 cycles of clock recovery decoder 48 sets the initial state, and the switches to idle. In the third case, the transfer of samples of the error vector, coefficients and insider information about recording new basic signal input operation unit 15, 21 is completely analogous to that considered only is permitted to record a new baseline signal through the normalizer 20 block memory 22 basis signals. After completion of the cycle of forming a new basic synchronizer signal decoder 26 sets 48 in an initial state, and he goes into an idle state. Synchronizer 18 (26) 25 operates as follows. Upon start pulse signal resets the counter 73 and the corresponding output block 74 block the permanent memory, a second input connected to AND gate 71, set the high level signal, the clock pulses fed to the counting input of the counter 73 which begins to touch the block address 74, and sootvet30 congestion at 18 (26), controllable threshold unit 3 and 5, and the output unit 10 (the input unit 21 for receiving side). Synchronizer 18 (26) generates control signals as long as the output unit 74 does not lock ustanovits low level, prohibiting the passage of the clock input to counter 73. Switching (tuning) of the synchronizer 18 (Y6) occurs by strobing the memory unit 72 a signal recording the corresponding output unit 74. At block 72 the memory is recorded while the signals at its inputs fixed. Cleaning block 72 the contents of the memory is performed at start synchronizer 18 (26). Comparison of the effectiveness of the device with basic object-performed 151449989 16 n elk with the same input sigma-connected through a communication channel with the corresponding le. As input data inputs was used sponding bely noise, missed input unit receiving side through a low pass filter with a given first - fourth inputs and controls - governmental parameters. When the dimension of inputs of the input unit connected to the input vector and 64 points, respectively, with a given input Start, lane-medium accuracy 1 percent reduction Vym - third ustanovochnm inputs forming the basis of the proposed and the corresponding first output device was completed on 23 th vector of the synchronizer, the second output re-sync, and famous - to 31-m yektore, ronizatora connected with the corresponding compression rate thus increased by control inputs schimi normalization by almost 30 percent. Furthermore, the reduction. torus, multipliers, which yields the number of basis vectors, with the corresponding first trebuyuschih.soedineny expensive rdah memory devices, with 15 inputs of the adder, the clock input leads to a reduction of their cost, and synchronizing the receiving side also reduces in-time signal processing-l a second clock input channels-mouth after forming the basis. Ta roystva characterized Thus, informative proposed, that, with a view to increasing the information device zhenogr vache least 20 EEL device. in his re-than 100 percent informative known side giving introduced shaper nogo.porogovogo signal analyzer activity, the second threshold unit, quad-claims quadric adder, subtractor and chet25 Werth memory block outputs of the second one. transmission apparatus and PRIE-storage unit connected to the corresponding ma-information containing all the relevant pass on the first inputs of the subtractor ing side synchronizer, the first and second data inputs of the first and the third - the seventh which outputs. - Activity analyzer which outputs are connected respectively to the control cerned zone L are connected to respective input yuschim first memory block, the first data inputs, a control input of the first threshold and second threshold-block, and the formation of the block-matching control yuschi bodies threshold signal E which outputs of correlators, the first controlled w - cerned are connected to respective inputs schimi output unit, 35 first information input unit inputs the second control unit yu1tsimi memory whose outputs are connected to the memory, the gate inputs of normalization with the corresponding first congestion information and the first inputs of the gate inputs of the first threshold Zion third a storage unit, the output of the first block, the first information input of the threshold unit 40 is connected to the second correlators and the second information input of the control unit inputs an output of the analyzer and the activity of the union first mounting Nena-input sync, respectively, and are connected to roizatora outputs information input from the normalizer devices are connected to the second information-rye homonymous data inputs correlation E inputs of the third block of memory, 45 I tori connected to the corresponding outputs are connected to the corresponding outputs from the third storage unit, second sponding first inputs of multipliers corresponding inputs are connected to the corre- sponding multipliers whose outputs corresponding eponymous correlation - sootvetstvuyuschimitorov connected to the outputs of the adder are connected to inputs of the adder outputs then-gQ correlation with the respective second inputs connected to respective moat per-subtractor which outputs compound Vym information input Output-Nena with relevant information - th block, data inputs of the second-fourth block entrances onnyimi pas-cerned of the memory, input Start and so th minute and quadratic adder you-The quantum input synchronizer are gg moves are connected to the corresponding input information are respectively the second-sponding E information, input Start and first clock.First input, a second input of the threshold, the first outputs and the shaper block threshold output signal of the transmitting side unit, the first control input signal threshold 1714A998918 shaper outputs, which are connected to respective inputs and pervg memory unit, the second outputs of the adder connected to respective first inputs isTOporo subtractor whose outputs are connected to the cor WMOs respective first and second control input of the third memory unit are combined and connected to the output of the first threshold unit, a second control input of the threshold unit connected to the second output of the synchronizer, the second output of the threshold unit connected to the third control - a third adder rows, the outputs of which are connected to respective second input yuschim output unit 1Q and the second inputs of the memory, the second adjusting inputs input synchronizer, the outputs of the fourth memory block are connected to corresponding data inputs of the normalizer and second data inputs of the output unit 15, a second whose output is connected to a third input of the installation-sync ronizatora, eighth - eleven whose outputs are respectively connected to corresponding input of the gate 20 and the third adder obedinenvhodami activity analyzer, the gate inputs of the adder quadratic, the gate input of the fourth memory block and the second inputs of the gate shaper threshold signal on the reception side memory blocks introduced n tye outputs the input block are connected to respective second inputs of the adder and the data inputs of the normalizer which outputs are connected with the same inputs of the first information storage unit, a first control input of which is connected to a fourth input to the output unit outputs a first block memory connected to respective first inputs of respective multipliers with TM, sixth outputs coupled to the input unit, the respective information adder 40 and inputs the combined sootvetstnyimi vtrogor memory unit which outputs are connected with the corresponding respective second inputs of multipliers, and the third Tide fourth synchronizer outputs respectively connected to respective inputs of the gate of the second memory block and the second inputs of the gate of the first storage unit outputs the sum of the torus are output devices,

Classifications:

International (IPC 8-9): G08C19/28 (Advanced/Invention);
G08C19/16 (Core/Invention)

International (IPC 1-7): G08C19/28



Family:

Publication number	Publication date	Application number	Application date
SU1449989 A1	19890107	SU19874213655	19870320

Priority:

SU19874213655 19870320

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Inventor(s): ZARITSKIY ANATOLIY F SU ; ZARITSKIY ALEKSANDR F SU ; SVALOV YURIJ L SU

12) Family number: 28199908 (US2002051619A)

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Title: **Distortion analyzer**

Abstract: A **distortion analyzer** for generating a distortion signal based on an input signal. For example, the distortion signal may be generated by adding a first signal corresponding to the entire spectrum of the input signal to a second signal corresponding to a low-frequency component of the input signal and then subtracting from the result of addition a third signal corresponding to a specific frequency band of the input signal. The effect of polarization mode dispersion that an optical signal experiences as it propagates through an optical transmission fiber may be compensated for at a receiver using a birefringent compensator, in which the **distortion analyzer** continuously examines the signal outputted by the compensator and supplies the distortion signal to the compensator, which causes the compensator to reduce the effect of such polarization mode dispersion based on the level of the distortion signal.

Classifications:

International (IPC 8-9): G01R23/20 G02B6/34 H04B10/02

H04B10/07 H04B10/08 H04B10/18 H04B10/2507

H04L25/06 (Advanced/Invention);

G01R23/20 H04B10/08 H04B10/18 (Core/Invention)

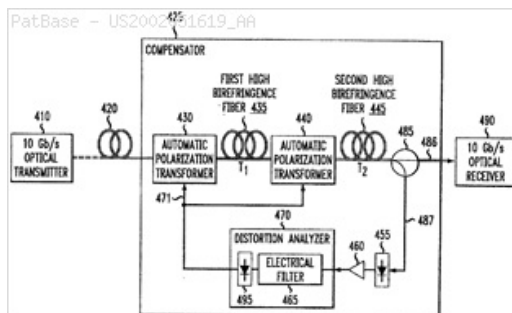
International (IPC 1-7): G01R23/20 G02B6/00 G02B6/26 G02B6/34

G02F1/00 H04B10/02 H04B10/08 H04B10/18 H04L25/06

CPC: H04B10/2569

European: H04B10/2569

US: 385/11 385/147 385/147P 385/15 385/15S 385/28 398/65 398/9



Family:

Publication number	Publication date	Application number	Application date
CA2327709 AA	20010616	CA20002327709	20001206
CA2327709 C	20041019	CA20002327709	20001206
CA2449694 AA	20010616	CA20002449694	20001206
CA2449694 C	20040831	CA20002449694	20001206
CA2450499 AA	20010616	CA20002450499	20001206
CA2450499 C	20040810	CA20002450499	20001206
CN1309305 A	20010822	CN20001036613	20001215
DE60024208 D1	20051229	DE20006024208	20001208
DE60024208 D1	20051229	DE20006024208T	20001208
DE60024208 T2	20060803	DE20006024208T	20001208

DE60026626 D1	20060504	DE20006026626T	20001208
DE60026626 D1	20060504	DE20006026626	20001208
DE60026626 T2	20061102	DE20006026626T	20001208
EP1109338 A2	20010620	EP20000310928	20001208
EP1109338 A3	20040107	EP20000310928	20001208
EP1109338 B1	20051123	EP20000310928	20001208
EP1494373 A2	20050105	EP20040021861	20001208
EP1494373 A3	20050112	EP20040021861	20001208
EP1494373 B1	20060308	EP20040021861	20001208
JP2001211120 A2	20010803	JP20000381365	20001215
US2002051619 AA	20020502	US20010997058	20011129
US6330375 BA	20011211	US19990465152	19991216
US6411750 BA	20020625	US20010997058	20011129

Priority:

US19990465152	19991216	CA20002327709	20001206	CA20002327709	20001206
CA20002449694	20001206	CA20002450499	20001206	EP20000310928	20001208
EP20000310928	20001208	US20010997058	20011129		

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Designated states: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

13) Family number: 1119938 (US3862380A)

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Title: INTERMODULATION **DISTORTION ANALYZER**

Abstract: An intermodulation **distortion analyzer** generates two pairs of sinusoidal test tones to serve as a test signal for the channel under test. The two pairs of tones simulate two respective noise band test signals but eliminate the long time averaging required for measurements when noise bands are used. A highly linear AGC circuit employs sampling at an output-controlled duty cycle to maintain a constant reference level for the analyzer. This reference level permits automatic distortion measurements to be read out directly in db below the test signal. An RMS detector circuit for second order intermodulation products employs feedback control to maintain the input signal to a squaring circuit constant. Squaring of the constant level sinusoids produces RMS DC components which can be separated for direct measurement. A distortion circuit provides known levels of second and third order intermodulation in the test signal to permit accurate check out of the analyzer.

Classifications:

International (IPC 8-9): H03G3/20 H03G3/30

H04B3/46 (Advanced/Invention);

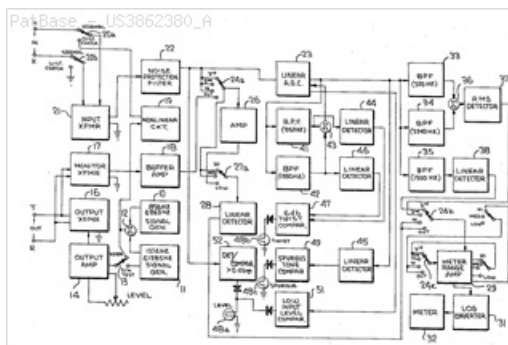
H03G3/30 (Core/Invention)

International (IPC 1-7): G01R23/20 H03B21/00 H03G3/00 H04B3/02 H04B3/46 H04M11/06 H04M7/00

CPC: H03G3/20 H03G3/3026 H04B3/46

European: 21AD71F H03G3/20 H03G3/30B8 H04B3/46

US: 179/175.3R 324/132 324/624 327/331 327/332 327/348 327/91 328/144 330/10 330/127 379/22.02 455/226.1



Family:

Publication number	Publication date	Application number	Application date
DE2406001 A1	19741031	DE19742406001	19740208
DE2406001 B2	19800410	DE19742406001	19740208
DE2406001 C3	19801127	DE19742406001	19740208
FR2325252 A1	19770415	FR19740001120	19740114
FR2325252 B1	19780324	FR19740001120	19740114
US3862380 A	19750121	US19730352552	19730419
US3940703 A	19760224	US19740497482	19740814
US3963992 A	19760615	US19740497483	19740814

Priority:

US19730352552	19730419	US19740497482	19740814	US19740497483	19740814
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Inventor(s): (std): HEKIMIAN NORRIS C ; TURNER JAMES F

Inventor(s): C HEKIMIAN NORRIS ; F TURNER JAMES

Title: ANALYZER SYSTEM USING PHASE DISTORTION MEASUREMENTS

Abstract: (Claim 1) is indi- 7(1 claim: cated at 4. Said **filter** circuit will select two components A phase **distortion analyzer** comprising a first constant of its square wave input and provide a single output which frequency signal means connected to an input of a divider; said divider having an output connected to an input of a selective **filter** which selects two components of its input and provides an output which has two frequencies; a second constant frequency signal means; a first mixer connected to said second signal means and the output of said **filter** for mixing said two frequencies with a second constant frequency of said second signal means; said mixer having an output which is connected to an input of a second mixer; a sweep generator connected to a second input of said second mixer; said second mixer m'x,ng a swept frequency output of said sweep generator with the output of said first mixer whereby the two frequencies are _swept linearly; the second mixer having an output which is connected to a linear electrical circuit element; a spectrum analyzer having an input connected to an output of said circiit elerlient for mei_uring the relative phase of the two frequencies_- said spectrum analyzer also having inputs connected to said first constant frequency signal means and said sweep generator; and a display means connected to an output of the spectrum analyzer.

Classifications:

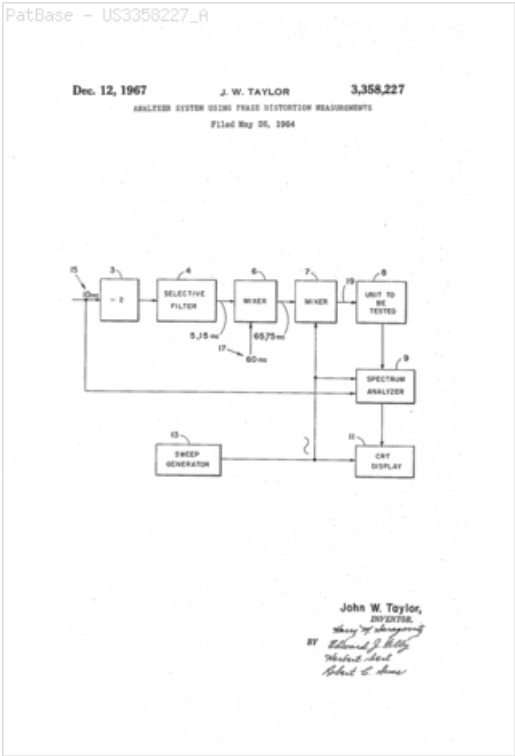
International (IPC 8-9): G01R27/32 (Advanced/Invention); G01R27/00 (Core/Invention)

International (IPC 1-7): G01R27/28

CPC: G01R27/32

European: G01R27/32

US: 324/622 324/76.23



Family:

Publication number	Publication date	Application number	Application date
US3358227 A	19671212	US19640370389	19640526

Priority:

US19640370389 19640526

Probable Assignee:

TAYLOR JOHN W

Assignee(s): (std):

TAYLOR JOHN W

Inventor(s): (std):

TAYLOR JOHN W

Title: TELEGRAPH **DISTORTION ANALYZER**

Abstract: (Claim 1) Having thus described my invention, what I claim and d_sike to secure by Letters Patent, is: 1.

Classifications:

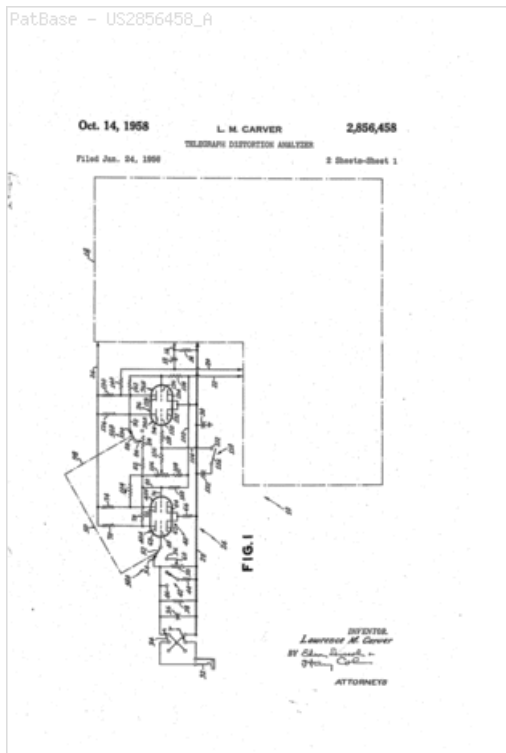
International (IPC 8-9): H04L12/26 H04L25/04 (Advanced/Invention); H04L12/26 H04L25/04 (Core/Invention)

International (IPC 1-7): H04L11/12

CPC: H04L1/248

European: H04L1/24M

US: 178/69.00A 178/69A

**Family:**

Publication number	Publication date	Application number	Application date
US2856458 A	19581014	US19560561000	19560124

Priority:

US19560561000 19560124

Probable Assignee:

STELMA INC

Assignee(s): (std):

STELMA INC

Inventor(s): (std):

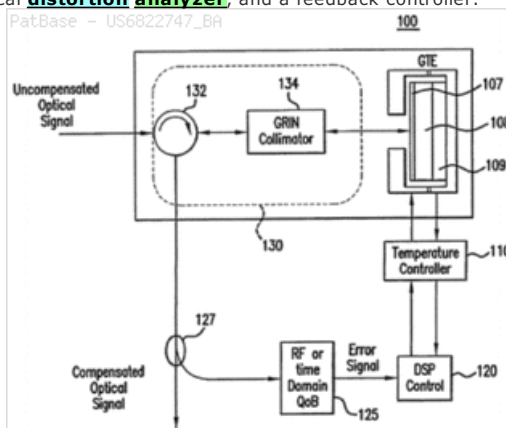
CARVER LAWRENCE M

16) Family number: 31345965 (US6822747B)

© PatBase

Title: Methods and apparatus for chromatic dispersion compensation**Abstract:** Methods and apparatus for chromatic dispersion compensation are provided. The apparatus includes a Gires-Tournois etalon, an optical beam separator, a GTE controller, an optical **distortion analyzer**, and a feedback controller.**Classifications:****International (IPC 8-9):** G02B6/34 (Advanced/Invention);

G02B6/34 (Core/Invention)

International (IPC 1-7): G01B9/02**CPC:** G02B6/29358 G02B6/29394 G02B6/29395 G02B6/29398**European:** S02B6/293W14**US:** 356/519**Family:**

Publication number	Publication date	Application number	Application date
US6822747 BA	20041123	US20020191486	20020710

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US20010304294P 20010710

US20020191486 20020710

Probable Assignee: STRATALIGHT COMMUNICATIONS INC**Assignee(s):** (std):

YAFO NETWORKS INC

Assignee(s):

STRATALIGHT COMMUNICATIONS INC

Inventor(s): (std):

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