

Search query (9): [SP]: backgroundfield of the disclosure[0001] the present invention relates to an interface, method and computer program product for controlling the transfer of electronic messages.description of the related art[0002] the "background" description provided herein is for the purpose of generally presenting the context of the disclosure. work of the presently named inventors, to the extent it is described in the background section, as well as aspects of the description which may not otherwise qualify as prior art at the time of filing, are neither expressly or impliedly admitted as prior art against the present invention.[0003] modern electronic banking systems allow funds to be electronically transferred between bank accounts of different banks using electronic transaction request messages (transaction messages). such a method of transferring funds is both secure (making use of various known security protocols which allow secure transfer of data over a network) and convenient (since it allows bank account holders to make requests to transfer funds at any time, 24 hours a day, 365 days a year).[0004] however, although such electronic transaction request messages may be made at any time, funds are only actually transferred between banks on a periodic basis. this is known as a "settlement cycle" model. during each settlement cycle, transaction messages issued by banks are received and recorded. then, at the end of the settlement cycle, funds are actually transferred between banks (this is known as "settlement"), on the basis of the recorded transaction messages. the time period between settlement cycles is typically 8, 12 or 24 hours, although any other suitable time period may be used.[0005] because the eventual settlement between banks is based on the recorded transaction messages made during the settlement cycle, it is of the utmost importance that the recorded transaction messages are stored and managed effectively, even in the case of, for example, a technology failure or natural disaster. this ensures that, at the end of each settlement cycle, each completed transaction is taken into account during settlement and is only taken into account once. this prevents any overpayment or underpayment of real money between banks. the present invention therefore aims to alleviate at least the problem of providing a resilient and flexible system for effectively storing and managing electronic transaction messages.summary[0006] the present invention provides an interface for controlling the transfer of electronic transaction messages between a first financial institution and a plurality of switches distributed amongst a plurality of switch sites, wherein the first financial institution and the plurality of switches are connected via a data communications network, the interface comprising communication circuitry, processing circuitry and memory storing the operational status of each switch site, wherein the communication circuitry is operable to transmit a test message to one of the switch sites over the data network if no transaction message has been received from that switch site for a predetermined time, and in response to the test message, the communication circuitry is operable to receive an echo of the test message from the switch site wherein the processing circuitry is operable such that if the echo is received within a defined time then the operational status of the switch site is set as operational and if the echo is not received within the defined time then the operational status of the switch site is set as not operational whereby in the event that the operational status of the switch site is set to not operational, the processing circuitry is operable such that no electronic messages are transferred to the switch site.[0007] advantageously, this arrangement means that electronic messages are not sent to switch sites which are determined to be unavailable and unable to accept messages. as well as this reducing the risk that messages become corrupted or lost, this also means that processing and network capacity are not wasted with messages which cannot be delivered. processing and network efficiency are therefore improved.[0008] in an embodiment, the communication circuitry is operable to send a further test message to a non-operational switch site after a specified period.[0009] in an embodiment, the memory is operable to store the operational status of a second financial institution connected to the plurality of switches via the data communications network the communication circuitry is operable to receive information from one or more of the plurality of switches indicating an updated operational status of the second financial institution and the processing circuitry is operable to update the operational status of the second financial institution stored in the memory on the basis of the information received from the one or more switches, wherein: in the case that the operational status of the second financial institution indicates that the second financial institution is not operational, the processing circuitry is operable prevent electronic transaction messages instructing a transaction from the first financial institution to the second financial institution from being transmitted to the switches.[0010] in an embodiment, the information indicating the updated operational status of the second financial institution is generated by one or more of the plurality of switches on the basis of either a lack of a response of a test message transmitted to the second financial institution by each of the switches within a predetermined period of time or an indication to one or more of the plurality of switches by the second financial institution that the second financial institution is to be disconnected from the data communications network.[0011] the present invention provides a method of controlling the transfer of electronic transaction messages between a first financial institution and a plurality of switches distributed amongst a plurality of switch sites, wherein the first financial institution and the plurality of switches are connected via a data communications network, the method comprising transmitting a test message to one of the switch sites over the data network if no transaction message has been received from that switch site for a predetermined time, and in response to the test message receiving an echo of the test message from the switch site wherein if the echo is received within a defined time then the operational status of the switch site is set as operational and if the echo is not received within the defined time then the operational status of the switch site is set as not operational whereby in the event that the operational status of the switch site is set to not operational, the method comprises transferring no electronic messages to the switch site.[0012] in an embodiment, the method comprises sending a further test message to a non-operational switch site after a specified period.[0013] in an embodiment, the method comprises storing the operational status of a second financial institution connected to the plurality of switches via the data communications network receiving information from one or more of the plurality of switches indicating an updated operational status of the second financial institution and updating the operational status of the second financial institution stored in the memory on the basis of the information received from the one or more switches, wherein: in the case that the operational status of the second financial institution indicates that the second financial institution is not operational, the method comprises preventing electronic transaction messages instructing a transaction from the first financial institution to the second financial institution from being transmitted to the switches.[0014] in an embodiment, the information indicating the updated operational status of the second financial institution is generated by one or more of the plurality of switches on the basis of either a lack of a response of a test message transmitted to the second financial institution by each of the switches within a predetermined period of time or an indication to one or more of the plurality of switches by the second financial institution that the second financial institution is to be disconnected from the data communications network.[0015] the present invention provides a computer program product comprising a storage medium upon which a computer program is stored, the computer program, when run on a computer, configures the computer to perform the above-mentioned method of the present invention.[0016] the foregoing paragraphs have been provided by way of general introduction, and are not intended to limit the scope of the following claims. the described embodiments, together with further advantages, will be best understood by reference to the following detailed description taken in conjunction with the accompanying figures.brief description of the drawings[0017] a more complete appreciation of the disclosure and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:[0018] fig. 1 shows various components of a system according to an embodiment[0019] figs. 2a-b show a flow chart showing various processing steps applied to a transaction message by a switch forming part of the system, according to an embodiment[0020] fig. 3a illustrates a problem associated with implementing a debit cap using the system[0021] fig. 3b illustrates a solution to the problem illustrated by f

Results: 8

Nicolas Vargas

Title: AN INTERFACE, METHOD AND COMPUTER PROGRAM PRODUCT FOR CONTROLLING THE TRANSFER OF ELECTRONIC MESSAGES

Abstract: The present invention provides an interface for controlling the transfer of electronic transaction messages between a first financial institution and a plurality of switches distributed amongst a plurality of switch sites, wherein the first financial institution and the plurality of switches are connected via a data communications network, the interface comprising communication circuitry, processing circuitry and memory storing the operational status of each switch site, wherein the communication circuitry is operable to transmit a test message to one of the switch sites over the data network if no transaction message has been received from that switch site for a predetermined time, and in response to the test message, the communication circuitry is operable to receive an echo of the test message from the switch site; wherein the processing circuitry is operable such that if the echo is received within a defined time then the operational status of the switch site is set as operational and if the echo is not received within the defined time then the operational status of the switch site is set as not operational; whereby in the event that the operational status of the switch site is set to not operational, the processing circuitry is operable such that no electronic messages are transferred to the switch site.

Classifications:

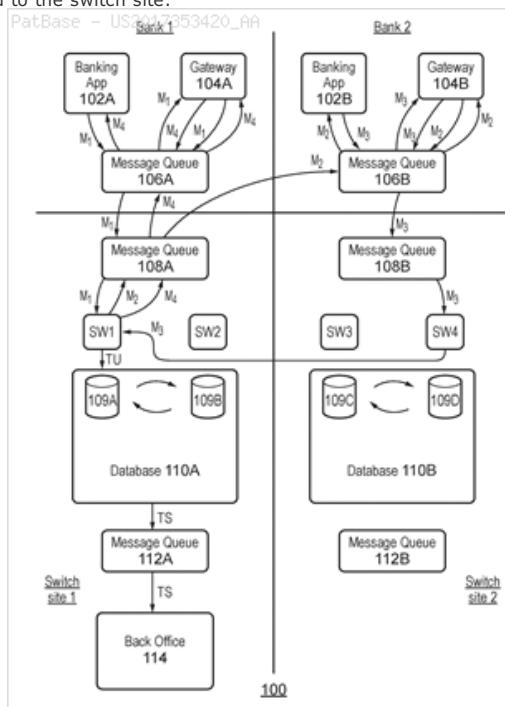
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G06Q20/02 G06Q20/38 G07F19/00 (Advanced/Non-invention)

CPC: H04L43/10 G06Q20/00 G07F19/00 H04L29/14 H04L43/0805 H04L69/40 H04L51/30 G06Q20/027 G06Q20/3827

JP F-Term: 5B089 5B089/GA01 5B089/GA32 5B089/GB02 5B089/JA03 5B089/JB01 5B089/KA12 5B089/KC17 5B089/MC12 5B089/ME06 5K030 5K030/GA12 5K030/LB05 5K030/MA03 5K030/MB01 5K030/MC03 5K030/MC08 5K030/MD02 5L055 5L055/BB34

JP F-Index: G06F13/00/351/M G06Q40/02 H04L12/721/Z



Family:

Publication number	Publication date	Application number	Application date
AU2015365699 AA	20160623	AU20150365699	20151014
CA2971684 AA	20170616	CA20152971684	20151014
CO20170007205 A2	20170929	CO20170007205	20170718
EA201791342 A1	20171130	EA20170091342	20151014
EP3235187 A1	20171025	EP20150784120	20151014
GB2533562 A1	20160629	GB20140022637	20141218
IN201717021286 A	20171208	IN201717021286	20170617
JP2018504863 T2	20180215	JP20170551374T	20151014
SG11201704899T A1	20170728	SG20171104899	20151014
US2017353420 AA	20171207	US20150537129	20151014
WO16097675 A1	20160623	WO2015GB53042	20151014

Priority:

GB20140022637 20141218 WO2015GB53042 20151014

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Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: Multipoint polling technique

Abstract: A multipoint polling system wherein a multipoint switch selectively connects a plurality of remote terminals to a central station in response to remote terminal addresses transmitted on a signaling path to the multipoint switch. Polling apparatus stores portions of a remote terminal address list provided by the central station and transmits individual ones of the stored remote terminal addresses on to the signaling path. The polling apparatus periodically requests different portions of the remote terminal address list and replaces the stored remote terminal address portion with the requested remote terminal address portion.

Classifications:

International (IPC 8-9): G06F13/00 G06F15/16 G06F15/177
H04Q5/00 H04Q9/00 H04Q9/14 (Advanced/Invention);

G06F13/00 G06F15/16 H04Q9/14 (Core/Invention)

International (IPC 1-7): G06F11/00 G06F15/16 G06F15/30 G06F3/04
G08C19/00 G08C25/00 G11C H04B1/00 H04J3/04 H04L11/00
H04Q3/00 H04Q3/48 H04Q3/54 H04Q5/00 H04Q9/00

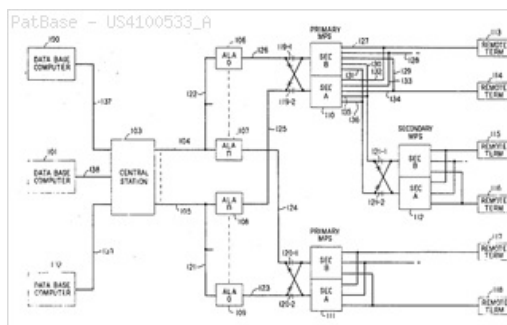
CPC: H04Q9/14

European: H04Q9/14

US: 178/3 340/147R 340/3.51 340/825.22 340/825.52 340/825.53
340/9.1 370/449 375/222

JP F-Term: 5B045 5B045/BB02 5B045/BB17 5B045/JJ44 5B089
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5K030/CB10 5K030/DB01 5K030/DB02 5K030/ED01 5K030/ED05
5K033 5K033/AA03 5K033/CA01 5K033/CA03 5K033/DA01
5K033/DB03 5K033/DB04 5K033/DB12 5K033/EA05

JP F-Index: G06F13/00/357/B G06F15/16/310/B G06F15/177/676/B H04L11/00/340 H04L11/02/Z H04L12/02/B
H04L12/44/M H04L12/44/103



Family:

Publication number	Publication date	Application number	Application date
BE861442 A	19780331	BE19770183121	19771202
CA1079829 A1	19800617	CA19770292057	19771130
DE2753532 A1	19780608	DE19772753532	19771201
ES464798 A1	19781101	ES19770464798	19771206
FR2373204 A1	19780630	FR19770036074	19771130
IT1089127 A	19850618	IT19770030336	19771202
JP53105143 A2	19780913	JP19770145785	19771206
NL7713155 A	19780608	NL19770013155	19771129
SE7713247 A	19780607	SE19770013247D	19771123
US4100533 A	19780711	US19760747700	19761206

Priority:

US19760747700 19761206

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Title: METHOD AND SYSTEM FOR FAULT-TOLERANT NETWORK CONNECTION SWITCHOVER

Abstract: A computer is connected to redundant network switches by primary and secondary connections, respectively. Test messages are sent across each connection to the attached switches. A break in a connection, or a faulty connection, is detected upon a failed response to one of the test messages. In response to this failure, traffic is routed across the remaining good connection. To facilitate fast protocol rerouting, a test message is sent across the now active connection bound for the switch connected to the failed connection. This message therefor traverses both switches causing each to learn the new routing. Rerouting is therefor accomplished quickly.

Classifications:

International (IPC 8-9): H04L12/24 H04L12/26 H04L12/56
H04L12/701 H04L12/703 H04L12/707 H04L12/721

H04L29/14 (Advanced/Invention);

H04L12/24 H04L12/26 H04L12/56 H04L29/14 (Core/Invention)

International (IPC 1-7): G06F11/00 H04L12/00 H04L12/24

H04L12/26 H04L12/56 H04L29/14

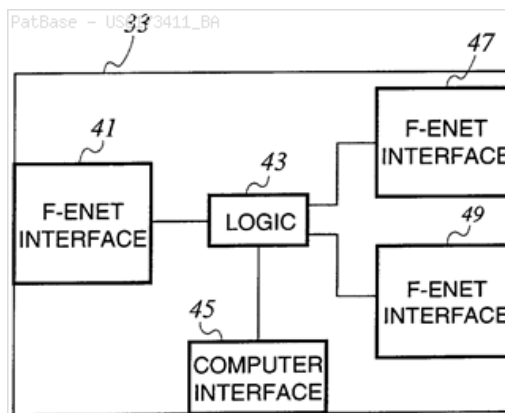
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H04L45/22 H04L45/26 H04L45/28

European: H04L12/24D3 H04L12/26T H04L41/06C2 H04L43/08C

H04L43/50 H04L45/00 H04L45/22 H04L45/26 H04L45/28 T04L41/06C

US: 709/223 714/4 714/4.3

**Family:**

Publication number	Publication date	Application number	Application date
AU199910990 A1	19990510	AU19990010990	19981016
DE69828810 D1	20050303	DE19986028810	19981016
DE69828810 T2	20060406	DE19986028810T	19981016
EP1025680 A2	20000809	EP19980953670	19981016
EP1025680 B1	20050126	EP19980953670	19981016
US6173411 BA	20010109	US19980059896	19980414
WO9921322 A2	19990429	WO1998US21984	19981016
WO9921322 A3	19990819	WO1998US21984	19981016
WO9921322 C2	19991007	WO1998US21984	19981016

Priority:

US19970062581P 19971020

US19970062984P 19971021

US19970062681P 19971022

US19980059896 19980414

WO1998US21984 19981016

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Inventor(s): (std): ALAN A GALE ; CUMMINGS A ; CUMMINGS GENE A ; GALE A ; GALE ALAN A ; GENE A CUMMINGS ; HIRST D ; HIRST MICHAEL D ; MICHAEL D HIRST

Designated states: AL AM AT AU AZ BA BB BE BF BG BJ BR BY CA CF CG CH CI CM CN CU CY CZ DE DK EE ES FI FR GA GB GE GH GM GN GR GW HR HU ID IE IL IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MC MD MG MK ML MN MR MW MX NE NL NO NZ PL PT RO RU SD SE SG SI SK SL SN SZ TD TG TJ TM TR TT UA UG UZ VN YU ZW

Title: SYSTEM AND METHOD OF MANAGING DATA TRANSMISSION LOADS

Abstract: A system and method of managing transmission loads in a data communication network implement a plurality of data processing modules, such as computer servers, each of which may be responsible for a limited range of data processing tasks. A load manager may distribute incoming data packets in accordance with the particular network transaction with which the data packets are associated as well as the present load at each of the plurality of data processing modules. A dedicated load manager, such as a computer server, may execute a hash function to direct incoming, data traffic and to allocate system resources.

Classifications:

International (IPC 8-9): H04L12/56 H04L29/06

H04L29/08 (Advanced/Invention);

H04L12/56 H04L29/06 H04L29/08 (Core/Invention)

International (IPC 1-7): G06F11/30

CPC: H04L65/1006 H04L65/1069 H04L65/4007 H04L29/06027

H04L47/10 H04L47/125 H04L67/1008 H04L67/1002 H04L67/1023

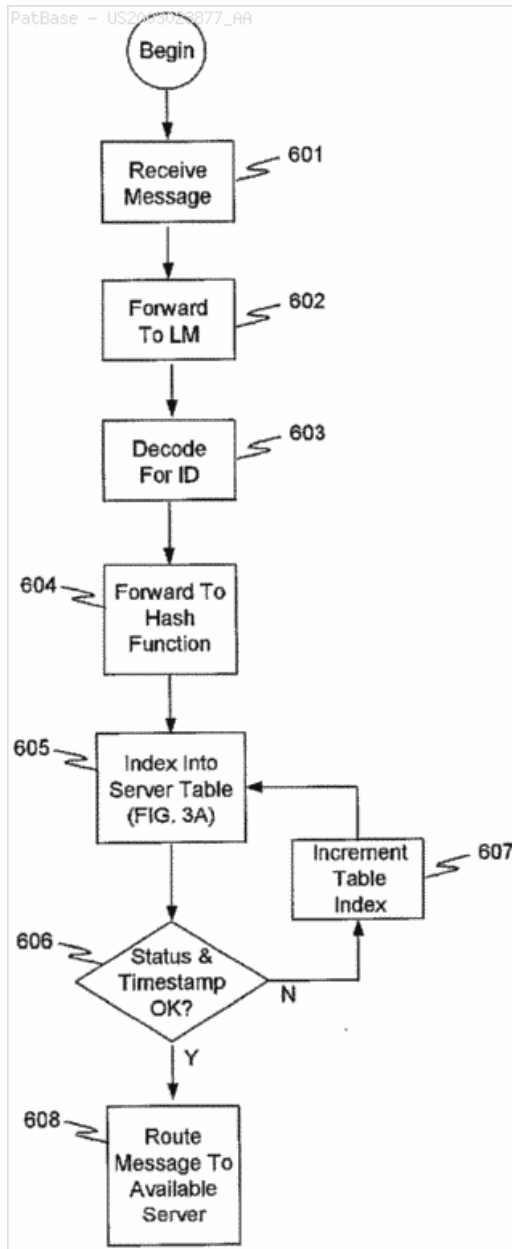
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US: 713/201 726/4 726/4P

**Family:**

Publication number	Publication date	Application number	Application date
US2003023877 AA	20030130	US20010919457	20010730

Priority:

US20010919457 20010730

Probable Assignee: LONGBOARD INC

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Inventor(s): (std): LUTHER MICHAEL ; TAVARES HUMBERTO M ; TERRY DAVID A

Title: COMPUTER SYSTEM THAT PREDICTS IMPENDING FAILURE IN APPLICATIONS SUCH AS BANKING

Abstract: To predice impending system failures, dummy messages are periodically transmitted from a surveillance computer via a message broker to a host computer that executes processes in response to electronic messages from terminals and returns an electronic message. The dummy electronic messages are time-stamped when transmitted from the surveillance computer, when received and transmitted by the message broker, and when a process is executed by the host. The surveillance computer predicts impending failures by comparing the time required while a transmitted dummy electronic message returns to the surveillance computer, a mean value of the required time, a time required while the dummy electronic message passes through the message broker, a mean value of the time for the passage, a time required for a dummy electronic message transmission between each computer and a mean value of the time for transmission to each base value.

Classifications:

International (IPC 8-9): G06F11/30 G06F13/00 G06F15/00

G07F19/00 H04L12/24 (Advanced/Invention);

H04L12/58 (Advanced/Non-invention);

G06F11/30 G06F13/00 G06F15/00 G07F19/00

H04L12/24 (Core/Invention);

H04L12/58 (Core/Non-invention)

International (IPC 1-7): G06F11/30 G06F13/00 G06F15/00

G06F17/60 H04L12/28

CPC: H04L51/00 H04L41/06 G07F9/026 G07F19/20 G07F19/207

G07F19/211 H04L41/147 H04L43/0817

European: G07F19/00 G07F19/00F G07F19/20 G07F19/207

G07F19/211 G07F9/02D H04L12/24D H04L12/26M3A2 H04L41/06

H04L41/14C H04L43/08D T04L12/58

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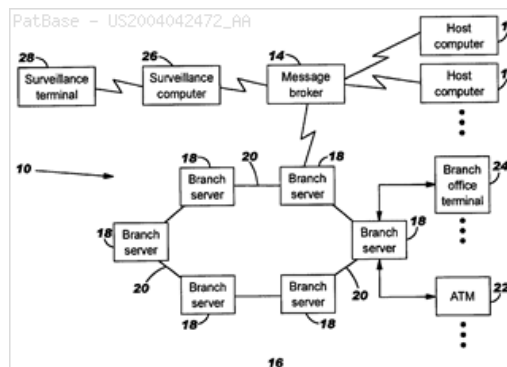
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5B185 5B185/AC12 5B185/CA04

JP F-Index: G06F11/30/310/H G06F13/00/351/N G06F15/00/320/L G06F15/00/470



Family:

Publication number	Publication date	Application number	Application date
JP2004046338 A2	20040212	JP20020200005	20020709
JP3737460 B2	20060118	JP20020200005	20020709
US2004042472 AA	20040304	US20030615437	20030708
US6896179 BB	20050524	US20030615437	20030708

Priority:

JP20020200005 20020709

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Agent(s): PIVNICHNY JOHN R; IRVIN DAVID R; DAVID R; JOHN R

Title: HIGH AVAILABILITY ETHERNET BACKPLANE ARCHITECTURE

Abstract: A high availability backplane architecture. The backplane system includes redundant node boards operatively communicating with redundant switch fabric boards. Uplink ports of the node boards are logically grouped into trunk ports at one end of the communication link with the switch fabric boards. The node boards and the switch fabric boards routinely perform link integrity checks when operating in a normal mode such that each can independently initiate failover to working ports when a link failure is detected. Link failure is detected either by sending a link heartbeat message after the link has had no traffic for a predetermined interval, or after receiving a predetermined consecutive number of invalid packets. Once the link failure is resolved, operation resumes in normal mode.

Classifications:

International (IPC 8-9): G01R31/08 G06F11/00 G06F11/20 H04L1/00 H04L12/24 H04L12/26 H04L12/28 H04L12/413 H04L12/44 H04L12/56 H04L29/14 (Advanced/Invention); H04L1/00 H04L12/56 (Advanced/Non-invention); H04L12/24 H04L12/26 H04L12/407 H04L12/44 H04L12/56 H04L29/14 (Core/Invention); H04L12/56 (Core/Non-invention)

International (IPC 1-7): G01R31/08 G01R31/08 G06F11/30 H04L1/00 H04L12/24 H04L12/26 H04L12/28 H04L12/44 H04L12/50 H04L12/56 H04L29/14 H04Q1/20

CPC: H04L69/40 H04L43/0811 H04L41/0663 H04L41/0677 H04L43/10 H04L43/103 H04L49/1523 H04L49/351 H04L49/552

European: H04L12/24D H04L12/26M3A1 H04L12/26M4 H04L41/06C1A H04L41/06D H04L43/08C H04L43/10 H04L49/15C1 H04L49/35A H04L49/55A T04L12/26M4A T04L29/14 T04L43/10A

US: 370/216 370/216P 370/216P 370/242 370/242S 370/245 370/248 370/249 370/338 370/375 370/375S 370/392 370/395.2 709/223 709/231 709/238 709/242

PatBase - US2004085893_AA

Patent Application Publication May 6, 2004 Sheet 1 of 6 US 2004/085893 A1

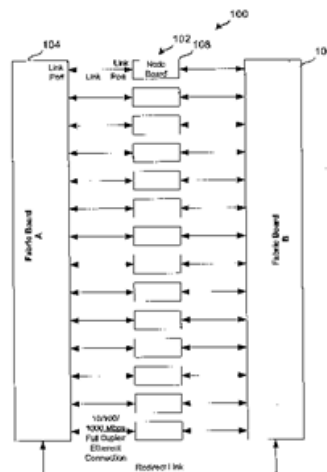


FIG. 1

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Publication number	Publication date	Application number	Application date
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DE10360190 A1	20040729	DE20031060190	20031220
EP1416671 A2	20040506	EP20030103925	20031023
EP1416671 A3	20060705	EP20030103925	20031023
FR2849731 A1	20040709	FR20030015000	20031219
KR20040055710 A	20040626	KR20030094263	20031220
TW200421777 A	20041016	TW20030130492	20031031
TW200422629 A	20041101	TW20030136285	20031219
TWI274886 B	20070301	TW20030136285	20031219
US2004085893 AA	20040506	US20020284856	20021031
US2004085894 AA	20040506	US20020326352	20021220
US7260066 BB	20070821	US20020326352	20021220
US7835265 BB	20101116	US20020284856	20021031

Priority:

US20020284856 20021031 US20020326352 20021220

Probable Assignee: SYNAPTICS INC

Assignee(s): (std): GALINK SEMICONDUCTOR V N INC ; GALINK SEMICONDUCTOR VN INC ; CONEXANT SYSTEMS INC ; ZARLINK SEMICONDUCTOR VN INC ; ZARLINK SEMICONDUCTOR V N INC

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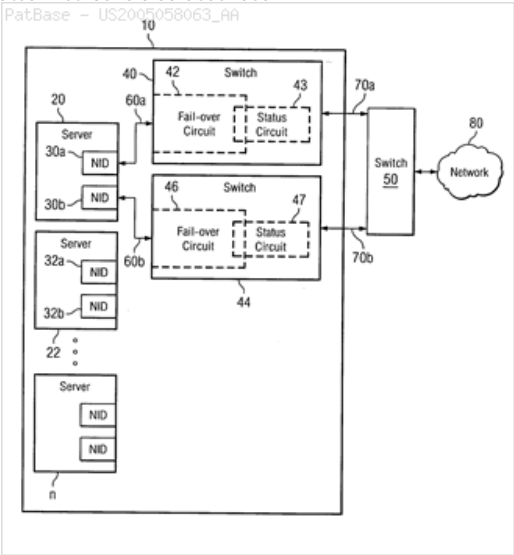
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Title: METHOD AND SYSTEM SUPPORTING REAL-TIME FAIL-OVER OF NETWORK SWITCHES

Abstract: An example embodiment of a system for providing fail-over between switches in a network may include a switch having a server-side port and a fail-over circuit in communication with the server-side port. The switch may also include a status circuit, in communication with the fail-over circuit. The switch may also include a switch-side port. The status circuit may communicate the link status of the switch-side port to the fail-over circuit. In response to receiving a link status of down for the switch-side port, the fail-over circuit may automatically disable the server-side port. A related system may include more than one switch, and the system may automatically fail-over from a first switch to a second switch, in response to the disablement of the server-side port in the first switch. At least one related method is also described.

Classifications:

International (IPC 8-9): H04L12/24 H04L12/26
H04L29/14 (Advanced/Invention);
H04L29/06 H04L29/08 (Advanced/Non-invention);
H04L12/24 H04L12/26 H04L29/14 (Core/Invention);
H04L29/06 H04L29/08 (Core/Non-invention)
International (IPC 1-7): H04L12/26
CPC: H04L67/1002 H04L67/1034 H04L69/40 H04L41/0663
H04L43/0817 H04L2029/06054
European: H04L12/24D3 H04L29/14 H04L41/06C1A H04L43/08D
T04L29/06C8A T04L29/08N9A T04L29/08N9A11
US: 370/217 370/217P



Family:

Publication number	Publication date	Application number	Application date
US2005058063 AA	20050317	US20030662833	20030915

Priority:

US20030662833 20030915

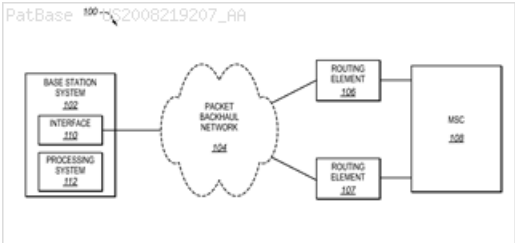
Probable Assignee:	DELL INC
Assignee(s): (std):	DELL INC ; DELL PRODUCTS LP
Assignee(s):	DELL PRODUCTS L P
Inventor(s): (std):	YANG YINGLIN ; MASUYAMA JINSAKU
Agent(s):	MICHAEL R BARRE BAKER BOTTS LLP

Title: BASE STATIONS ROUTING TRAFFIC OVER A PACKET BACKHAUL NETWORK TO MULTIPLE ROUTING ELEMENTS

Abstract: System, methods, and networks are disclosed that allow base station systems of a wireless communication network to transmit outgoing traffic over a packet backhaul network to multiple routing elements on the MSC side of the network. A base station system described herein identifies a primary routing element and a backup routing element. The primary routing element is the device to which the base station system transmits outgoing traffic under normal operation, and the backup routing element is an alternate to the primary routing element. To transmit traffic over the packet backhaul network, the base station system monitors the availability of the primary routing element. If the primary routing element is available, then the base station system transmits outgoing traffic over the packet backhaul network to the primary routing element. If unavailable, then the base station system transmits outgoing traffic over the packet backhaul network to the backup routing element.

Classifications:

International (IPC 8-9): G01R31/08 G06F11/00 G06F15/173
G08C15/00 H04J1/16 H04J3/14 H04L1/00 H04L12/26 H04L12/28
H04L12/56 H04Q7/00 H04W40/00 H04W40/02
H04W92/04 (Advanced/Invention);
H04B1/74 (Advanced/Non-invention);
H04L12/56 H04W40/02 (Core/Invention)
CPC: H04W92/045 H04B1/745 H04L45/00 H04L45/22 H04L45/28
H04W40/02
European: H04L45/00 H04L45/22 H04L45/28 H04W40/02
US: 370/217 370/237 370/328 370/328P 455/445 709/239



Family:

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US2008219207 AA	20080911	US20070681883	20070305
US8804486 BB	20140812	US20070681883	20070305
WO08109043 A2	20080912	WO2008US02804	20080303
WO08109043 A3	20081030	WO2008US02804	20080303

Priority:

US20070681883 20070305

Probable Assignee: PROVENANCE ASSET GROUP LLC

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Inventor(s): (std): CHEN INA Z ; VELTRI JOSEPH ; ZHANG QINQING

Agent(s): DUFT BORNSSEN AND FISHMAN LLP; DUFT BORNSSEN AND FETTIG LLP; BORNSSEN BRETT L

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN SV SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW