

Search query (6): [SP]: 1. a reference voltage generator, comprising: a temperature-dependent device a processing device comprising circuitry configured to process a reference voltage and digital representations of first and second voltages, the first and second voltages being derived from the temperature dependent device, and to output a value a digital to analog converter (dac) comprising circuitry configured to generate the reference voltage based on the value wherein the first voltage is proportional to absolute temperature (ptat) and the second voltage is complementary to absolute temperature (ctat), and wherein the reference voltage is substantially independent of absolute temperature in an operating temperature range of the reference voltage generator and wherein the reference voltage is fed back from the dac to the processing device. 2. the reference voltage generator of claim 1, wherein the temperature-dependent device comprises: a solid-state semiconductor device having first and second terminals, wherein the first voltage is a voltage drop across the first and second terminals when the solid-state semiconductor device receives a first current, and wherein the second voltage is a difference between (1) a voltage drop across the first and second terminals when the solid-state semiconductor device receives a second current and (2) the first voltage. 3. the reference voltage generator of claim 2, wherein the solid-state semiconductor device comprises a pn junction. 4. the reference voltage generator of claim 3, wherein the solid-state semiconductor device comprises a diode or a bipolar junction transistor (bjt). 5. the reference voltage generator of claim 2, wherein the solid-state semiconductor device comprises a bipolar junction transistor (bjt). 6. the reference voltage generator of claim 2, wherein the processing device comprises a controller configured to control a current source to produce the first and second currents. 7. the reference voltage generator of claim 1, wherein the processing device is configured to determine the value according to: $nbg = nbe1 + m * \Delta t_{anbe}$, wherein: nbe1 is the digital representation of the first voltage Δt_{anbe} is the digital representation of the second voltage and m is a constant scaling factor determined based on at least an operating temperature of the reference voltage generator and process parameters associated with the reference voltage generator. 8. the reference voltage generator of claim 1, wherein the processing device comprises a digital processing module configured to: compute a digital representation of a predetermined reference voltage based on the digital representations of the first and second voltages and determine an error based on a digital representation of the reference voltage and the computed digital representation of the predetermined reference voltage. 9. the reference voltage generator of claim 8, wherein the processing device is configured to control the dac to generate the reference voltage based on the error. 10. the reference voltage generator of claim 1, further comprising: an analog to digital converter (adc), wherein a gain of the adc is a function of the reference voltage, wherein the processing device is configured to compare a predetermined value with the value to generate an error, and wherein the processing device is configured to control the dac to generate the reference voltage based on the error. 11. the reference voltage generator of claim 1, further comprising circuitry configured to control a current used to generate at least one of the first and second voltages using the reference voltage. 12. a method of generating a reference voltage, comprising: determining, by a processing device, a value based on digital representations of first and second voltages, and a digital representation of a reference voltage and generating, by a digital to analog converter (dac), the reference voltage based on the determined value wherein the first voltage is proportional to absolute temperature (ptat) and the second voltage is complementary to absolute temperature (ctat), wherein the reference voltage is substantially independent of absolute temperature in a predetermined temperature range and wherein the reference voltage is fed back from the dac to the processing device. 13. the method of claim 12, further comprising: measuring the first voltage as a voltage across first and second terminals of a semiconductor device when the semiconductor device receives a first current and measuring a third voltage as a voltage across the first and second terminals of the semiconductor device when the semiconductor device receives a second current wherein the second voltage is a difference between the third and first voltages. 14. the method of claim 12, wherein the generating comprises: computing a digital representation of a predetermined reference voltage based on the digital representations of the first and second voltages determining an error based on a digital representation of the reference voltage and the computed digital representation of the predetermined reference voltage generating the reference voltage based on the error. 15. the method of claim 12, wherein the digital representations of the first and second voltages are generated using an analog to digital converter, further comprising: controlling a gain of the analog to digital converter using the reference voltage wherein the generating comprises: determining an error based on a predetermined value and a digital representation of the reference voltage generating the reference voltage based on the error. 16. the method of claim 12, further comprising: controlling a current used to generate at least one of the first and second voltages using the reference voltage. 17. a non-transitory computer readable medium carrying one or more sequences of one or more instructions for execution by one or more processors to perform a method for generating a reference voltage, execution of the instructions by the one or more processors causing the one or more processors to: determine, by a processing device, a value based on digital representations of a first and second voltages, and a digital representation of a reference voltage and generate, by a digital to analog converter (dac), a the reference voltage based on the determined value wherein the first voltage is proportional to absolute temperature (ptat) and the second voltage is complementary to absolute temperature (ctat), wherein the reference voltage is substantially independent of absolute temperature in a predetermined temperature range and wherein the reference voltage is fed back from the dac to the processing device. 18. the non-transitory computer readable medium of claim 17, wherein execution of the instructions by the one or more processors further causes the one or more processors to: measure the first voltage as a voltage across first and second terminals of a semiconductor device when the semiconductor device receives a first current and measure a third voltage as a voltage across the first and second terminals of the semiconductor device when the semiconductor device receives a second current wherein the second voltage is a difference between the third and first voltages. 19. the non-transitory computer readable medium of claim 17, wherein execution of the instructions by the one or more processors to generate the reference voltage further comprises causing the one or more processors to: compute a digital representation of an ideal reference voltage based on the digital representations of the first and second voltages determine an error based on a digital representation of the reference voltage and the computed digital representation of the ideal reference voltage and generate the reference voltage based on the error. 20. the non-transitory computer readable medium of claim 17, wherein the digital representations of the first and second voltages are generated using an analog to digital converter wherein execution of the instructions by the one or more processors further causes the one or more processors to control a gain of the analog to digital converter using the reference voltage and wherein execution of the instructions by the one or more processors to generate the reference voltage further comprises causing the one or more processors to: determine an error based on a predetermined value and a digital representation of the reference voltage and generate the reference voltage based on the error. 21. the non-transitory computer readable medium of claim 17, wherein execution of the instructions by the one or more processors further causes the one or more processors to: control a current used to generate at least one of the first and second voltages using the reference voltage.

Results: 9

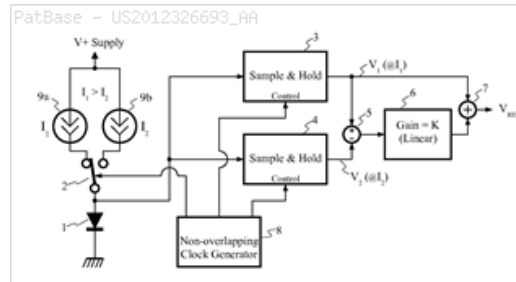
1) Family number: 51296337 (US2012326693A)

© PatBase

Forward Citations: US9897490, US9785176, US9323274, US9285822, US2015276497, US2014145701, US2014132241, US10447243,

Abstract:

A highly accurate voltage reference and temperature sensor circuit requires only several low-cost components in addition to a general-purpose microcontroller with an analog-to-digital converter. Unlike known circuits, the circuit disclosed does not rely on matching between a pair of semiconductor devices, as only a single semiconductor junction is used. All of the signal processing may be performed digitally.

**2) Family number: 52815369** (US2013015834A)

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Title: SYSTEM AND METHOD FOR POWER TRIMMING A BANDGAP CIRCUIT

Priority: US20110182056 20110713

Family:	Publication number	Publication date	Application number	Application date
	US2013015834 AA	20130117	US20110182056	20110713
	US9535446 BB	20170103	US20110182056	20110713

Probable Assignee: ANALOG DEVICES INC

Assignee(s):(std): ANALOG DEVICES INC ; GLIBBERY ADAM

Inventor(s):(std): GLIBBERY ADAM

Agent(s): SCHWEGMAN LUNDBERG AND WOESSNER PA

International class (IPC 8-9): G05F1/10 G05F3/02 G05F3/16 G05F3/20 G05F3/30 (Advanced/Invention)

CPC: G05F3/30

US class: 323/313

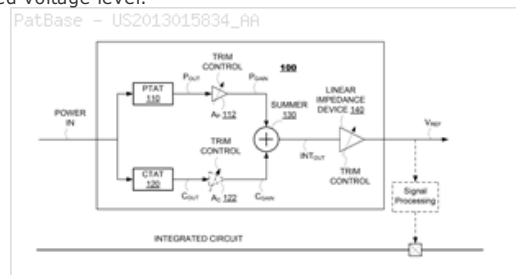
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Cited documents: US8228053 BB, US7782042 BB, US7224209 BB, US7170274 BB, US6501256 BA, US2010156519 AA, US2010123514 AA, US2002033720 AA,

Forward Citations: US9804614, US9323274, US2017255221, US2014145701, US10120399,

Abstract:

Techniques to perform bandgap circuit trimming that maximize the operating range and minimize the trimming time at which the bandgap will be accurate. A bandgap circuit output voltage may be trimmed by heating the circuit, supplying increasing input power to the bandgap circuit, and adjusting operational parameters of the bandgap circuit to generate a constant bandgap circuit output voltage. When the bandgap circuit output voltage may remain constant, a constant input power may be applied to the bandgap circuit and its output voltage may be adjusted to a predetermined voltage level.

**3) Family number: 61123379** (US2015362942A)

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Title: METHOD OF TRIMMING CURRENT SOURCE USING ON-CHIP ADC

Priority: US20140307472 20140617

Family:	Publication number	Publication date	Application number	Application date
	US2015362942 AA	20151217	US20140307472	20140617
	US9353017 BB	20160531	US20140307472	20140617

Probable Assignee: NXP SEMICONDUCTORS NV

Assignee(s):(std): VARMA VIKRAM ; FREESCALE SEMICONDUCTOR INC ; KRISHNA SIDDHARTHA GOPAL

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC ; CITIBANK NA NOTES COLLATERAL AGENT AS ; NXP USA INC ; NXP BV ; NXP F K A FREESCALE SEMICONDUCTOR INC BV ; NXP SEMICONDUCTORS NV

Inventor(s):(std): KRISHNA SIDDHARTHA GOPAL ; VARMA VIKRAM

Agent(s): CHARLES E

International class (IPC 8-9): C05F3/02 G05F3/02 H03L5/00 H03M1/12 (Advanced/Invention)

CPC: H03M1/12 C05F3/02 H03M1/48 G05F3/02 Y02P20/145 Y02A40/206

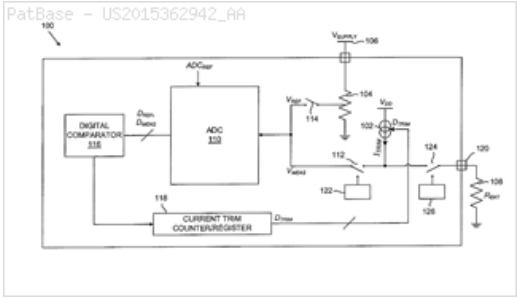
US class: 1/1 327/306

[Classification Explorer](#)

Cited documents: US8094135 BB, US7728577 BB, US7541953 BB, US7482859 BB, US7433790 BB, US6331830 BA, US5717321 A, US5410366 A, US2014253071 AA, US2014145701 AA, US2013288614 AA, US2013214946 AA, US2013107621 AA, US2012299630 AA, US2012013495 AA, US2011298642 AA, US2010102832 AA, US2009190384 AA, US2009039869 AA, US2008061217 AA, US2005068076 AA,

Forward Citations: US10305369, US10218339, EP3470860, EP3435107,

Abstract:
A method of trimming a current source in an IC includes deriving a reference voltage from an external supply, and developing a measurement voltage across an external reference resistance receiving the current to be trimmed. An on-chip ADC is used to provide corresponding digital reference and digital measurement signals. A digital comparator compares the digital signals and provides a digital trim signal, which is used to adjust the current to be trimmed until the digital measurement signal is equal to the digital reference signal within an acceptable tolerance. Gain and offset errors in the ADC cancel and do not affect the calibration of the trim operation.



4) Family number: 65759619 (US2017147019A) © PatBase

Title: CIRCUIT AND METHOD FOR GENERATING REFERENCE VOLTAGE BASED ON TEMPERATURE COEFFICIENT

Priority: KR20150163983 20151123

Family:

Publication number	Publication date	Application number	Application date
■ CN106873703 A	20170620	CN201611042252	20161121
■ KR20170059703 A	20170531	KR20150163983	20151123
■ US2017147019 AA	20170525	US20160265872	20160915
■ US9874886 BB	20180123	US20160265872	20160915

Probable Assignee: SAMSUNG ELECTRONICS CO LTD

Assignee(s):(std): SAMSUNG ELECTRONICS CO LTD

Assignee(s): SAMSUNG ELECTRONICS CO

Inventor(s):(std): KIM JONG CHEOL ; JONG CHEOL KIM

Agent(s): MUIR PATENT LAW PLLC

International class (IPC 8-9): G05F1/10 G05F1/46 G05F1/567 G05F3/22 G11C11/4074 G11C11/4099 G11C5/14 G11C7/04 (Advanced/Invention); G11C7/14 (Advanced/Non-invention)

CPC: G05F1/468 G11C11/4074 G11C11/4099 G05F3/225 G11C5/147 G11C7/04 G11C7/14 G11C29/021 G11C29/028 G11C29/56012 G11C2029/5602 G05F1/567

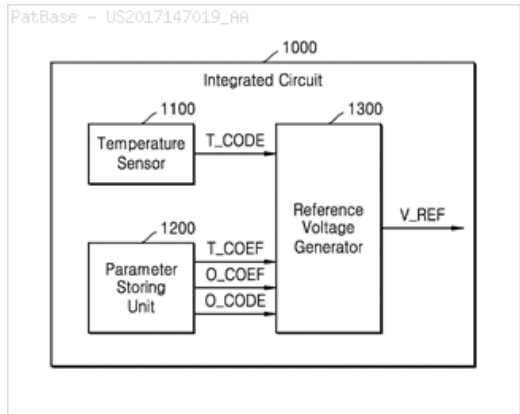
US class: 1/1 327/538

[Classification Explorer](#)

Cited documents: US9331707 BA, US8981817 BB, US8710898 BA, US8705273 BB, US8334796 BB, US7889575 BB, US7643889 BB, US7280407 BB, US7279960 BA, US2016349786 AA, US2015277456 AA, US2014320097 AA, US2014145701 AA, US2013257517 AA, US2013009622 AA, US2012249114 AA, US2012099388 AA, US2011205823 AA, US2010195412 AA, US2010060345 AA, US2010002747 AA, US2009237151 AA, KR20120043522 A, KR100851989 B1, CN1963535 A, CN1703831 A, CN104903689 A, CN103105181 A, CN101908860 A, CN101171496 A,

Forward Citations: KR101937263, FR3080236, EP3557743,

Abstract:
An integrated circuit may include a reference voltage generating circuit for generating a reference voltage. The reference voltage generating circuit may include a digital operation circuit and a digital-to-analog converter. The digital operation circuit is configured to adjust a reference voltage to temperature code relationship using a coefficient that adjusts a relative relationship between the reference voltage and the temperature code, and separate code that adjusts an absolute relationship between the reference voltage and the temperature code, wherein the temperature code reflects a temperature at the integrated circuit. The digital-to-analog converter is configured to generate the reference voltage based on an output from the digital operation circuit



5) Family number: 60542659 (US2015286239A)

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Title: SINGLE-JUNCTION VOLTAGE REFERENCE

Priority: US20140245693 20140404

Family:	Publication number	Publication date	Application number	Application date
	US2015286239 AA	20151008	US20140245693	20140404
	US10120405 BB	20181106	US20140245693	20140404

Probable Assignee: NATIONAL INSTRUMENTS CORP

Assignee(s):(std): NAT INSTR CORP ; NAT INSTRUMENTS CORP

Assignee(s): NATIONAL INSTRUMENTS CORP

Inventor(s):(std): REGIER CHRISTOPHER G

Agent(s): MEYERTONS HOOD KIVLIN KOWERT AND GOETZEL PC ; HOOD JEFFREY C

International class (IPC 8-9): G01R19/00 G05F3/16 G05F3/20 H01L29/66 (Advanced/Invention)

CPC: G05F3/16

US class: 323/313 324/76.11

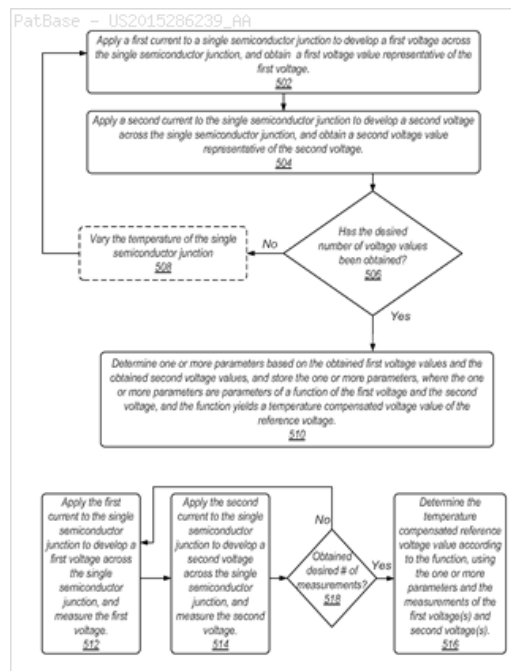
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Cited documents: US9726696 BB, US9329614 BA, US9218016 BB, US8760180 BA, US8433265 BB, US8350555 BB, US8094033 BB, US7564298 BB, US7164308 BB, US7122997 BA, US7116588 BB, US7108420 BA, US6987416 BB, US6650170 BA, US6512412 BB, US6483372 BA, US6342780 BA, US6222470 BA, US6184661 BA, US6111397 A, US5973550 A, US5838192 A, US5640085 A, US5631551 A, US5434533 A, US5053640 A, US4769589 A, US4668903 A, US4562400 A, US2015214903 AA, US2014168041 AA, US2014145701 AA, US2014084899 AA, US2014009221 AA, US2012250721 AA, US2011080153 AA, US2011068854 AA, US2009146748 AA, US2009146719 AA, US2006202772 AA, US2003025551 AA,

Forward Citations: US10274440,

Abstract:

A single semiconductor-based junction may be used to create a voltage reference, and temperature compensate the voltage reference, by time-multiplexing the voltage reference between different current drive levels. That is, the value of the current driven through the single junction may be repeatedly varied in a recurring manner. In case the junction is a zener diode, the current may be repeatedly switched between forward and reverse directions. As long as the temperature coefficients (in ppm/degrees centigrade) of the different voltages developed responsive to the different currents across the junction are different, a weighting of the different voltage values yield a zero temperature coefficient voltage reference value. To implement a bandgap reference, a single diode-connected bipolar junction transistor may alternately be forward-biased using a first current and at least a second current. A weighting of the (at least) two resulting V_{be} (base-emitter voltage) drops may yield a zero temperature coefficient bandgap voltage.



6) Family number: 56544812 (US2014145701A)

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Title: SELF-CALIBRATING DIGITAL BANDGAP VOLTAGE AND CURRENT REFERENCE

Priority: US20120687182 20121128

Family:

Publication number	Publication date	Application number	Application date
US2014145701 AA	20140529	US20120687182	20121128
US9323274 BB	20160426	US20120687182	20121128

Probable Assignee: ATI TECHNOLOGIES ULC

Assignee(s):(std): ATI TECHNOLOGIES ULC

Inventor(s):(std): CHEKMAZOV FILIPP ; DRAPKIN OLEG ; TEMKINE GRIGORI

Agent(s): VOLPE AND KOENIG PC

International class (IPC 8-9): G05F3/02 G05F3/08 G05F3/30 (Advanced/Invention)

CPC: G05F3/30 G05F3/10 G05F3/08

US class: 1/1 323/314

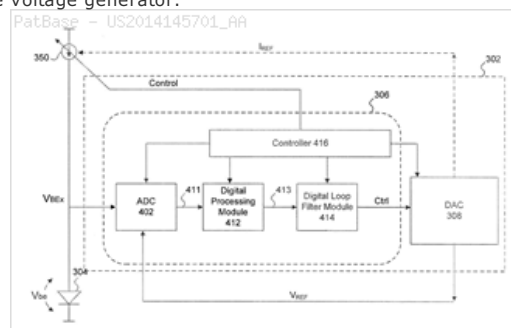
[Classification Explorer](#)

Cited documents: US7543253 BB, US6329804 BA, US2013015834 AA, US2012326693 AA, US2008122669 AA,

Forward Citations: US9874886, US9353017, US2015362942, US2015286239, US10120405,

Abstract:

A reference voltage generator is provided. In an example, the reference voltage generator includes a temperature-dependent device, a processing module configured to process a digital representations of first and second voltages derived from the temperature-dependent device and a reference voltage to determine a value, and a digital to analog converter (DAC) configured to generate a reference voltage based on the value. The first voltage is proportional to absolute temperature (PTAT) and the second voltage is complementary to absolute temperature (CTAT) and the reference voltage is substantially independent of absolute temperature in an operating temperature range of the reference voltage generator.



7) Family number: 41847863 (US2008122669A)

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Title: DIGITAL BANDGAP REFERENCE AND METHOD FOR PRODUCING REFERENCE SIGNAL

Priority: US20060592411 20061102

Family:

Publication number	Publication date	Application number	Application date
US2008122669 AA	20080529	US20060592411	20061102

Probable Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD

Assignee(s):(std): DEKEN RICHARD ; FREESCALE SEMICONDUCTOR INC

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC ; NORTH STAR INNOVATIONS INC ; NXP BV ; NXP F K A
FREESCALE SEMICONDUCTOR INC BV ; TAIWAN SEMICONDUCTOR MFG CO LTD ; SHENZHEN
XINGUODU TECHNOLOGY CO LTD ; CITIBANK NA ; CITIBANK NA COLLATERAL AGENT AS ; CITIBANK
NA NOTES COLLATERAL AGENT AS

Inventor(s):(std): DEKEN RICHARD

Agent(s): INGRASSIA FISHER AND LORENZ PC

International class (IPC 8-9): G01R31/00 H03M1/00 (Advanced/Invention);
G01R31/00 H03M1/00 (Core/Invention)

CPC: G05F3/30

European class: G05F3/30

US class: 323/314 324/760.01 324/770 341/124

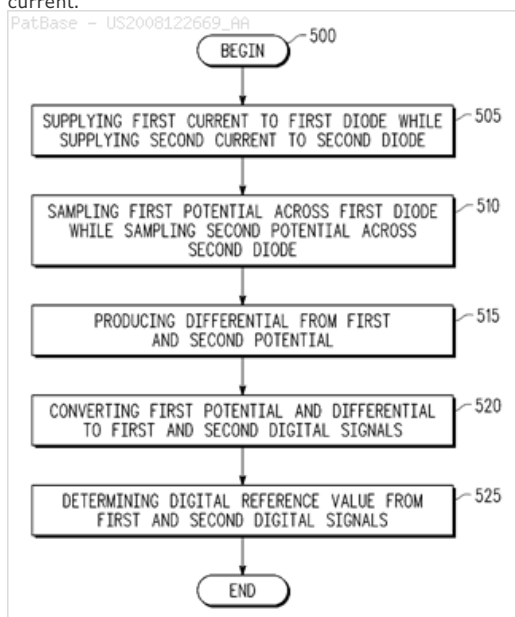
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Cited documents: US7225099 BA, US6590372 BA, US6075407 A, US5867054 A, US2008095213 AA, US2006093016 AA, US2004155840 AA, US2004085086 AA, US2003071683 AA,

Forward Citations: US9804036, US9323274, US8854120, US8783949, US8446140, US8330445, US8278905, US8167485, US2018100774, US2015369674, US2014145701, US2011127988, US2011127987, US2011116527, US2011084681, US2010002748, US10295416, CN107917764,

Abstract:

A system and method (400) for producing a reference signal is provided. The method includes supplying (405) a first current to a diode, sampling (410) a first voltage across the diode, supplying (405) a second current to the diode, sampling (410) a second voltage across the diode, converting (415) the first voltage and the second voltage to a first digital value and a second digital value, and determining (420) a digital reference value from the first digital value and the second digital value. The first voltage is based on the first current, and the second voltage is based on the second current.



8) Family number: 15964985 (US6329804B)

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Title: Slope and level trim DAC for voltage reference

Priority: US19990416896 19991013

Family:	Publication number	Publication date	Application number	Application date
	US6329804 BA	20011211	US19990416896	19991013

Probable Assignee: NATIONAL SEMICONDUCTOR CORP

Assignee(s):(std): NAT SEMICONDUCTOR CORP

Assignee(s): NATIONAL SEMICONDUCTOR CORP

Inventor(s):(std): MERCER MARK J

International class (IPC 8-9): G05F3/30 (Advanced/Invention);
G05F3/08 (Core/Invention)

International class (IPC 1-7): G05F3/16 G05F3/20

CPC: G05F3/30

European class: G05F3/30

US class: 323/314 323/315

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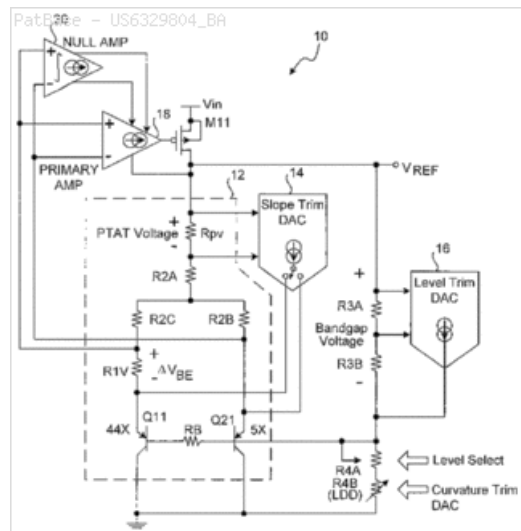
Cited documents: US5867015 A, US5814979 A, US5736843 A, US5705919 A, US5686821 A, US5677558 A, US5675241 A, US5672959 A, US5631598 A, US5629609 A, US5563504 A, US5519308 A, US5510697 A, US5485109 A, US5410241 A, US5391980 A, US5352973 A, US5334928 A, US5325045 A, US5291122 A, US5274323 A, US5191278 A, US5168209 A, US5126653 A, US4928056 A, US4926109 A, US4906913 A, US4902959 A, US4808908 A, US4803612 A, US4792747 A, US4613809 A, US4603291 A, US4543522 A, US4250445 A, US4190805 A, US3887863 A,

Forward Citations: WO06102324, WO06102324, WO06030375, WO05033820, US9991784, US9966048, US9703306,

US9671800, US9568928, US9377805, US9354644, US9323274, US9141124, US8941370, US8791683, US8421659, US8421434, US8294447, US8125366, US8102201, US7903014, US7902912, US7880533, US7750728, US7724075, US7714563, US7675792, US7612606, US7605578, US7598799, US7576598, US7543253, US7433790, US7230473, US7164260, US7019585, US6933770, US6867573, US6816099, US2016078957, US2015102856, US2015084686, US2014145701, US2012001784, US2011234197, US2010102789, US2010085029, US2009243713, US2009243708, US2009160538, US2009160537, US2009080267, US2008265860, US2008224759, US2008136381, US2008074172, US2006276986, US2006208790, US2006108994, US2005073290, US2004183706, US10310528, US10013013, TWI581084, TWI571723, KR100931770, JP2009501363, EP2487797, DE102016220715, DE102016220715, DE102006034695, DE102006034695,

Abstract:

A method and apparatus for trimming the level and slope in a voltage reference using current-switching DACs to inject small correction currents into or draw currents from the voltage reference circuit. Each DAC is controlled via a programmable non-volatile memory, which can be programmed after final packaging. Thus, the present technique enables trimming the voltage reference circuit after the circuit has been packaged. For the slope trim, the current is injected into or drawn from one side or the other of the band-gap core cell. The level trim DAC sources a correction current into or sinks a correction current from the resistor chain that sets the voltage level at the base of the transistors in the band-gap core. The level and slope trim DACs generate currents that are precise multiples of the currents through the resistors being trimmed. Thus the corrections are invariant with process and temperature, the necessary trim range is minimized, and the shape of the remaining error (curvature) is not altered. This current replication technique has the same effect as an ideal trim, i.e. produces the same result as changing the values of the resistors around which the trim circuits are placed.



9) Family number: 31797997 (US2005073290A)

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Title: METHOD AND APPARATUS FOR COMPENSATING FOR TEMPERATURE DRIFT IN SEMICONDUCTOR PROCESSES AND CIRCUITRY

Priority: US20030680265 20031007 WO2004IE00132 20040928

Family:	Publication number	Publication date	Application number	Application date
	CN1864116 A	20061115	CN200480029279	20040928
	CN1864116 B	20101103	CN200480029279	20040928
	JP2007514988 T2	20070607	JP20060530992T	20040928
	JP4523942 B2	20100811	JP20060530992T	20040928
	TW200519558 A	20050616	TW20040129420	20040929
	TWI341448 B	20110501	TW20040129420	20040929
	US2005073290 AA	20050407	US20030680265	20031007
	US7543253 BB	20090602	US20030680265	20031007
	WO05033820 A1	20050414	WO2004IE00132	20040928

Probable Assignee: ANALOG DEVICES INC

Assignee(s):(std): ANALOG DEVICES INC ; MARINCA STEFAN ; O DWYER THOMAS G

Inventor(s):(std): MARINCA STEFAN O DWYER THOMAS ; MARINCA STEFAN ; O DWYER THOMAS G ; STEFAN MARINCA

Inventor(s): MARINCA STEFAN O DWYER THOMAS G ; O'DWYER THOMAS G ; O DWYER THOMAS

Agent(s): WOLF GREENFIELD AND SACKS PC FEDERAL RESERVE PLAZA; WOLF GREENFIELD AND SACKS PC

Designated states: AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MC MD MG MK ML MN MR MW MX MZ NA NE NI NL NO NZ OM PG PH PL PT RO RU SC SD SE SG SI SK SL SN SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

International class (IPC 8-9): G05F3/16 G05F3/20 G05F3/22 G05F3/24 G05F3/30 G06F17/50 H01L21/822 H01L27/04 H03F1/30 H03F3/45 H03K17/78 (Advanced/Invention); G05F3/08 G06F17/50 H01L21/70 H01L27/04 H03F1/30 H03F3/45 H03K17/78 (Core/Invention)

International class (IPC 1-7): G05F3/16 G05F3/30 G06F17/50

CPC: H03F1/30 H03F3/45179 H03F2200/447

European class: H03F1/30 H03F3/45S1B T03F200/447

US class: 323/313 323/313P 323/315 323/907 323/907S 327/512 327/540 716/1 716/3 716/4

[Classification Explorer](#)

Cited documents: US7482798 BB, US7472030 BB, US7411380 BB, US7372244 BB, US7301321 BA, US7260377 BB, US7248098 BA, US7236047 BB, US7224210 BB, US7211993 BB, US7199646 BA, US7193454 BA, US7173407 BB, US7170336 BB, US7112948 BB, US7091761 BB, US7088085 BB, US7068100 BB,

US7057444 BB, US7012416 BB, US6992533 BB, US6987416 BB, US6958643 BB, US6930538 BB, US6919753 BB, US6894544 BB, US6891358 BB, US6885178 BB, US6853238 BA, US6836160 BB, US6828847 BA, US6798286 BB, US6791307 BB, US6750641 BA, US6690228 BA, US6664847 BA, US6661713 BA, US6642699 BA, US6614209 BA, US6590372 BA, US6531857 BB, US6529066 BA, US6501256 BA, US6489835 BA, US6489787 BA, US6483372 BA, US6462625 BB, US6426669 BA, US6373330 BA, US6356161 BA, US6356161 B1, US6329868 BA, US6329804 BA, US6329804 B1, US6255807 BA, US6225796 BA, US6218822 BA, US6157245 A, US6075354 A, US6075354, US6002293 A, US5982201 A, US5952873 A, US5933045 A, US5828329 A, US5821807 A, US5767664 A, US5646518 A, US5563504 A, US5512817 A, US5424628 A, US5352973 A, US5325045 A, US5229711 A, US5119015 A, US5053640 A, US4939442 A, US4808908 A, US4714872 A, US4603291 A, US4475103 A, US4399398 A, US2008265860 AA, US2008224759 AA, US2008074172 AA, US2008018319 AA, US2006038608 AA, US2006017457 AA, US2005237045 AA, US2005194957 AA, US2003234638 AA, KR115143, KR0115143 B1, JP9160663 A2, JP8030345 A2, JP58080716 A2, JP55056212 A2, JP4167010 A2, JP4167010, JP2006519433 T2, JP2006512682 T2, JP2003529227 T2, JP2002513179 T2, JP2000330658 A2, JP2000201073 A2, JP2000089843 A2, JP11298299, JP11121694, EP1359490 A3, EP1359490 A2, EP1337037 A1, EP0510530 A2, EP0510530 A2,

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WO13137867, WO13126414, US9859848, US9703306, US9601209, US9411354, US9354644, US9323274, US9231519, US8710888, US8624661, US8358119, US8102201, US7902912, US7880533, US7750728, US7714563, US7710190, US7696909, US7612606, US7605578, US7598799, US7576598, US7453252, US7268711, US7113025, US7113025, US2014145701, US2013241524, US2013009622, US2011043185, US2010001711, US2009243713, US2009243711, US2009243708, US2009160538, US2009160537, US2008265860, US2008224759, US2008129371, US2008074172, US2008061864, US2008036524, US2007222651, US2007001748, US2005231270, US10191507, TWI549480, JP4837111, JP2010231774, CN105318980, CN105318980, CN104145227, CN104145227,

Abstract:

The present invention provides a method and apparatus for compensating for temperature effects in the operation of semiconductor processes circuitry, such as reference circuits. The method operates on the realisation that the second order effects such as "curvature" in the reference voltage variation over a temperature range is removed. The reference voltage variation over a temperature range can be represented as a straight line. This method provides for the trimming of the absolute voltage by scaling the reference voltage at a first temperature to the desired value by a temperature independent voltage. Then, at a second temperature, the output voltage slope is corrected by adding or subtracting a voltage which is always zero at the first temperature.

