

1) Family number: 4623135 (US5021743A)

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Title:

Priority:

Family:

Probable Assignee:

Assignee(s):(std):

Assignee(s):

Inventor(s):(std):

International class (IPC 8-9):

International class (IPC 1-7):

CPC:

European class:

US class:

[Classification Explorer](#)

Cited documents:

Forward Citations:

Biasing networks for matrix amplifiers

US19890443985 19891130

Publication number

Publication date

Application number

Application date

US5021743 A

19910604

US19890443985

19891130

RAYTHEON CO

RAYTHEON CO

RAYTHEON COMPANY

CHU SHIOU L L ; TAJIMA YUSUKE ; SCHINDLER MANFRED J

H03F3/60 (Advanced/Invention);

H03F3/60 (Core/Invention)

H03F3/60

H03F3/607

H03F3/60D1

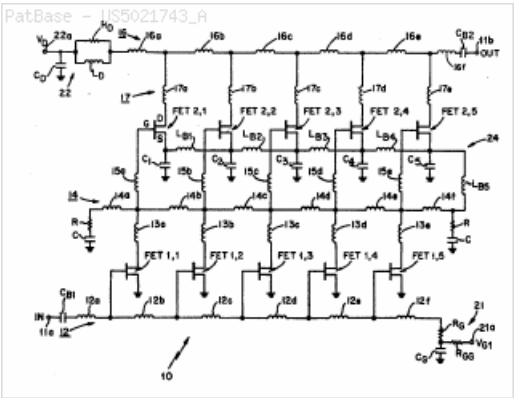
330/277 330/286 330/54

[Classification Explorer](#)

US4752746 A, US4486719 A,

US9202660, US9024703, US8823455, US8669812, US8576009, US8179045, US7782140, US7656236, US7579913, US6930557, US6861903, US6674329, US6377125, US6215360, US5880640, US5551075, US5548248, US5485118, US5349306, US5319318, US2014035652, US2013063213, US2012268213, US2009212868, US2009102574, US2009009253, US2004085133, US10355652, AU2008229976,

Abstract:
A radio frequency matrix amplifier includes an input propagation network for successively connecting input electrodes of a first plurality of transistors. Output electrodes are successively coupled by an intermediate propagation network. The amplifier also includes a second plurality of transistors, having input electrodes successively coupled by the intermediate propagation network and output electrodes successively coupled by an output propagation network. A bias circuit for the amplifier includes an inductor connected between a last one of the second plurality of transistors and the intermediate propagation network and a plurality of capacitors disposed to connect reference electrodes of the second plurality of transistors to a reference potential. With this arrangement stages are connected in series for D.C. potentials and in cascade for r.f. potentials. In a preferred embodiment, capacitors are disposed between the input electrodes of each of the second plurality of transistors and the output electrodes of each of the first plurality of transistors to D.C. isolate the stages, and a voltage divider is disposed between the drain bias terminal and a reference potential for balancing input voltages at each of the inputs of the first plurality of transistors substantially independently of current through the output electrodes of each of the plurality of transistors.



2) Family number: 64747159 (US2017026961A)

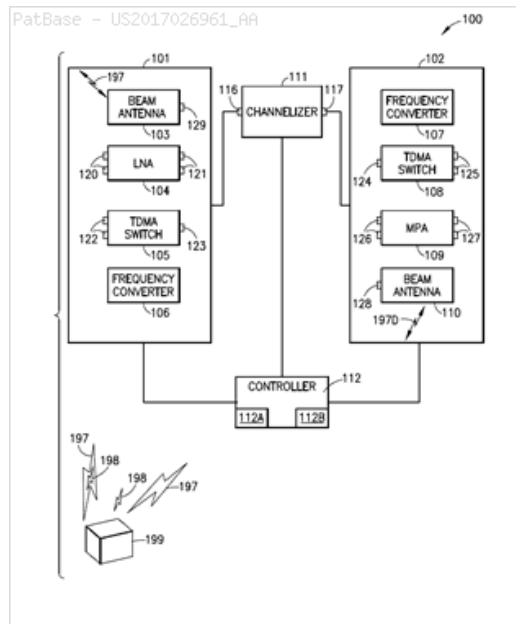
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Title:	NOVEL FDMA/TDMA ARCHITECTURE USING CHANNELIZER AND MATRIX POWER AMPLIFIER					
Priority:	US20150803269	20150720	RU20160117585	20160505	EP20160173717	20160609
	JP20160140290	20160715				
Family:	Publication number	Publication date	Application number	Application date		
	CA2930419 AA	20170120	CA20162930419	20160518		
	CA2930419 C	20191119	CA20162930419	20160518		
	CN106385275 A	20170208	CN201610534458	20160707		
	DE602016002516 D1	20180517	DE201660002516T	20160609		

EP3121975 A1	20170125	EP20160173717	20160609
EP3121975 B1	20180418	EP20160173717	20160609
ES2676947 T3	20180726	ES20160173717T	20160609
JP2017108375 A2	20170615	JP20160140290	20160715
RU2016117585 A	20171113	RU20160117585	20160505
RU2016117585 A3	20191001	RU20160117585	20160505
US2017026961 AA	20170126	US20150803269	20150720
US9801176 BB	20171024	US20150803269	20150720

Probable Assignee: BOEING CO
Assignee(s):(std): BOEING CO
Assignee(s): BOEING CO CHICAGO ; HAHN CARL J III ; ROSENHECK LEONARD
Inventor(s):(std): ROSENHECK LEONARD ; HAHN III CARL J ; CARL J HAHN III ; LEONARD ROSENHECK ; HAHN CARL J ; HAHN CARL J III
Inventor(s): ROSENHECK LEONARD CHICAGO ; HAHN III CARL J CHICAGO
Agent(s): SIM AND MCBURNEY; MARKS AND CLERK; LAND ADDICK ADRIANUS GOSLING; CARVAJAL Y ISABEL; SONODA AND KOBAYASHI INTELLECTUAL PROPERTY LAW; PERMAN AND GREEN LLP
Designated states: AL AT BA BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT RO RS SE SI SK SM TR
International class (IPC 8-9): H04B7/00 H04B7/08 H04B7/10 H04B7/185 H04B7/204 H04B7/26 H04J1/00 H04J3/00 H04J4/00 H04L12/931 H04L5/20 H04W72/04 (Advanced/Invention); H01Q21/00 (Advanced/Non-invention)
CPC: H04B7/0408 H04B7/0802 H04J4/00 H04L49/10 H04B7/18515 H04B7/2041 H04B7/2046 H04B7/2615 H04W72/0446
US class: 1/1 370/337
JP class F-Term: 5J500 5J500/AA21 5J500/AA41 5J500/AA53 5J500/AC36 5J500/AF15 5J500/AM10 5J500/CK06 5J500/CK07 5K072 5K072/CC13 5K072/CC15 5K072/CC32 5K072/EE04 5K072/GG14 5K159 5K159/CC04 5K159/FF04
JP class F-Index: H03F3/68/B H03F3/68/220 H04B7/06/950 H04B7/08/800 H04B7/10/A H04B7/185
[Classification Explorer](#)
Cited documents: US7542716 BB, US6434361 BA, US4931802 A, US4858225 A, US4858225 A, US2014092804 AA, EP1058410 A2, EP1058410 A2,
Forward Citations: US9848370, US10454567, US10355652,

Abstract:
A communication system including at least one first TDMA high speed switch having a first switch output, a FDMA channelizer, configured to receive an input RF signal from the at least one first TDMA high speed switch, at least one matrix power amplifier having at least one input and at least one output, and at least one second TDMA high speed switch having a second switch input coupled to a respective one of at least one channelizer output and at least one second switch output coupled to a corresponding input of the at least one matrix power amplifier, the at least one second TDMA high speed switch being configured to receive an output RF signal from the FDMA channelizer and transmit the output RF signal to a selected input of the at least one matrix power amplifier, wherein each predetermined output is coupled to a corresponding antenna beam.



3) Family number: 10242178 (US4752746A)

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Title: Wideband microwave matrix amplifier
Priority: US19870015908 19870218

Family:	Publication number	Publication date	Application number	Application date
	US4752746 A	19880621	US19870015908	19870218

Probable Assignee: WATKINS JOHNSON CO

Assignee(s):(std): WATKINS JOHNSON CO

Assignee(s): WATKINS JOHNSON COMPANY ; FIRST UNION COMMERCIAL CORP ; M A COM TECH INC ; STELLEX MICROWAVE SYSTEMS INC ; TYCO ELECTRONICS LOGISTICS AG

Inventor(s):(std): NICLAS KARL B

International class (IPC 8-9): H03F3/60 (Advanced/Invention); H03F3/60 (Core/Invention)

International class (IPC 1-7): H03F3/60

CPC: H03F3/607

European class: H03F3/60D1

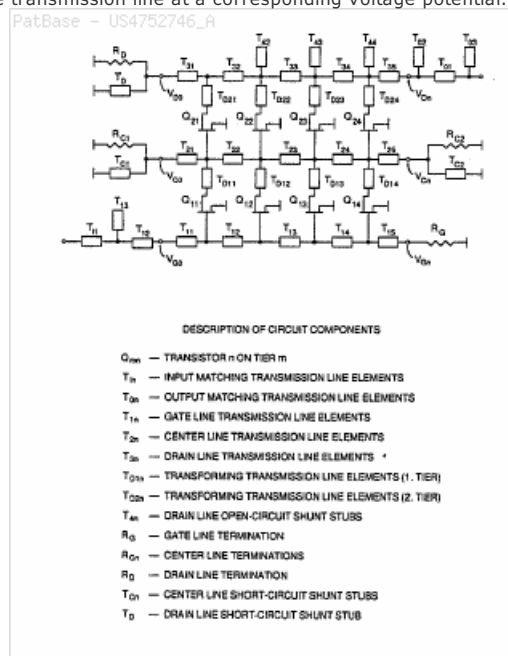
US class: 330/277 330/286 330/54

[Classification Explorer](#)

Cited documents: US4291286 A,

Forward Citations: WO17133776, US8823455, US8665022, US8451059, US7724091, US7142052, US5559472, US5485118, US5136720, US5105166, US5021743, US5012203, US2018302040, US2013063213, US2009102574, US2004130390, US10355652, JP5315851, JP3188705, EP2051373, EP0430509, EP0430509, AU2008229976,

Abstract:
A microwave amplifier that both multiplicatively and additively amplifies microwave frequency signals. The amplifier, herein coined a matrix amplifier, is a distributed amplifier with two or more tiers (rows) of transistors. Each tier has a plurality of transistors which additively amplify the signal entering that row of the amplifier, and each row multiplicatively amplifies the output of the previous row. The gates of the transistors in each row are sequentially coupled to an input transmission line having a series of transmission elements. The outputs of all the transistors from each row are sequentially coupled to the input transmission line of the next tier, except that the outputs of the last tier are coupled to an output transmission line for transmitting the output of the amplifier to an output node. Furthermore, each transmission lines has (1) at least one line termination at one of its ends for absorbing signals incident on that end of the transmission line, and (2) biasing means for d.c. biasing the transmission line at a corresponding voltage potential.



4) Family number: 66582346 (US2018097484A)

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Title: MATRIX POWER AMPLIFIER

Priority: WO2016EP52386 20160204 US20170809502 20171110 US20190428918 20190531

Family:

Publication number	Publication date	Application number	Application date
BR112018015791 A2	20181226	BR20181115791	20160204
CA3013235 AA	20180731	CA20163013235	20160204
CN109075750 A	20181221	CN201680084383	20160204
CO20180009289 A2	20181010	CO20180009289	20180904
EP3411950 A1	20181212	EP20160702935	20160204
IL260902 A0	20180920	IL20160260902	20160204
JP2019508955 T2	20190328	JP20180540132T	20160204
KR20180109990 A	20181008	KR20187025157	20160204
MX2018009562 A1	20190328	MX20180009562	20160204
US2018097484 AA	20180405	US20170809502	20171110
US2019288651 AA	20190919	US20190428918	20190531
US10355652 BB	20190716	US20170809502	20171110
WO17133776 A1	20170810	WO2016EP52386	20160204

Probable Assignee: FRAUNHOFER GES

Assignee(s):(std): FRAUNHOFER GES ZUR FORDERUNG DER ANGEWANDTEN FORSCHUNG E V ; FRAUNHOFER GES FORSCHUNG ; FRAUNHOFER GES ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG E V

Assignee(s): FRAUNHOFER GES ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG EV ; FRAUNHOFER GES ;
FRAUNHOFER GES ZUR FORDERUNG DER ANGEWANDTEN FORSCHUNG EV ; VAN RAA Y DR ING FRIEDBERT
; VAN RAA Y FRIEDBERT ; VAN RAA Y ING FRIEDBERT

Inventor(s):(std): VAN RAA Y DR ING FRIEDBERT ; VAN RAA Y FRIEDBERT ; DR ING FRIEDBERT VAN RAA Y ; FRIEDBERT VAN
RAA Y ; VAN RAA Y ING FRIEDBERT

Agent(s): BERESKIN AND PARR LLP SENCRL SRL; CONROY JOHN; ABE MASAHIRO; FISH AND RICHARDSON PC;
CONROY PHD JOHN F

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU
CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN
IR IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW
MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM
SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

International class (IPC 8-9): H03F H03F1/02 H03F1/06 H03F1/52 H03F1/56 H03F3/195 H03F3/21 H03F3/213 H03F3/217 H03F3/24
H03F3/26 H03F3/42 H03F3/45 H03F3/60 H03F3/68 (Advanced/Invention);
H01Q23/00 (Advanced/Non-invention)

International class (IPC 1-7): H03F1/02 H03F1/52 H03F1/56 H03F3/195 H03F3/24 H03F3/42 H03F3/45 H03F3/60

CPC: H03F1/523 H03F1/565 H03F3/195 H03F3/245 H03F3/423 H03F3/45183 H03F3/45475 H03F3/604 H03F3/607
H03F2200/06 H03F2200/108 H03F2200/135 H03F2200/181 H03F2200/222 H03F2200/255 H03F2200/297
H03F2200/301 H03F2200/315 H03F2200/318 H03F2200/387 H03F2200/42 H03F2200/423 H03F2200/451
H03F2200/48 H03F2200/498 H03F2200/75 H03F2203/45138 H03F2203/45148 H03F2203/45151
H03F2203/45156 H03F2203/45166 H03F2203/45202 H03F2203/45208 H03F2203/45224 H03F2203/45258
H03F2203/45338 H03F2203/45458 H03F2203/45488 H03F2203/45496 H03F2203/45528 H03F2203/45544
H03F2203/45594 H03F2203/45631 H03F2203/45696 H03F2203/45702 H03F3/211 H01Q23/00 H03F1/56

US class: 1/1 330/295

JP class F-Term: 5J067 5J067/AA04 5J067/AA15 5J067/AA16 5J067/AA23 5J067/AA35 5J067/AA41 5J067/CA33 5J067/CA36
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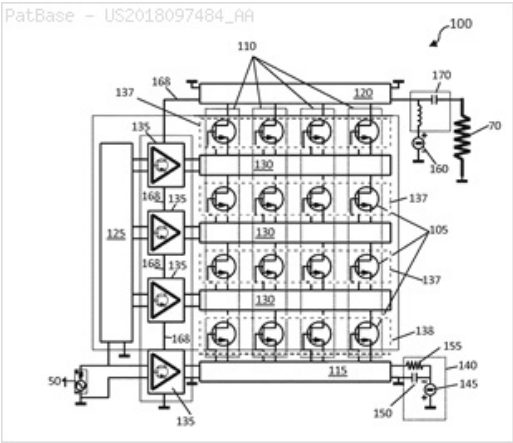
JP class F-Index: H03F3/213 H03F3/217/130 H03F3/24 H03F3/26 H03F3/45 H03F3/60 H03F3/68/210 H03F3/68/220

[Classification Explorer](#)

Cited documents: WOWO2017133776, WO17133776 A1, US9054676 BB, US8823455 BB, US8558619 BB, US7956840 BB,
US7551036 BB, US7511575 BB, US6864750 BB, US6724252 BB, US6137367 A, US5867061 A, US5485118
A, US5386130 A, US5021743 A, US4752746 A, US4498106 A, US4079336 A, US2017026961 AA,
US2015097746 AA, US2014266460 AA, US2013307626 AA, US2013049867 AA, US2009018969 AA,
US2008265997, JP7131264, JP54075978, JP3188705, JP2015170957, JP2014220770, JP2003516690 T2,
JP2002314353, FR2727003 A1, DE69318253 T2,

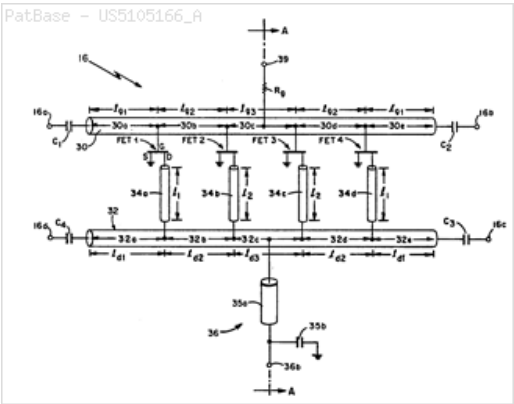
Forward Citations: US10355652,

Abstract:
A power amplifier includes a two-dimensional matrix of NxM active cells formed by stacking main terminals of multiple active cells in series. The stacks are coupled in parallel to form the two-dimensional matrix. The power amplifier includes a driver structure to coordinate the driving of the active cells so that the effective output power of the two-dimensional matrix is approximately NxM the output power of each of the active cells.



Assignee(s):(std): RAYTHEON CO
Assignee(s): RAYTHEON COMPANY
Inventor(s):(std): TSUKII TOSHIKAZU ; HOUNG S GENE ; SCHINDLER MANFRED J ; ESU JIIN HOUN ; TOSHIKAZU TSUKII ; MANFURETSUDO JIEI SHIYUINDORAA
Designated states: DE FR GB IT
International class (IPC 8-9): G01S7/28 H03F3/60 H03F3/62 (Advanced/Invention); G01S7/28 H03F3/60 H03F3/62 (Core/Invention)
International class (IPC 1-7): G01S7/28 H03F3/16 H03F3/60 H03F3/62
CPC: H03F3/607 H03F3/62 H03F2200/372
European class: H03F3/60D1 H03F3/62 T03F200/372
US class: 330/277 330/286
JP class F-Term: 5J067 5J067/AA04 5J067/AA22 5J067/AA35 5J067/AA41 5J067/AA55 5J067/CA35 5J067/CA41 5J067/CA62 5J067/CA64 5J067/CA92 5J067/FA07 5J067/FA10 5J067/FA12 5J067/FA15 5J067/FA19 5J067/HA09 5J067/HA25 5J067/HA29 5J067/HA32 5J067/HA33 5J067/HA38 5J067/KA16 5J067/KA42 5J067/KA47 5J067/KA68 5J067/KS01 5J067/KS03 5J067/KS05 5J067/KS15 5J067/KS18 5J067/KS34 5J067/LS01 5J067/LS12 5J067/MA08 5J067/QS04 5J067/SA00 5J067/SA13 5J067/SA16 5J067/TA01 5J069 5J069/AA04 5J069/AA35 5J069/AA55 5J069/BC01 5J069/CA36 5J069/CA47 5J069/FA14 5J069/FA15 5J069/HA09 5J069/HA25 5J069/HA29 5J069/SA13 5J069/TA01 5J070 5J070/AB01 5J070/AD01 5J070/AD10 5J070/AH40 5J070/AH50 5J070/AK21 5J070/AK27 5J070/AK28 5J070/AK40 5J070/AL01 5J070/BH20 5J500 5J500/AA04 5J500/AA35 5J500/AA55 5J500/AC36 5J500/AC47 5J500/AF14 5J500/AF15 5J500/AH09 5J500/AH25 5J500/AH29 5J500/AS13 5J500/AT01 5J500/CB01
JP class F-Index: G01S7/28/Z G01S7/28/220 H03F3/60 H03F3/62
[Classification Explorer](#)
Cited documents: US4847568 A, US4845490 A, US4752746 A, US3612780 A, EP0285345 A2, EP0216432 A2,
Forward Citations: WO9514331, WO17055988, WO16138406, WO07093096, WO04047288, WO03005573, US9948254, US9858532, US9843312, US9780943, US9559643, US9194970, US9182617, US8868006, US8208869, US7315206, US7239852, US6686875, US5821813, US2018040935, US2015116036, US2013162257, US2011234321, US2009247074, US2005026571, US2001046840, US10468740, US10461385, US10424712, US10424711, US10404214, TWI618348, JP6318548, JP5835020, JP4290653, JP4269629, JP4206589, JP2019508955, JP2015088840, JP2013183450, JP2009077428, JP2006056879, JP2004135185, JP2002033627, JP2001160723, GB2558831, EP1505726, EP1274165,

Abstract:
A transceiver module includes a bi-directional amplifier having a pair of symmetric signal paths for amplification of both transmit and receive signals is described. The amplifier is a bi-directional amplifier and includes a pair of symmetric signal paths. The amplifier is disposed between a pair of r.f. switches to provide a pair of signal paths between two terminals of the module. A phase shifter is coupled between one of the terminals of the module and one of the r.f. switches, wherein the second terminal of the module is coupled directly to the other one of the pair of switches.



6) Family number: 12348520 (US5485118A) © PatBase

Title: Non-uniformly distributed power amplifier
Priority: US19940253809 19940603
Family:

Publication number	Publication date	Application number	Application date
US5485118 A	19960116	US19940253809	19940603

Probable Assignee: MASSACHUSETTS INST
Assignee(s):(std): MASSACHUSETTS INST TECHNOLOGY
Assignee(s): MASSACHUSETTS INSTITUTE OF TECHNOLOGY ; AIR FORCE UNITED STATES ; MASSACHUSETTS INST
Inventor(s):(std): CHICK RICHARD W
International class (IPC 8-9): H03F3/60 (Advanced/Invention); H03F3/60 (Core/Invention)
International class (IPC 1-7): H03F3/60
CPC: H03F3/607
European class: H03F3/60D1
US class: 330/277 330/286 330/295 330/52 330/54

Cited documents:

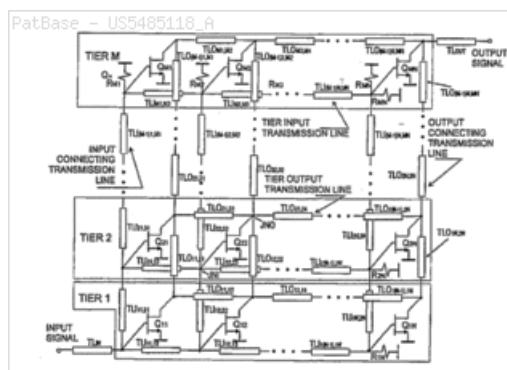
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Forward Citations:

WO02078180, US9917080, US9843262, US9640632, US9564497, US9536803, US9455327, US9425752, US9325281, US9202874, US9147632, US9142620, US9136341, US9129802, US9124221, US9093420, US9070761, US8988097, US8823455, US8766427, US8669812, US8665022, US8576009, US8451059, US8076975, US8058930, US8035449, US7924097, US7724091, US7671702, US7271657, US7142052, US6754692, US6590448, US6539484, US6453444, US6275111, US6008694, US2017110968, US2014320211, US2010300899, US2009309659, US2009219087, US2009102574, US2009096554, US2005248407, US2004130390, US2004080370, US2002091950, US10355652, US10164579, US10122325, US10069464, US10062684, KR100976638, JP4238034, JP2004532549, FR2747523, EP2475007, EP2051373, EP1741181, EP0801467, CN105608276, CN105608276, CN102593120, CN102593120, AU2008229976,

Abstract:

An amplifier extracts the maximum power from a plurality of identical three-terminal electronic amplifying devices, herein coined "cells," by additively combining their power contributions. The amplifier, herein coined a "non-uniformly distributed power amplifier," is a distributed amplifying circuit in which the transmission line impedances between adjacent electronic amplifying devices varies throughout the distribution in a prescribed manner so as to optimize the power output and/or amplifying efficiency of the distribution. The distribution may be constructed in one, two, or three dimensions but will always produce an overall mid-band power gain which is equivalent to the sum of the gains of the devices contained in the distribution of an overall power output which is equal to the number of devices times the power contribution of a single contributing device. Regardless of the amplifier's dimensions, microwave input power will be disbursed throughout the amplifier by an array of transmission lines of varying characteristic impedance which interconnects the input terminals of nearest neighbor cells. A similar array of transmission lines having a mirror-image topology interconnect the outputs of nearest neighbor cells to produce an output port. The output end (or outbound edges of a rectangular distribution, or outbound surfaces of a three-dimensional array) of the input array terminated in a resistor to absorb incident signals. However the output transmission line array requires no resistive terminations other than the intended load which will be attached to the output port.

**7) Family number: 24142521** (JP2002314353A)

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Title: SEMICONDUCTOR AMPLIFIER CIRCUIT**Priority:** JP20010112906 20010411**Family:**

Publication number	Publication date	Application number	Application date
JP2002314353 A2	20021025	JP20010112906	20010411
JP3856658 B2	20061213	JP20010112906	20010411

Probable Assignee: OKI ELECTRIC IND CO LTD**Assignee(s):(std):** OKI ELECTRIC IND CO LTD**Inventor(s):(std):** KAWAKAMI YASUSHI

International class (IPC 8-9): H03F1/56 H03F3/24 H03F3/68 (Advanced/Invention); H03F1/00 H03F3/20 H03F3/68 (Core/Invention)

International class (IPC 1-7): H03F1/56 H03F3/24 H03F3/68

JP class F-Term: 5J069 5J069/AA01 5J069/CA75 5J069/CA87 5J069/FA15 5J069/HA09 5J069/HA12 5J069/HA19 5J069/HA24 5J069/HA25 5J069/HA29 5J069/HA32 5J069/KA00 5J069/KA02 5J069/KA18 5J069/MA00 5J069/MA08 5J069/MA21 5J091 5J091/AA01 5J091/CA75 5J091/CA87 5J091/FA15 5J091/HA09 5J091/HA12 5J091/HA19 5J091/HA24 5J091/HA25 5J091/HA29 5J091/HA32 5J091/KA00 5J091/KA02 5J091/KA18 5J091/MA00 5J091/MA08 5J091/MA21 5J091/TA01 5J500 5J500/AA01 5J500/AC75 5J500/AC87 5J500/AF15 5J500/AH09 5J500/AH12 5J500/AH19 5J500/AH24 5J500/AH25 5J500/AH29 5J500/AH32 5J500/AK00 5J500/AK02 5J500/AK18 5J500/AM00 5J500/AM08 5J500/AM21 5J500/AT01

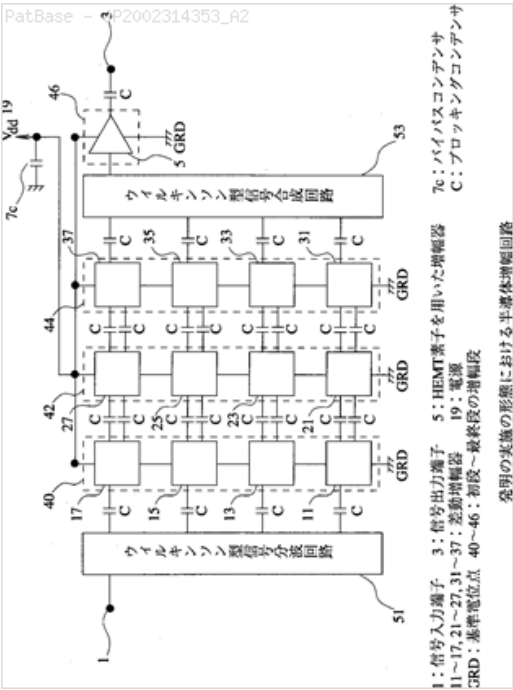
JP class F-Index: H03F1/56 H03F3/24 H03F3/68/B H03F3/68/220

Classification Explorer

Cited documents: JP3188702, JP2002171141,**Forward Citations:** WO19172168, JP5191221, JP2019508955, JP2009010910, JP2006115307,**Abstract:**

PROBLEM TO BE SOLVED: To drive an amplifier in each stage with one power supply, also to suppress the costs and to facilitate impedance matching in a circuit. SOLUTION: This semiconductor amplifier circuit is provided with differential amplifiers connected in a matrix of N rows and M columns (where, N and M are positive integers), the first to M-th columns are respectively composed of amplifiers from the first stage to the M-th stage and the semiconductor amplifier circuit is further provided with a signal divider circuit for dividing one input signal into N pieces of output signals, a signal synthesizing circuit for combining N pieces of input signals into one output signal and amplifiers constituting the last amplification stage. The N pieces of output signals are inputted to N pieces of differential amplifiers on the amplifier stage of the first stage respectively, output signals from the N pieces of differential amplifiers of

the M stage are made the N pieces of input signals, the one output signal is made an input signal to the amplifiers constituting the last amplification stage, and the amplifier stages from the first stage to the last stage are parallely connected between a common power supply and a reference potential point.



8) Family number: 53123568 (US2013049867A)

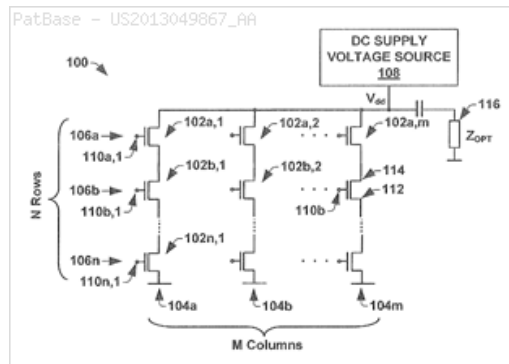
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Title: CLASS OF POWER AMPLIFIERS FOR IMPROVED BACK OFF OPERATION
Priority: US20110221118 20110830 DE201210215332 20120829
Family:

Publication number	Publication date	Application number	Application date
CN102969988 A	20130313	CN201210314595	20120830
CN102969988 B	20161221	CN201210314595	20120830
DE102012215332 A1	20130307	DE201210215332	20120829
DE102012215332 B4	20190207	DE201210215332	20120829
TW201320587 A	20130516	TW20120128233	20120806
TWI514754 B	20151221	TW20120128233	20120806
US2013049867 AA	20130228	US20110221118	20110830
US8482348 BB	20130709	US20110221118	20110830

Probable Assignee: INTEL CORP
Assignee(s):(std): INTEL CORP ; INTEL DEUTSCHLAND GMBH ; INTEL MOBILE COMM GMBH ; PINARELLO SANDRO ; MUELLER JAN ERIK
Assignee(s): ALUMINUM ATHLETIC EQUIPMENT CO ; INTEL MOBILE COMMUNICATIONS GMBH
Inventor(s):(std): PINARELLO SANDRO ; MUELLER JAN ERIK
Agent(s): ESCHWEILER AND ASSOCIATES LLC
International class (IPC 8-9): H03F1/02 H03F1/14 H03F1/22 H03F1/56 H03F3/16 H03F3/20 H03F3/21 H03F3/68 H03F3/72 (Advanced/Invention)
CPC: H03F1/0277 H03F1/223 H03F1/56 H03F3/193 H03F3/211 H03F3/245 H03F2200/108 H03F2200/27 H03F2200/387 H03F2203/21106 H03F2203/21109 H03F2203/21142 H03F2203/7206 H03F1/0211 H03F3/72
US class: 330/277 330/295 330/296 330/311 330/51
[Classification Explorer](#)
Cited documents: US8189713 BB, US8120428 BB, US8022772 BB, US7330071 BA, US6137367 A, US6064264 A, US2011176623 AA, US2011012682 AA, US2010237945 AA, US2008297259 AA, US2006119435 AA, US2005195039 AA, EP1349269 A1,
Forward Citations: WO17133776, WO17062427, US9419560, US9306513, US8830000, US2017366140, US2014266448, US2014225675, US2013069722, US10476546, US10355652, US10250999, US10218314, US10033336, TWI590582, KR20140112428, KR101665174, CN108111185,

Abstract:
One embodiment of the present invention relates to a power amplifier comprising a plurality of amplifying elements connected in a serial-parallel matrix configuration, containing parallel columns having amplifying elements connected in series. The parallel columns are connected to a common output path coupled to a supply voltage source configured to provide an equal supply voltage to each of the columns. One or more input signals (e.g., RF input signals) are connected to the power amplifier by way of input terminals on a first row of amplifying elements. The remaining amplifying elements have control terminals that are connected to independent control signals, which allow each amplifying element to be operated independent of the other amplifying elements in the matrix. This selective operation of amplifying elements allows for improved efficiency over a wide range of power amplifier output powers.



9) Family number: 50221593 (US2013169367A)

Title: ACTIVE CIRCULATOR
Priority: WO2010SE50695 20100618
Family:

Publication number	Publication date	Application number	Application date
EP2583349 A1	20130424	EP20100853324	20100618
EP2583349 A4	20131106	EP20100853324	20100618
IN10902DN2012 A	20141010	IN2012DN10902	20121214
KR101687642 B1	20161219	KR20137001008	20100618
KR20130037703 A	20130416	KR20137001008	20100618
US2013169367 AA	20130704	US20100805032	20100618
US9054676 BB	20150609	US20100805032	20100618
WO11159213 A1	20111222	WO2010SE50695	20100618

Probable Assignee: SAAB AB
Assignee(s):(std): NILSSON JOAKIM ; SAAB AB ; VICKES HANS OLOF
Inventor(s):(std): VICKES HANS OLOF ; NILSSON JOAKIM
Agent(s): NORBERG CHARLOTTE; VENABLE LLP; ERIC J; ALBIHNS ZACCO AB
Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

International class (IPC 8-9): H01P1/32 H01P1/38 H03F3/60 H03H11/36 H03H11/38 (Advanced/Invention)

CPC: H03H11/362 H03F3/604 H03F3/607 H03H11/38 H03F3/60

European class: H03F3/60C1

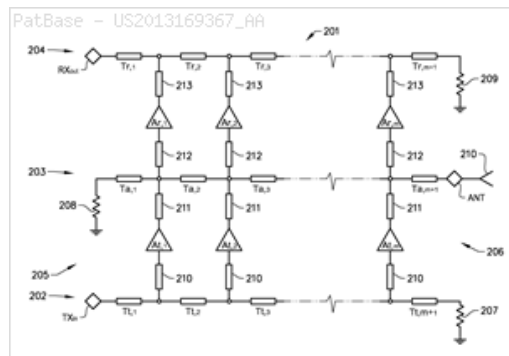
US class: 1/1 330/295

[Classification Explorer](#)

Cited documents: WO0241442 A1, US7541890 BB, US7129783 BB, US5081709 A, US5081706 A, US5081706, US2010052814 AA, US2010052814, US2009286492 AA, US2009108954 AA, US2009108954, US2004192392 AA, FR2895150 A1, EP2159922 A1,

Forward Citations: WO16085505, US9893401, US9641156, US2014266399, US10355652, US10177741,

Abstract:
An active circulator for a microwave system. The microwave system includes at least one front-end arrangement. Each front-end arrangement includes a power amplifier function arranged to deliver an amplified output signal via a circulator function to an antenna in a transmit mode. A low noise amplifier function is arranged to amplify an input signal from the antenna via the circulator function in a receive mode. The circulator function is arranged to direct a signal flow between the transmit and receive modes. Each front-end arrangement includes one active circulator. The active circulator includes the power amplifier function, the low noise amplifier function and the circulator function of directing a signal flow. The functions integrated into one module. Also, a method to manufacture the active circulator.



Title: MATRIX DISTRIBUTED POWER AMPLIFIER
Priority: US20110534095P 20110913 US20120605134 20120906
Family:

Publication number	Publication date	Application number	Application date
US2013063213 AA	20130314	US20120605134	20120906
US8823455 BB	20140902	US20120605134	20120906

Probable Assignee: QORVO US INC
Assignee(s):(std): KOBAYASHI KEVIN W ; RF MICRO DEVICES INC
Assignee(s): BANK OF AMERICA NA ADMINISTRATIVE AGENT AS ; QORVO US INC
Inventor(s):(std): KOBAYASHI KEVIN W
Agent(s): WITHROW AND TERRANOVA PLLC

International class (IPC 8-9): H03F1/22 H03F3/60 H03F3/68 (Advanced/Invention)

CPC: H03F3/605 H03F3/189 H03F3/245

US class: 330/286 330/291 330/295 330/53

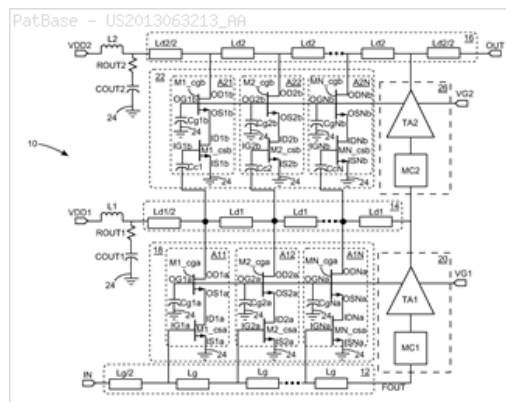
[Classification Explorer](#)

Cited documents: US7924097 BB, US7804362 BB, US7804262 BB, US7724091 BB, US7482874 BB, US7482868 BB, US6943631 BB, US6759907 BB, US6727762 BA, US6400226 BB, US6377125 BA, US6342815 BA, US6049250 A, US5880640 A, US5485118 A, US5414387 A, US5378999 A, US5365197 A, US5361038 A, US5227734 A, US5208547 A, US5046155 A, US5028879 A, US5021743 A, US4788511 A, US4752746 A, US4543535 A, US4540954 A, US2010052814 AA, US2003843831, US2003184383 AA,

Forward Citations: WO17074229, US9825603, US9500688, US9356564, US2018302040, US2017359042, US2015340997, US2014081586, US10367463, US10355652, US10340858, JP2018532340, EP3369174,

Abstract:

Disclosed is a matrix distributed amplifier (DA) having an input transmission line, an intermediate transmission line, and an output transmission line. A first plurality of amplifiers has inputs coupled to and spaced along the input transmission line and has outputs coupled to and spaced along the intermediate transmission line. A second plurality of amplifiers has inputs coupled to and spaced along the intermediate transmission line and has outputs coupled to and spaced along the output transmission line. A termination amplifier has an input coupled to the input transmission line and an output coupled to the intermediate transmission line. In at least one embodiment, a second termination amplifier has an input coupled to the intermediate transmission line and an output coupled to the output transmission line.



Title: PULSE GENERATOR FOR SOLID-STATE TELEVISION CAMERA
Priority: JP19810117777 19810729

Publication number	Publication date	Application number	Application date
DE3228199 A1	19830217	DE19823228199	19820728
DE3228199 C2	19850718	DE19823228199	19820728
FR2510851 A1	19830204	FR19820013211	19820728
FR2510851 B1	19861212	FR19820013211	19820728
JP58020066 A2	19830205	JP19810117777	19810729
US4498106 A	19850205	US19820402420	19820728

Probable Assignee: HITACHI LTD
Assignee(s):(std): HITACHI LTD
Assignee(s): HITACHI SEISAKUSHO KK
Inventor(s):(std): NISHIZAWA SHIGEKI ; TAKAHASHI KENJI ; AKIYAMA TOSHIYUKI ; SATOU KAZUHIRO ; IZUMIDA MORIJI ; IZUMITA MORISHI ; SATO KAZUHIRO
Inventor(s): KAZUHIRO SATO MORISHI IZUMITA KENJI TAKAHASHI TOSH ; KAZUHIRO SATO MORISHI IZUMITA KENJI TAKAHASHI TOSHIYUKI AKIYAMA ET SHIGEKI NISHIZAWA ; KAZUHIRO SATO MORISHI IZUMITA KENJI TAKAHASHI... ; IZUMITA MORISHI INAGI JP ; NISHIZAWA SHIGEKI MOBARA JP ; SATO KAZUHIRO TOKIO TOKYO JP ; AKIYAMA TOSHIYUKI KODAIRA JP

International class (IPC 8-9): H03K21/40 H04N3/14 H04N3/15 H04N5/06 H04N5/335 (Advanced/Invention)

1-7):

CPC: H03K21/40 H04N5/06 H04N5/335

European class: H03K21/40 H04N5/06 H04N5/335

US class: 348/308 348/312 348/524 348/550 348/E05.011 348/E05.091 348/E5.011 348/E5.091 358/150 358/212 358/213

JP class F-Term: 5C067

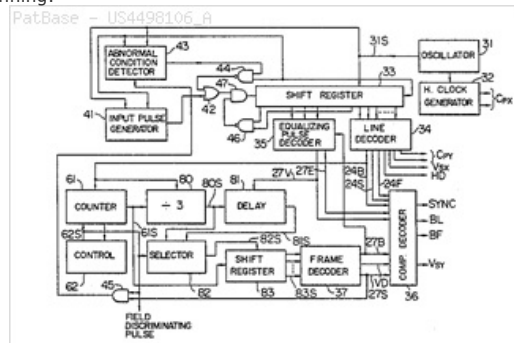
JP class F-Index: H04N3/14 H04N3/15

Classification Explorer

Forward Citations: WO9966710, US6160578, US5877808, US5559553, US5426536, US5134489, US5134488, US5038215, US4750035, US4724485, US4603354, US4551758, US10355652, EP0379371, EP0064298, EP0064298,

Abstract:

A pulse generator circuit for a solidstate television camera comprising a first circuit arrangement including a shift register of endless . type for obtaining pulses of a horizontal scanning frequency for television, a second circuit arrangement for obtaining necessary pulse trains of the horizontal scanning frequency for a television camera from a plurality of output pulses of the shift register and a third circuit arrangement for dividing the pulse obtained by the second circuit arrangement by two-different factors of mode, n and $n+1$, and delaying the $1/n$ frequency-divided mode pulse by $1/2$ horizontal scanning period in response to the output pulse from the second circuit arrangement thereby obtaining a frame pulse capable of interlaced scanning.



12) Family number: 34024963 (US2006284683A)

Title: ELECTRO-OPTICAL DEVICE, DRIVING METHOD, AND ELECTRONIC APPARATUS

Priority: JP20050177307 20050617 JP20060098049 20060331

Family:

Publication number	Publication date	Application number	Application date
JP2007025632 A2	20070201	JP20060098049	20060331
JP5011788 B2	20120829	JP20060098049	20060331
US2006284683 AA	20061221	US20060422506	20060606
US7956840 BB	20110607	US20060422506	20060606

Probable Assignee: SEIKO EPSON CORP

Assignee(s):(std): SEIKO EPSON CORP

Inventor(s):(std): ISHII TATSUYA

Agent(s): OLIFF AND BERRIDGE PLC

International class (IPC 8-9): G02F1/133 G09G3/20 G09G3/36 H03F3/68 (Advanced/Invention);
G02F1/13 G09G3/20 G09G3/36 H03F3/68 (Core/Invention)

CPC: G09G3/001 G09G3/3688 G09G5/006 G09G2300/0842 G09G2310/0251 G09G2310/0275

European class: G09G3/20M G09G3/36C14A G09G5/00T4 S09G3/00B S09G300/08E12 S09G310/02S6 S09G310/02V5

US class: 330/295 330/295P 345/100 345/103 345/99 348/790 348/791 348/792

JP class F-Term: 2H093/2H093/NA16 2H093/NA34 2H093/NA41 2H093/NA43 2H093/NA44 2H093/NC12 2H093/NC13 2H093/NC23 2H093/NC34 2H093/NC35 2H093/ND06 2H093/ND09 2H193 2H193/ZA04 2H193/ZC20 2H193/ZD32 2H193/ZF36 5C006 5C006/AC11 5C006/AC21 5C006/AF25 5C006/AF43 5C006/AF44 5C006/AF71 5C006/BB16 5C006/BC13 5C006/BC16 5C006/BC23 5C006/BF11 5C006/EC11 5C006/FA22 5C080 5C080/AA05 5C080/AA06 5C080/AA10 5C080/AA13 5C080/AA18 5C080/BB05 5C080/DD05 5C080/EE29 5C080/FF07 5C080/FF11 5C080/JJ02 5C080/JJ03 5C080/JJ04 5C080/JJ06

JP class F-Index: G02F1/133/505 G02F1/133/550 G09G3/20/621/A G09G3/20/623/L G09G3/20/623/M G09G3/20/623/V
G09G3/20/642/B G09G3/36

Classification Explorer

Cited documents: US6806862 BA, US6731266 BA, JP2005107144 A2, JP2005107144, JP2004334115 A2, JP2004334115, JP2004163623 A2, JP2004163623, JP2000112437 A2, JP11338429 A2, JP11338429, JP112437,

Forward Citations: US9495912, US8614702, US8203112, US7834308, US7723664, US7561220, US2015145905, US2010025568, US2008291308, US2008290254, US10355652, JP4822406, JP2007086584.

Abstract:

An electro-optical device includes: a plurality of scanning lines; a plurality of data lines blocked for every "m" (m is an integer of 2 or greater) columns; pixels provided corresponding to the scanning lines and the data lines and showing grayscale specified by data signals sampled to data lines when a scanning line is selected; a scanning line driving circuit which selects the plurality of scanning lines in a predetermined order; a sampling signal output circuit which sequentially outputs a plurality of sampling signals; and a sampling circuit which has sampling switches provided in the data lines, respectively, and having their one ends connected to the data

lines, and which turns on the sampling switches to sample data signals supplied to "n" (n is an integer of 2 or greater) image signal lines, to the data lines. The sampling circuit groups the blocks for every "n" blocks, makes individual blocks in the same group correspond to different image signal lines, respectively, to connect the other ends of the sampling switches in the individual blocks to corresponding image signal lines, supplies one sampling signal to two adjacent groups, and when any one sampling signal is supplied, simultaneously turns on sampling switches in the same columns in "n" blocks belonging to one group of two groups corresponding to the sampling signal.

