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20 Documents

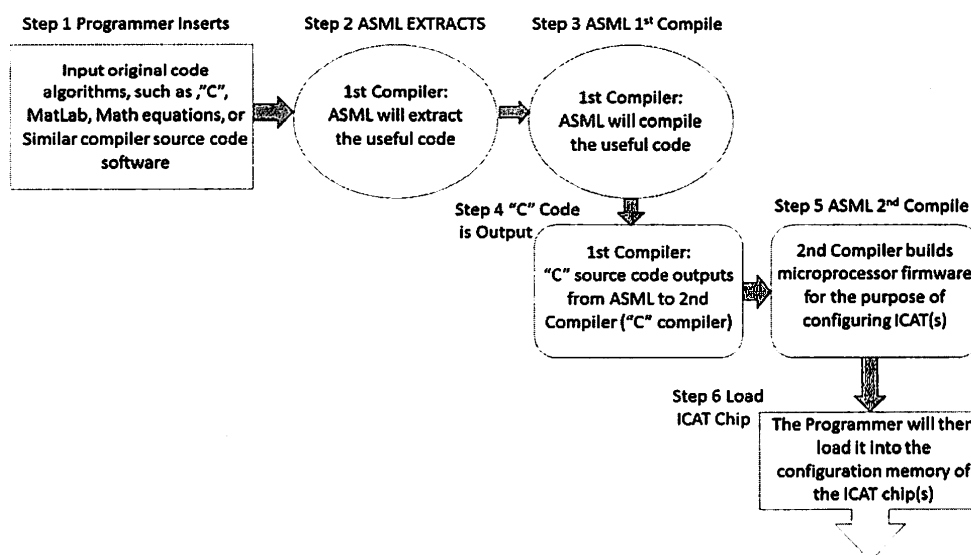
Publication numbers	Title	Current assignees
EP3408737 A1	Processor with reconfigurable algorithmic pipelined core and algorithmic matching pipelined compiler	ICAT
WO2018237361 A1	High throughput processors	ICAT
US5784636 A	Reconfigurable computer architecture for use in signal processing applications	NATIONAL SEMICONDUCTOR
EP1008069 A1	A method of designing fpgas for dynamically reconfigurable computing	XILINX
WO200440414 A2	Adaptable datapath for a digital processing system	INTEL
EP1073951 A1	Data processor with a configurable functional unit and method using such a data processor	US PHILIPS
US5933642 A	Compiling system and method for reconfigurable computing	RICOH
US6023742 A	Reconfigurable computing architecture for providing pipelined data paths	UNIVERSITY OF WASHINGTON
US5794062 A	System and method for dynamically reconfigurable computing using a processing unit having changeable internal hardware organization	RICOH, ...
EP-931380 A1	Reconfigurable computing system	NEORAM
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EP-668659 A2	Reconfigurable ASIC.	PILKINGTON GERMANY NO 2
WO200692556 A2	Reconfigurable logic in processors	CLEAR SPEED TECHNOLOGY
US20050149704 A1	Processor which accelerates execution of binary programs intended for execution on a conventional processor core, using a reconfigurable combinational logic array, a function lookup unit, and a compatible conventional processor core, without requiring recompilation	JOHNSON LUTHER A
EP1417576 A2	Retargetable compiling system and method	INTEL
WO200388071 A2	High-performance hybrid processor with configurable execution units	TENSILICA

Family 1/20 - FAMPAT - ©Questel

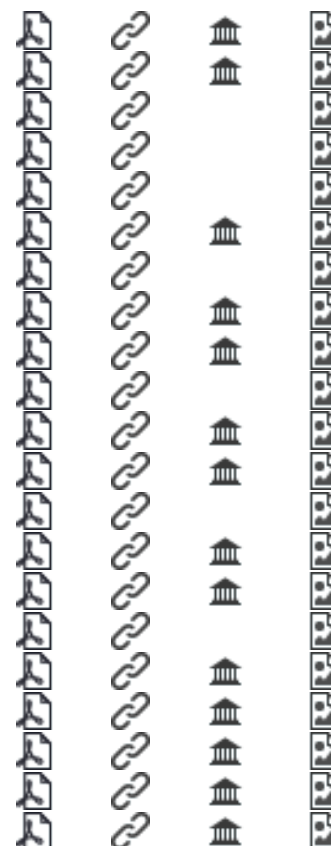
Title

(EP3408737)

Processor with reconfigurable algorithmic pipelined core and algorithmic matching pipelined compiler

Images**Publication numbers with kind code & date**

US10515041	B2	2019-12-24	US10515041
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VN62045	A	2019-03-25	VN--62045
MX2018009255	A	2019-03-18	MX2018009255
JP2019506695	A	2019-03-07	JP2019506695
CL2018002025	A1	2019-02-08	CL201802025
IN201817031832	A	2019-01-04	IN201817031832
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KR10-2018-0132044	A	2018-12-11	KR20180132044
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**IPC - International classification**

G06F-007/57; G06F-007/57; G06F-008/40; G06F-008/41; G06F-009/30; G06F-009/38; G06F-009/38; G06F-009/44; G06F-009/45; G06F-009/451; G06F-013/40; G06F-015/78; G06F-015/80; G06F-015/80; G06F-017/50; G06F-019/00

Abstract

(EP3408737)

An algorithmic matching pipelined compiler and a reusable algorithmic pipelined core comprise a system. The reusable

algorithmic pipelined core is a reconfigurable processing core with a pipelined structure comprising a processor with a setup interface for programming any of a plurality of operations as determined by setup data, a logic decision processor for programming a look up table, a loop counter and a constant register, and a block of memory. This can be used to perform functions. A reconfigurable, programmable circuit routes data and results from one core to another core and/or I/O controller and/or interrupt generator, as required to complete an algorithm without further intervention from a central or peripheral processor during processing of an algorithm.

Inventors

CATILLER ROBERT

Latest standardized assignees - inventors removed

ICAT

Family 2/20 - FAMPAT - ©Questel

Title

(WO2018237361)

High throughput processors

Images

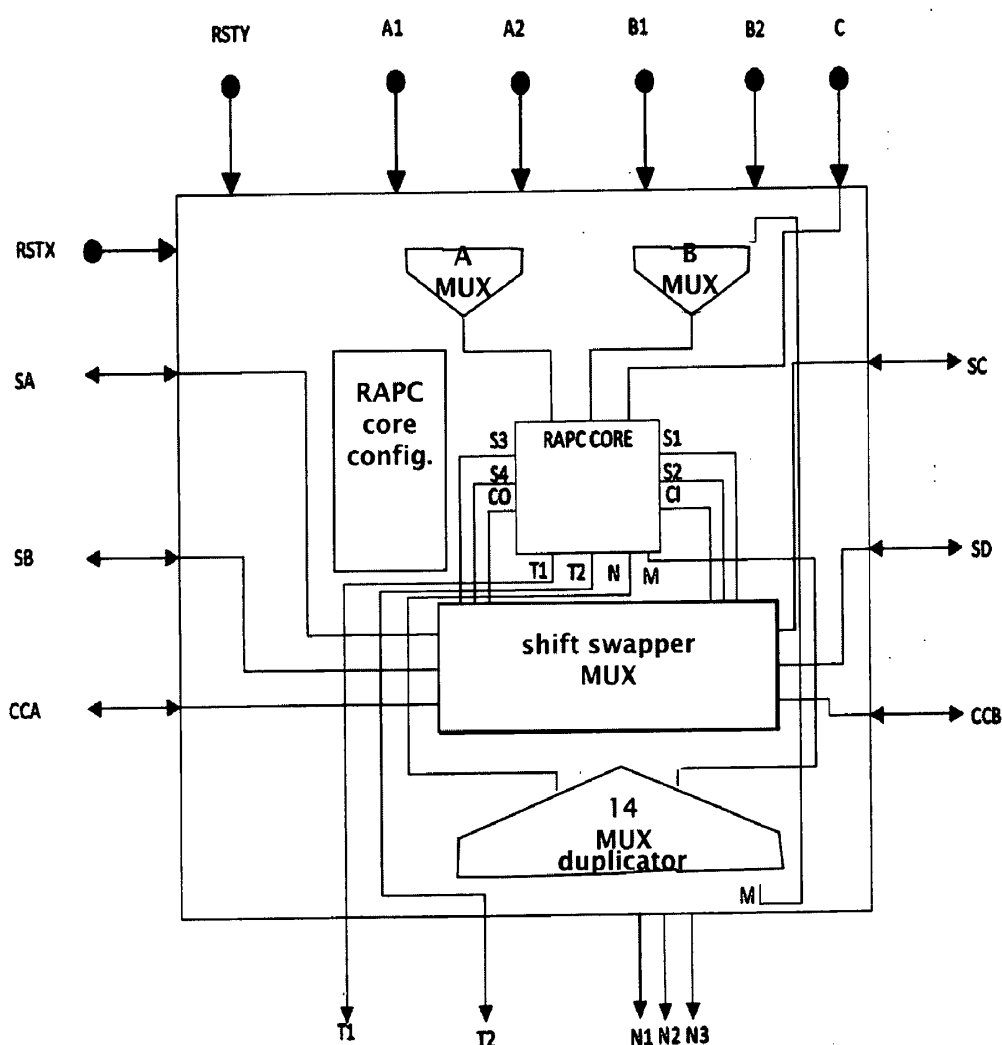


FIG. 14

Publication numbers with kind code & date

BR112019027531	A1	2019-12-31	BR112019027531
CA3067827	A1	2018-12-27	CA3067827
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IPC - International classification

G06F-007/38

Abstract

(WO2018/237361)

An algorithmic matching pipelined compiler and a reusable algorithmic pipelined core comprise a high throughput processor system. The reusable algorithmic pipelined core is a reconfigurable processing core with a pipelined structure comprising a processor with a setup interface for programming any of a plurality of operations as determined by setup data, a logic decision processor for programming a look up table, a loop counter and a constant register, and a block of memory. This can be used to perform functions. A reconfigurable, programmable circuit routes data and results from one core to another core and/or 10 controller and/or interrupt generator, as required to complete an algorithm without further intervention from a central or peripheral processor during processing of an algorithm.

Inventors

CATILLER ROBERT

ROIG DANIEL

ELUMALAI GNANASHANMUGAM

Latest standardized assignees - inventors removed

ICAT

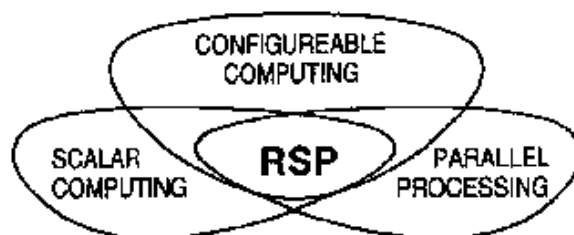
Family 3/20 - FAMPAT - ©Questel

Title

(US5784636)

Reconfigurable computer architecture for use in signal processing applications

Images

**FIG. 1**

Type ZA	OP				
Type SC	OP		C		
Type SM	OP		0	A	
Type SM Indirect	OP		1	AM	R
Type MS	OP	S	i	A	
Type MR	OP	R	i	A	
Type LC	OP		i	A	
	C				
Type LM	OP		i	A	
	A				

FIG. 4**Publication numbers with kind code & date**

DE19722365	B4	2005-07-28	DE19722365
KR100305947	B1	2001-10-19	KR100305947
US5784636	A	1998-07-21	US5784636
KR970076254	A	1997-12-12	KR19970076254
DE19722365	A1	1997-12-04	DE19722365

**IPC - International classification**

G06F-015/78; G06F-015/78; G06F-015/80

Abstract

(US5784636)

An architecture for information processing devices which allows the construction of low cost, high performance systems for

specialized computing applications involving sensor data processing. The reconfigurable processor architecture of the invention uses a programmable logic structure called an Adaptive Logic Processor (ALP). This structure is similar to an extendible field programmable gate array (FPGA) and is optimized for the implementation of program specific pipeline functions, where the function may be changed any number of times during the progress of a computation. A Reconfigurable Pipeline Instruction Control (RPIC) unit is used for loading the pipeline functions into the ALP during the configuration process and coordinating the operations of the ALP with other information processing structures, such as memory, I/O devices, and arithmetic processing units. Multiple components having the reconfigurable architecture of the present invention may be combined to produce high performance parallel processing systems based on the Single Instruction Multiple Data (SIMD) architecture concept.

Inventors

RUPP CHARLE R

Latest standardized assignees - inventors removed

NATIONAL SEMICONDUCTOR

Family 4/20 - FAMPAT - ©Questel

Title

(EP1008069)

A method of designing fpgas for dynamically reconfigurable computing

Images

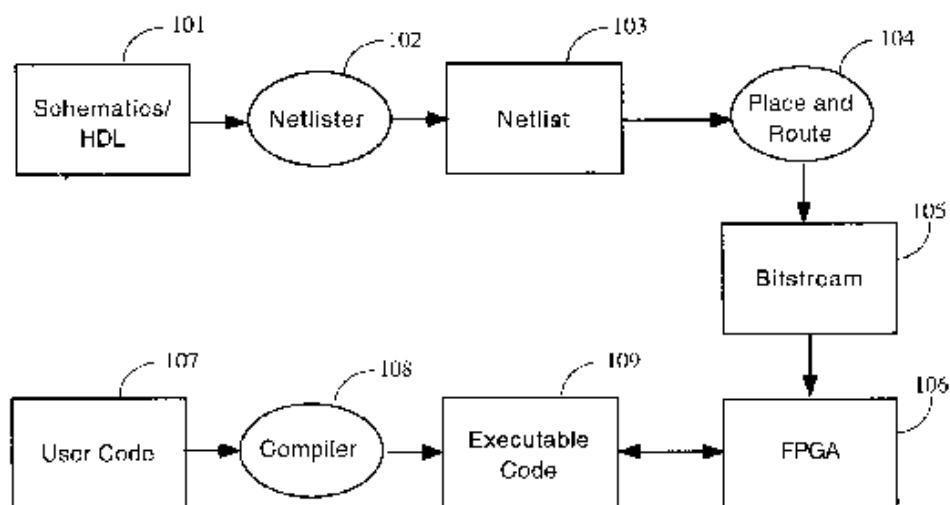


FIG. 1 (Prior Art)

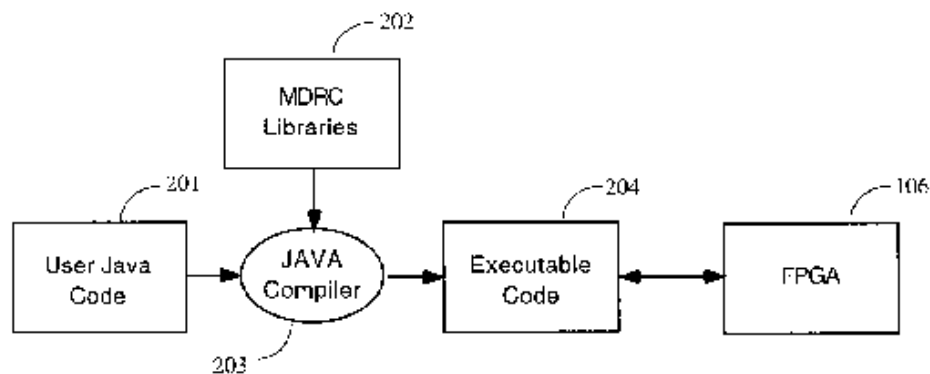


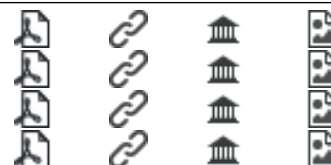
FIG. 2

Publication numbers with kind code & date

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US6557156	B1	2003-04-29	US6557156
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EP1187042	A1	2002-03-13	EP1187042
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US6216259	B1	2001-04-10	US6216259



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EP1008069	A1	2000-06-14	EP1008069
WO99/12111	B1	1999-04-15	WO9912111
WO99/12111	A1	1999-03-11	WO9912111

**IPC - International classification**

G06F-017/50; G06F-017/50

Abstract

(EP1008069)

A method of designing FPGAs for reconfigurable computing comprises a software environment for reconfigurable coprocessor applications. This environment comprises a standard high level language compiler (i.e. Java) and a set of libraries. The FPGA is configured directly from a host processor, configuration, reconfiguration and host run-time operation being supported in a single piece of code. Design compile times on the order of seconds and built-in support for parameterized cells are significant features of the inventive method.

Inventors

GUCCIONE STEVEN A

Latest standardized assignees - inventors removed

XILINX

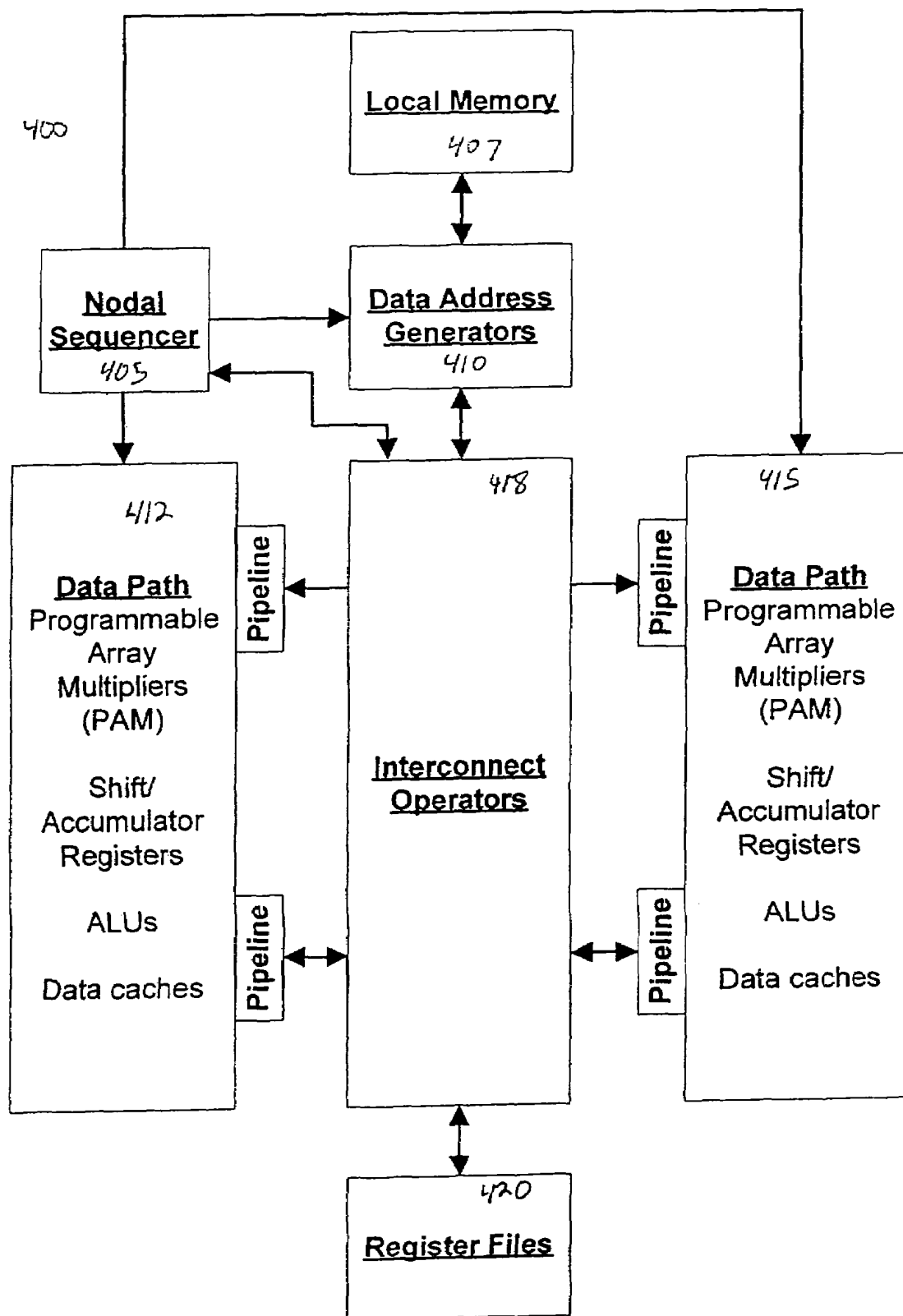
Family 5/20 - FAMPAT - ©Questel

Title

(WO200440414)

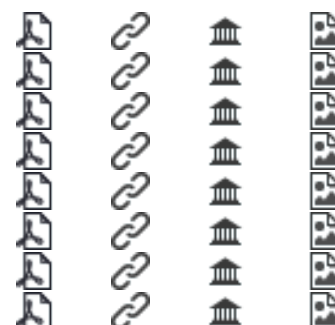
Adaptable datapath for a digital processing system

Images



Publication numbers with kind code & date

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WO2004/040414	A2	2004-05-13	WO200440414				
WO2004/040456	A2	2004-05-13	WO200440456				

IPC - International classification

G06F; G06F-003/00; G06F-009/00; G06F-009/06; G06F-009/30; G06F-009/302; G06F-009/312; G06F-009/318; G06F-009/38; G06F-009/38; G06F-012/00; G06F-012/02; G06F-013/00; G06F-017/14

Abstract

(WO2004/040414)

The present invention includes a adaptable high-performance node (RXN) with several features that enable it to provide high performance along with adaptability. A preferred embodiment of the RXN includes a run-time configurable data path and control path. The RXN supports multi-precision arithmetic including 8, 16, 24, and 32 bit codes. Data flow can be reconfigured to minimize register accesses for different operations. For example, multiply-accumulate operations can be performed with minimal, or no, register stores by reconfiguration of the data path. Predetermined kernels can be configured during a setup phase so that the RXN can efficiently execute, e.g., discrete cosine transform (DCT), fast-Fourier transform (FFT) and other operations. Other features are provided.

Inventors

RAMCHANDRAN AMIT

Latest standardized assignees - inventors removed

INTEL

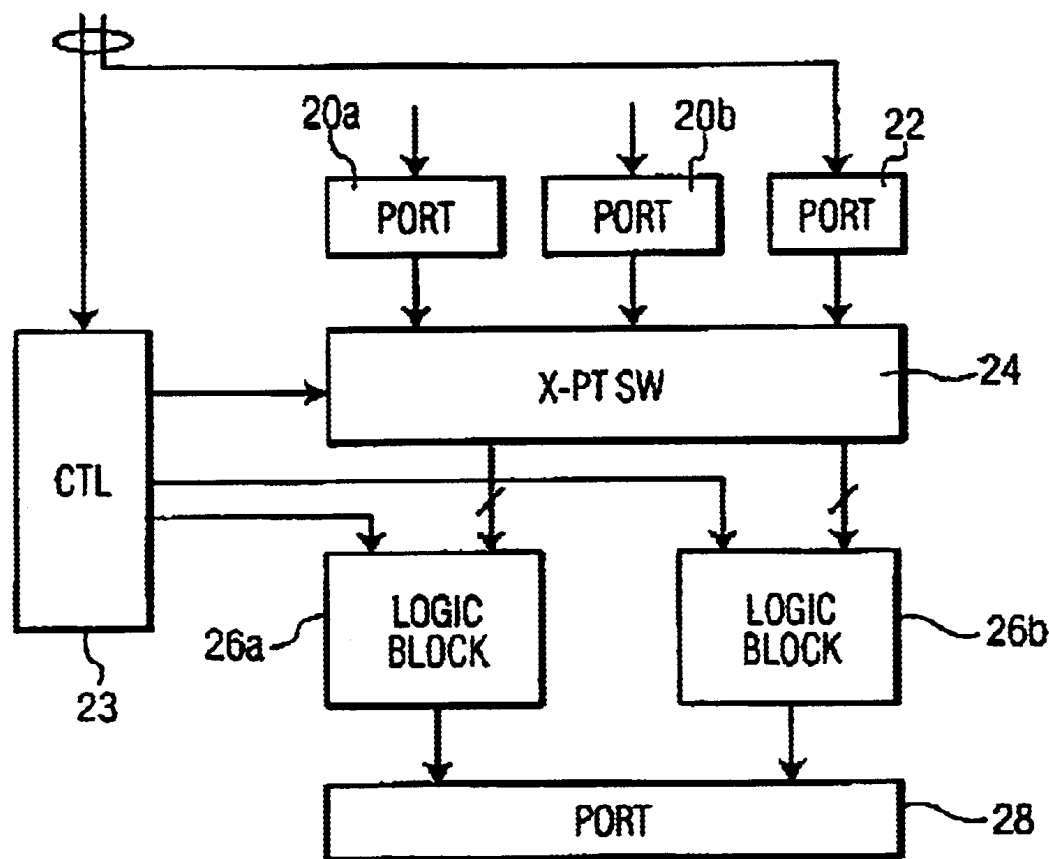
Family 6/20 - FAMPAT - ©Questel

Title

(EP1073951)

Data processor with a configurable functional unit and method using such a data processor

Images



Publication numbers with kind code & date

JP5148029	B2	2012-12-07	JP5148029
KR100731371	B1	2007-06-21	KR100731371
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EP1073951	A1	2001-02-07	EP1073951
WO00/49496	A1	2000-08-24	WO200049496



IPC - International classification

G06F-009/318; G06F-009/38; G06F-009/38; G06F-009/45; G06F-015/78; G06F-017/50

Abstract

(EP1073951)

A processor contains a configurable functional unit that is capable of executing reconfigurable instructions, whose effect can be redefined at run-time by loading a configuration program. Reconfigurable instructions are selected in combinations of more than one different reconfigurable instruction. A respective configuration program for each combination of instructions is generated. Each time when an instruction from one of the combinations is needed during execution and the configurable functional unit is not configured with the configuration program for that combination, the configuration program for all of the instructions of that combination is loaded into the configurable functional unit. The reconfigurable instructions selects which instruction of the combination is executed.

Inventors

DE OLIVEIRA KASTRUP PEREIRA BE

BINK ADRIANUS J

HOOGERBRUGGE JAN

Latest standardized assignees - inventors removed

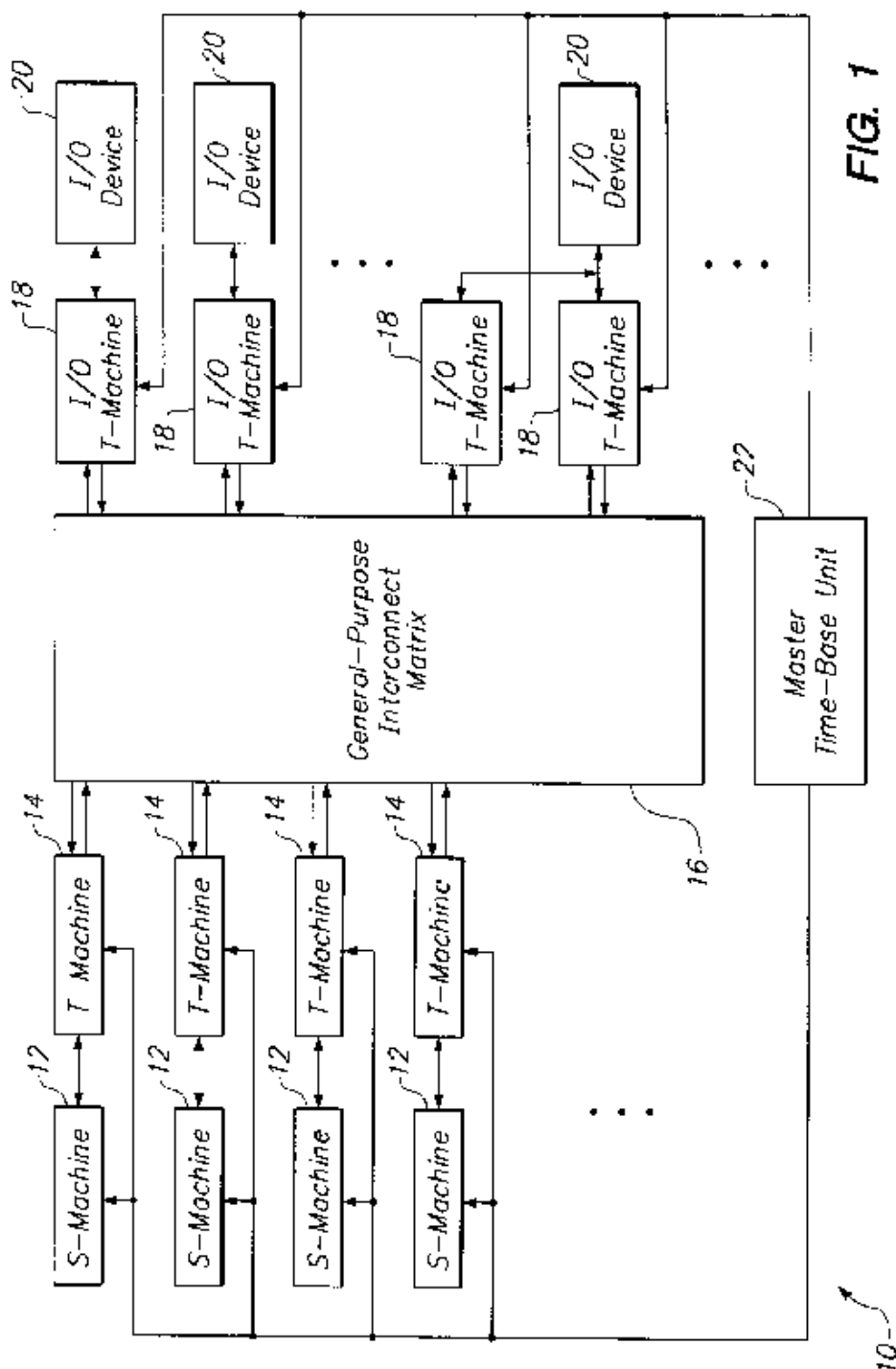
US PHILIPS

Family 7/20 - FAMPAT - ©Questel

Title

(US5933642)

Compiling system and method for reconfigurable computing

Images**Publication numbers with kind code & date**

JP4050764	B2	2007-12-07	JP4050764
JP2006155632	A	2006-06-15	JP2006155632
DE19815865	B4	2004-11-04	DE19815865
US5933642	A	1999-08-03	US5933642
DE19815865	A1	1998-12-10	DE19815865



JPH10320214

A

1998-12-04

JP10320214

**IPC - International classification**

G06F-009/24; G06F-009/30; G06F-009/318; G06F-009/38; G06F-009/445; G06F-009/45; G06F-015/78

Abstract

(US5933642)

A compiling system and method for generating a sequence of program instructions for use in a dynamically reconfigurable processing unit having an internal hardware organization that is selectively changeable among a plurality of hardware architectures, each hardware architecture executing instructions from a corresponding instruction set. Source files are compiled for execution using various instruction set architectures as specified by reconfiguration directives. Object files optionally encapsulate bitstreams specifying hardware architectures corresponding to instruction set architectures with executable code for execution on the architectures.

Inventors

GREENBAUM JACK E

BAXTER MICHAEL A

Latest standardized assignees - inventors removed

RICOH

Family 8/20 - FAMPAT - ©Questel

Title

(US6023742)

Reconfigurable computing architecture for providing pipelined data paths

Images

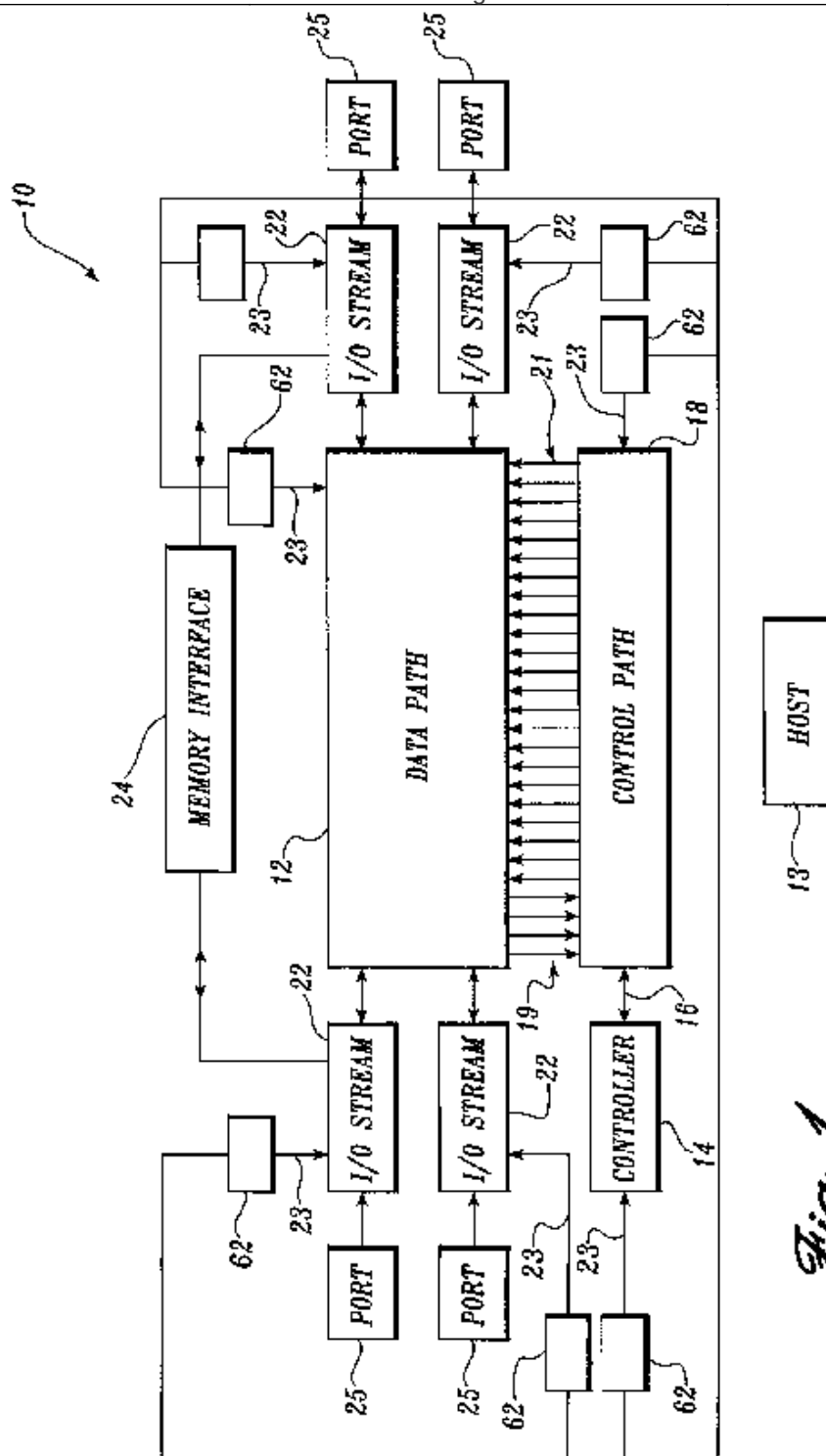


Fig. 1.

Publication numbers with kind code & date

US6023742

A 2000-02-08

US6023742



IPC - International classification

G06F-015/78; G06F-015/78

Abstract

(US6023742)

A configurable computing architecture (10) has its functionality controlled by a combination of static and dynamic control, wherein the configuration is referred to as static control and instructions are referred to as dynamic control. A reconfigurable data path (12) has a plurality of elements including functional units (32, 36), registers (30), and memories (34) whose interconnection and functionality is determined by a combination of static and dynamic control. These elements are connected together, using the static configuration, into a pipelined data path that performs a computation of interest.

The dynamic control signals (21) are suitably used to change the operation of a functional unit and the routing of signals between functional units. The static control signals (23) are provided each by a static memory cell (62) that is written by a host (13). The controller (14) generates control instructions (16) that are interpreted by a control path (18) that computes the dynamic control signals. The control path is configured statically for a given application to perform the appropriate interpretation of the instructions generated by the controller. By using a combination of static and dynamic control information, the amount of dynamic control used to achieve flexible operation is significantly reduced.

Inventors

EBELING WILLIAM HENRY CARL

CRONQUIST DARREN CHARLES

FRANKLIN PAUL DAVID

Latest standardized assignees - inventors removed

UNIVERSITY OF WASHINGTON

Family 9/20 - FAMPAT - ©Questel

Title

(US5794062)

System and method for dynamically reconfigurable computing using a processing unit having changeable internal hardware organization

Images

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US6594752

KR100283812

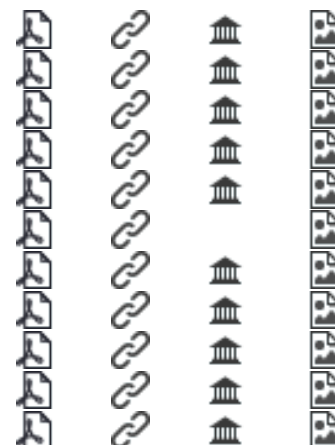
US6182206

TW-394884

US6058469

US6021186

US5794062



KR960038592	A	1996-11-21	KR19960038592
JP08286908	A	1996-11-01	JP08286908
DE19614991	A1	1996-10-24	DE19614991

**IPC - International classification**

G06F-009/24; G06F-009/30; G06F-009/30; G06F-009/312; G06F-009/318; G06F-009/38; G06F-009/445; G06F-009/45; G06F-012/00; G06F-015/00; G06F-015/00; G06F-015/173; G06F-015/78; G06F-015/80; G06F-015/80

Abstract

(US5794062)

A set of S-machines, a T-machine corresponding to each S-machine, a General Purpose Interconnect Matrix (GPIM), a set of I/O T-machines, a set of I/O devices, and a master time-base unit form a system for scalable, parallel, dynamically reconfigurable computing. Each S-machine is a dynamically reconfigurable computer having a memory, a first local time-base unit, and a Dynamically Reconfigurable Processing Unit (DRPU). The DRPU is implemented using a reprogrammable logic device configured as an Instruction Fetch Unit (IFU), a Data Operate Unit (DOU), and an Address Operate Unit (AOU), each of which are selectively reconfigured during program execution in response to a reconfiguration interrupt or the selection of a reconfiguration directive embedded within a set of program instructions. Each reconfiguration interrupt and each reconfiguration directive references a configuration data set specifying a DRPU hardware organization optimized for the implementation of a particular Instruction Set Architecture (ISA). The IFU directs reconfiguration operations, instruction fetch and decode operations, memory access operations, and issues control signals to the DOU and the AOU to facilitate instruction execution. The DOU performs data computations, and the AOU performs address computations. Each T-machine is a data transfer device having a common interface and control unit, one or more interconnect I/O units, and a second local time-base unit. The GPIM is a scalable interconnect network that facilitates parallel communication between T-machines. The set of T-machines and the GPIM facilitate parallel communication between S-machines.

Inventors

BAXTER MICHAEL A

Latest standardized assignees - inventors removed

RICOH

RICOH SILICON VALLEY

Family 10/20 - FAMPAT - ©Questel

Title

(EP-931380)

Reconfigurable computing system

Images

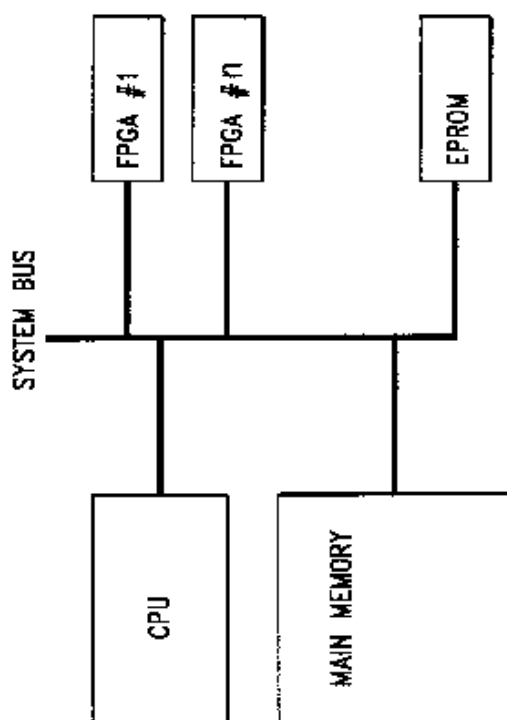


FIG. 1
PRIOR ART

Publication numbers with kind code & date

CA2264060	C	2008-01-08	CA2264060
JP3801214	B2	2006-05-12	JP3801214
HK1023458	A1	2005-12-02	HK1023458
CN1188948	C	2005-02-09	CN1188948C
KR100458371	B1	2004-11-26	KR100458371
DE69713784	T2	2003-03-13	DE69713784
DE69713784	D1	2002-08-08	DE69713784
AT220263	T	2002-07-15	ATE220263
EP0931380	B1	2002-07-03	EP-931380
JP2000516418	A	2000-12-05	JP2000516418
KR20000068256	A	2000-11-25	KR20000068256



CN1234923	A	1999-11-10	CN1234923				
EP0931380	A1	1999-07-28	EP-931380				
US5838165	A	1998-11-17	US5838165				
AU3705297	A	1998-03-06	AU9737052				
CA2264060	A1	1998-02-26	CA2264060				
WO98/08306	A1	1998-02-26	WO9808306				

IPC - International classification

G06F-015/78; H03K-019/177; H03K-019/177

Abstract

(EP0931380)

A technique for configuring arrays of programmable logic cells, including those associated with FPGA devices, through a novel DRAM-based configuration control structure that enables not only "on-the-fly" alterable chip and similar device reconfigurations, but, where desired, self-modifying reconfigurations for differing functionalities of the devices, eliminating current serious reconfigurability limitations and related problems, while providing significantly enhanced system performance at low cost. A large amount of memory is available internal to the FPGA and is accessed with a small number of pins such that the reconfiguration time is, for example, four orders of magnitude faster than the traditional approaches and at notably low cost.

Inventors

CHATTER MUKESH

Latest standardized assignees - inventors removed

NEORAM

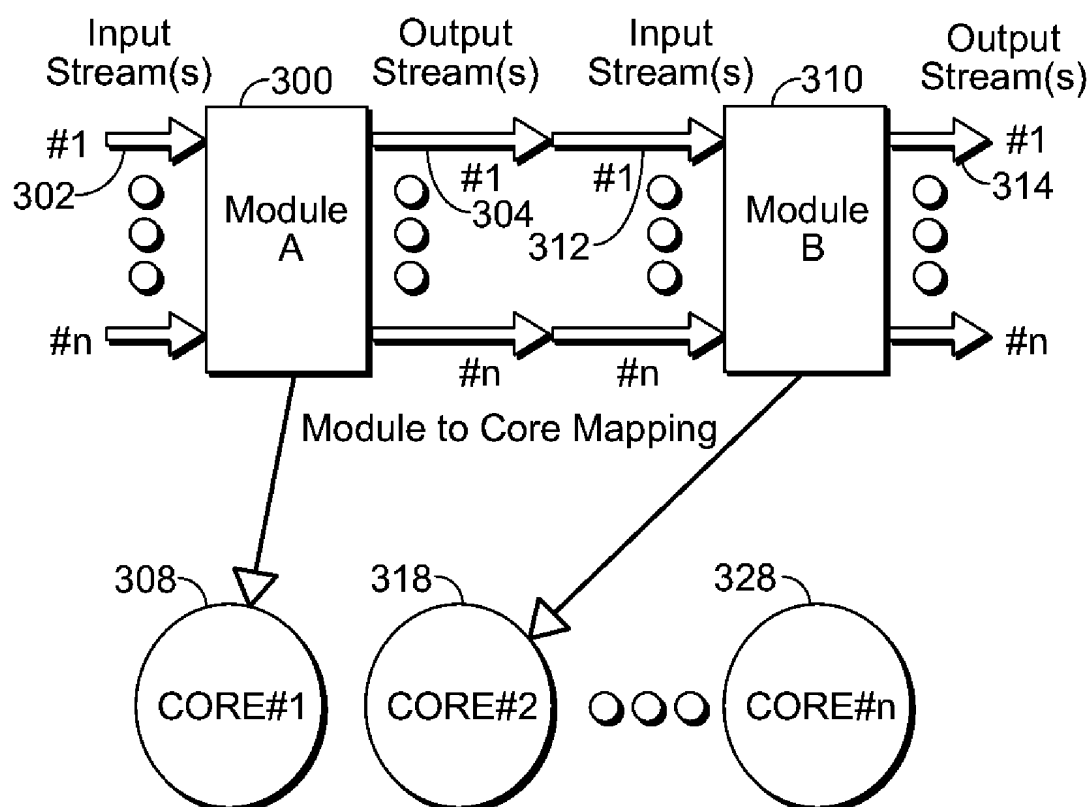
Family 11/20 - FAMPAT - ©Questel

Title

(EP2117123)

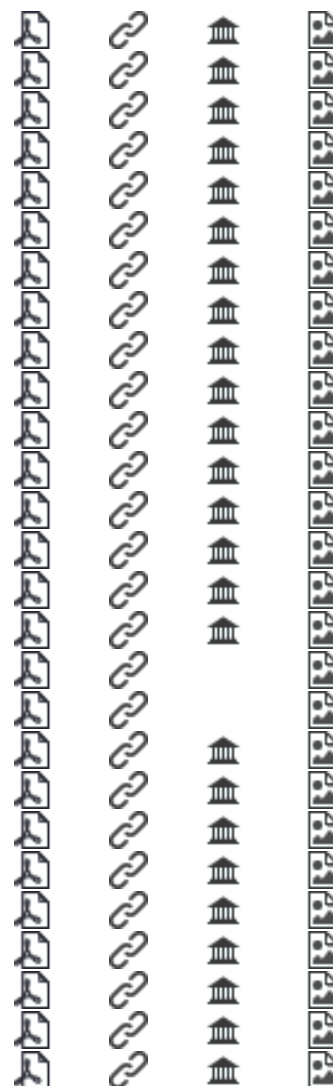
Adaptive integrated circuitry with heterogeneous and reconfigurable matrices of diverse and adaptive computational units having fixed, application specific computational elements

Images



Publication numbers with kind code & date

US10073700	B2	2018-09-11	US10073700
US9934011	B2	2018-04-03	US9934011
US20150347106	A1	2015-12-03	US20150347106
US9164952	B2	2015-10-20	US9164952
US9110692	B2	2015-08-18	US9110692
US20150012725	A1	2015-01-08	US20150012725
US20140122764	A1	2014-05-01	US20140122764
US8543795	B2	2013-09-24	US8543795
US8356161	B2	2013-01-15	US8356161
US20120124333	A1	2012-05-17	US20120124333
US20120036514	A1	2012-02-09	US20120036514
US20100161940	A1	2010-06-24	US20100161940
EP2117123	A3	2009-12-30	EP2117123
US7624204	B2	2009-11-24	US7624204
EP2117123	A2	2009-11-11	EP2117123
DE60233144	D1	2009-09-10	DE60233144
AT438227	T	2009-08-15	ATE438227
KR100910777	B1	2009-08-04	KR100910777
EP1415399	B1	2009-07-29	EP1415399
US20090037691	A1	2009-02-05	US20090037691
US20090037693	A1	2009-02-05	US20090037693
JP4238033	B2	2008-12-26	JP4238033
US7325123	B2	2008-01-29	US7325123
JP2005508532	A	2005-03-31	JP2005508532
US6836839	B2	2004-12-28	US6836839
US20040181614	A1	2004-09-16	US20040181614
EP1415399	A2	2004-05-06	EP1415399



EP1415399	A2	2004-05-06	EP1415399				
TW578098	B	2004-03-01	TW-578098				
WO02/77849	A3	2004-02-19	WO200277849				
KR20030096283	A	2003-12-24	KR20030096283				
US20030154357	A1	2003-08-14	US20030154357				
AU2002247295	A1	2002-10-08	AU2002247295				
WO02/77849	A2	2002-10-03	WO200277849				
US20020138716	A1	2002-09-26	US20020138716				

IPC - International classification

G06F-003/00; G06F-009/02; G06F-009/06; G06F-009/38; G06F-009/44; G06F-009/445; G06F-009/45; G06F-009/46; G06F-009/48; G06F-009/50; G06F-013/00; G06F-013/38; G06F-013/40; G06F-015/00; G06F-015/00; G06F-015/173; G06F-015/76; G06F-015/76; G06F-015/78; G06F-015/78; G06F-015/80; G06F-015/80; G06F-017/10; H03K-019/173; H03K-019/177; H03K-019/177

Abstract

(EP2117123)

A new category of integrated circuitry and a new methodology for adaptive or reconfigurable computing is provided. The preferred IC embodiment includes a plurality of heterogeneous computational elements coupled to an interconnection network. The plurality of heterogeneous computational elements includes computational elements having differing architectures for performing different functions such as memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output and field programmability. In response to configuration information, the interconnection network is operative in real-time to configure and reconfigure the plurality of heterogeneous computational elements for a plurality of different functional modes including linear algorithmic operations, non-linear algorithmic operations, finite state machine operations and bit-level manipulations. The various architectures are selected to comparatively minimize power consumption and increase performance of the adaptive computing integrated circuit which is particularly suitable for mobile, hand-held or other battery powered computing applications.

Inventors

MASTER PAUL L

HOGENAUER EUGENE

SCHEUERMANN WALTER JAMES

Latest standardized assignees - inventors removed

CORNAMI

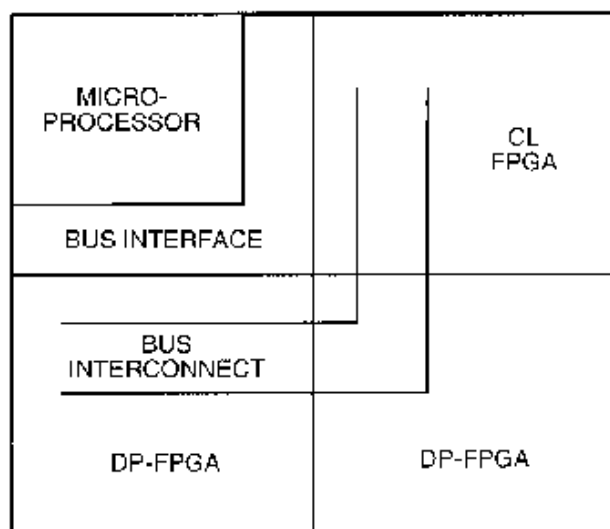
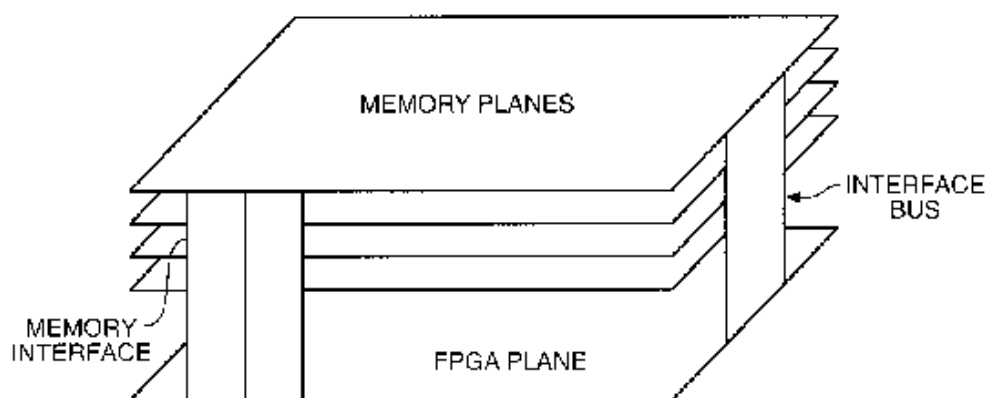
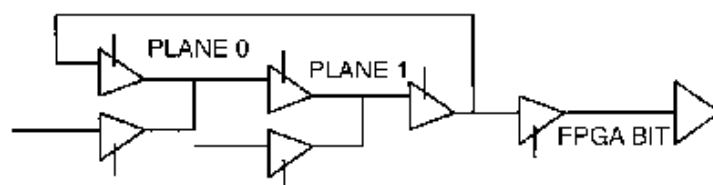
Family 12/20 - FAMPAT - ©Questel

Title

(EP1015984)

An integrated processor and programmable data path chip for reconfigurable computing

Images

**FIG._1****FIG._2****FIG._3 (PRIOR ART)****Publication numbers with kind code & date**

KR100614490	B1	2006-08-22	KR100614490
JP2002511173	A	2002-04-09	JP2002511173
EP1015984	A4	2001-11-21	EP1015984
US6282627	B1	2001-08-28	US6282627
KR20010020545	A	2001-03-15	KR20010020545
EP1015984	A1	2000-07-05	EP1015984
US5970254	A	1999-10-19	US5970254
AU8177598	A	1999-01-19	AU9881775
CA2291789	A1	1999-01-07	CA2291789
WO99/00739	A1	1999-01-07	WO9900739

IPC - International classification



G06F-009/38; G06F-009/38; G06F-013/00; G06F-013/14; G06F-015/78

Abstract

(EP1015984)

The present invention, generally speaking, provides a reconfigurable computing solution that offers the flexibility of software development and the performance of dedicated hardware solutions. A reconfigurable processor chip includes a standard processor, blocks of reconfigurable logic (1101, 1103), and interfaces (319a, 319b, 311) between these elements. The chip allows application code to be recompiled into a combination of software and reloadable hardware blocks using corresponding software tools. A mixture of arithmetic cells and logic cells allows for higher effective utilization of silicon than a standard interconnect. More efficient use of configuration stack memory results, since different sections of converted code require different portions of ALU functions and bus interconnect. Many types of interfaces with the embedded processor are provided, allowing for fast interface between standard processor code and configurable "hard-wired" functions.

Inventors

WONG DALE

PHILLIPS CHRISTOPHER E

COOKE LAURENCE H

Latest standardized assignees - inventors removed

INTEL

Family 13/20 - FAMPAT - ©Questel

Title

(US5737631)

Reprogrammable instruction set accelerator

Images

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Publication numbers with kind code & date

US5752035	A	1998-05-12	US5752035
US5748979	A	1998-05-05	US5748979
US5737631	A	1998-04-07	US5737631



IPC - International classification

G06F-009/30; G06F-009/30; G06F-009/318; G06F-009/32; G06F-009/38; G06F-009/45; G06F-015/78

Abstract

(US5737631)

A microprocessor comprises a defined execution unit coupled to internal buses of the processor for execution of a predefined set of instructions, combined with a programmable execution unit coupled to the internal buses for execution of a programmed instruction providing an on chip reprogrammable instruction set accelerator RISA. The programmable

execution unit may be made using a field programmable gate array having a configuration store, and resources for accessing the configuration store to program the programmable execution unit. An instruction register is included in the data processor which holds a current instruction for execution, and is coupled to an instruction data path to supply the instruction to the defined instruction unit and to the programmable instruction unit in parallel, through appropriate decoding resources. A condition code register is coupled to instruction fetching resources, and connected to receive condition codes from both the defined execution unit and from the programmable execution unit. The programmable execution unit includes logic to signal the instruction fetching resources to provide a next instruction when execution of the programmed instruction is done. Resources for accessing the configuration store to program the programmable execution unit are provided, which can utilize the internal buses of the data processor or be completely independent of them.

Inventors

TRIMBERGER STEPHEN M

Latest standardized assignees - inventors removed

XILINX

Family 14/20 - FAMPAT - ©Questel

Title

(WO9910802)

A reconfigurable arithmetic datapath

Images

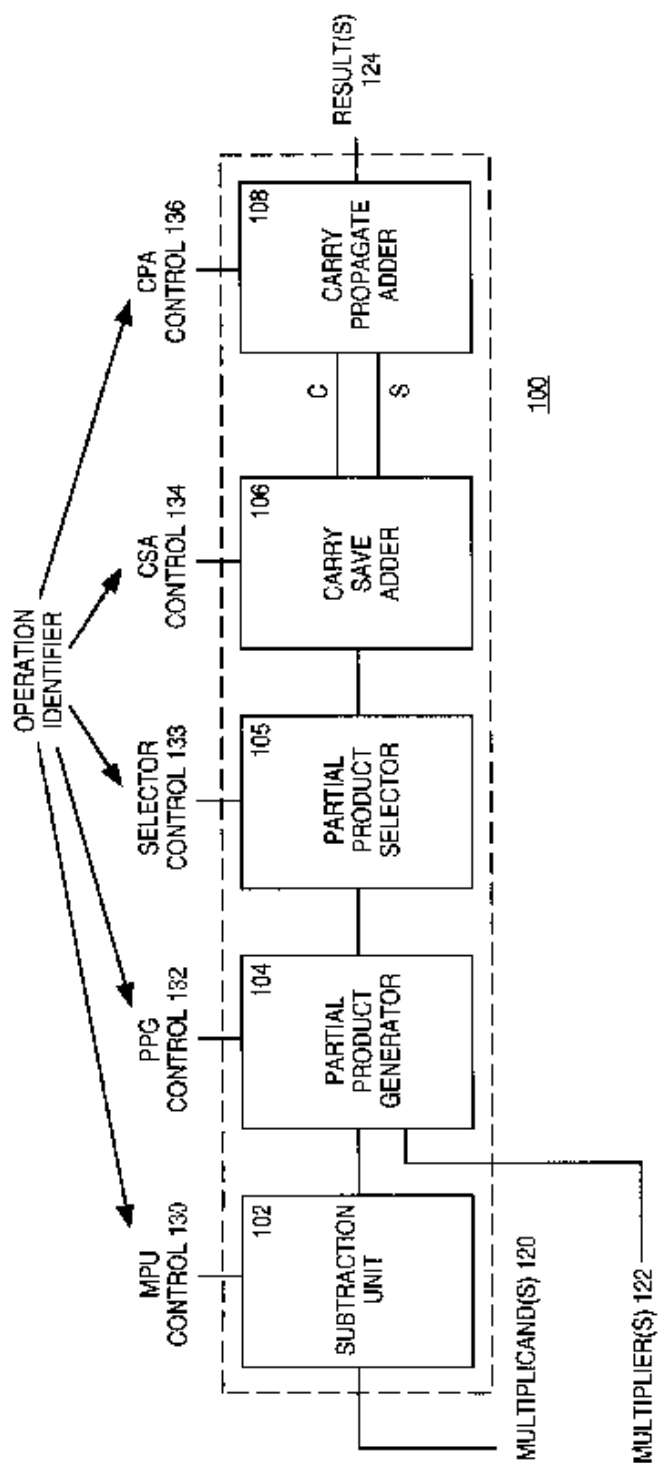


FIG. 1

Publication numbers with kind code & date

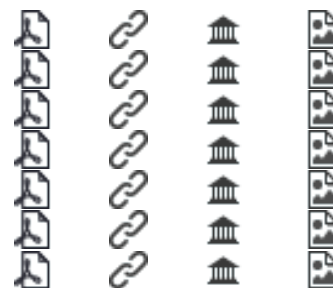
US6438569	B1	2002-08-20	US6438569
AU6338600	A	2001-01-31	AU200063386
WO01/01236	A1	2001-01-04	WO200101236
US6150836	A	2000-11-21	US6150836
US5974435	A	1999-10-26	US5974435
AU9039598	A	1999-03-16	AU9890395
WO99/10802	A1	1999-03-04	WO9910802

IPC - International classification

G06F-007/52; G06F-007/533; G06F-007/544; G06F-017/10; H03K-019/173; H03K-019/177; H03K-019/177

Abstract

(WO99/10802)



A method and apparatus that combine the same basic hardware elements in several ways to perform a plurality of arithmetic operations over different numbers of operands of different lengths. The allowed options include the multiplication (120) and summing of several operands in a single operation. The reuse of hardware elements is obtained by the use of a multiplication hardware (120) structure together with multiplexer (122) logic (or similar selection logic) at appropriate points in the hardware structure, which allows a minimum of extra hardware and a small number of extra gate delays along any critical path, thereby ensuring that the flexibility to use different operand lengths and numbers of operands incurs only a small penalty in processing speed and/or chip area in a VLSI circuit implementation.

Inventors

ABBOTT CURTIS

Latest standardized assignees - inventors removed

PMC SIERRA

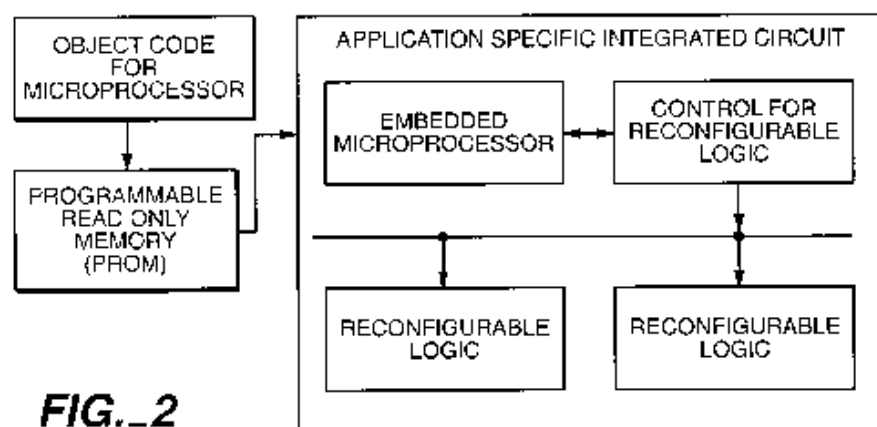
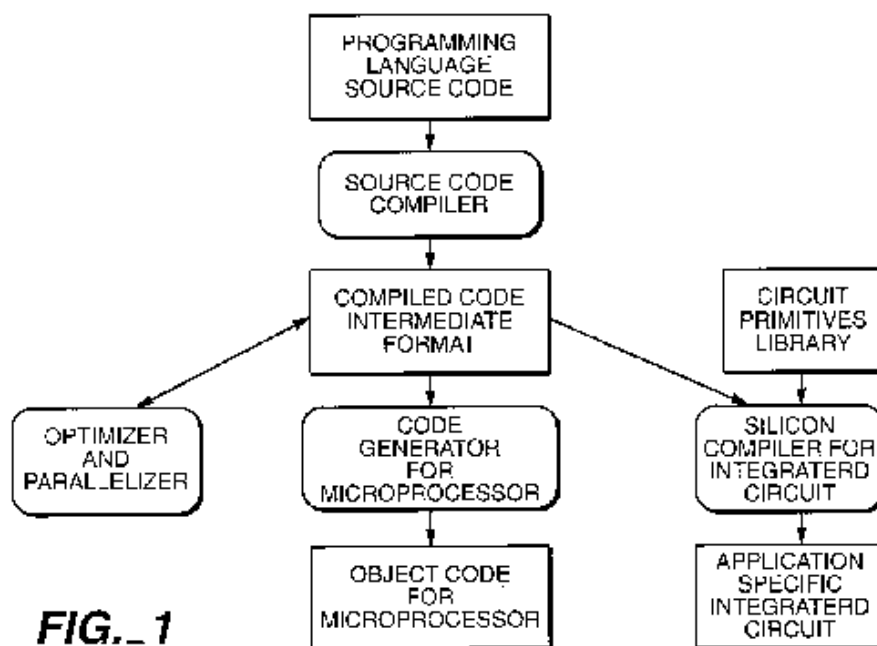
Family 15/20 - FAMPAT - ©Questel

Title

(EP-991997)

Method for compiling high level programming languages

Images



Publication numbers with kind code & date

KR100614491	B1	2006-08-22	KR100614491
EP0991997	A4	2004-12-29	EP-991997
US6708325	B2	2004-03-16	US6708325
US20030014743	A1	2003-01-16	US20030014743
JP2002508102	A	2002-03-12	JP2002508102
KR20010020544	A	2001-03-15	KR20010020544
EP0991997	A1	2000-04-12	EP-991997
US5966534	A	1999-10-12	US5966534
AU8275498	A	1999-01-19	AU9882754
CA2290649	A1	1999-01-07	CA2290649
WO99/00731	A1	1999-01-07	WO9900731



IPC - International classification

G06F-009/45; G06F-009/48; G06F-017/50

Abstract

(EP0991997)

A computer program (item 101), written in a high level programming language, is compiled (item 103) into an intermediate data structure (105) which represents its control and data flow. This data structure is analyzed (item 111) to identify critical blocks of logic which can be implemented as an application specific integrated circuit (item 117) to improve the overall performance. The critical blocks of logic are first transformed into new equivalent logic with maximum data parallelism. The new parallelized logic is then translated into a Boolean gate representation which is suitable for implementation on an application specific integrated circuit (item 117). The application specific integrated circuit (item 117) is coupled with a generic microprocessor via custom instructions for the microprocessor (item 107). The original computer program is then compiled into object code (item 109) with the new expanded target instruction set.

Inventors

COOKE LAURENCE H

PHILLIPS CHRISTOPHER E

WONG DALE

Latest standardized assignees - inventors removed

INTEL

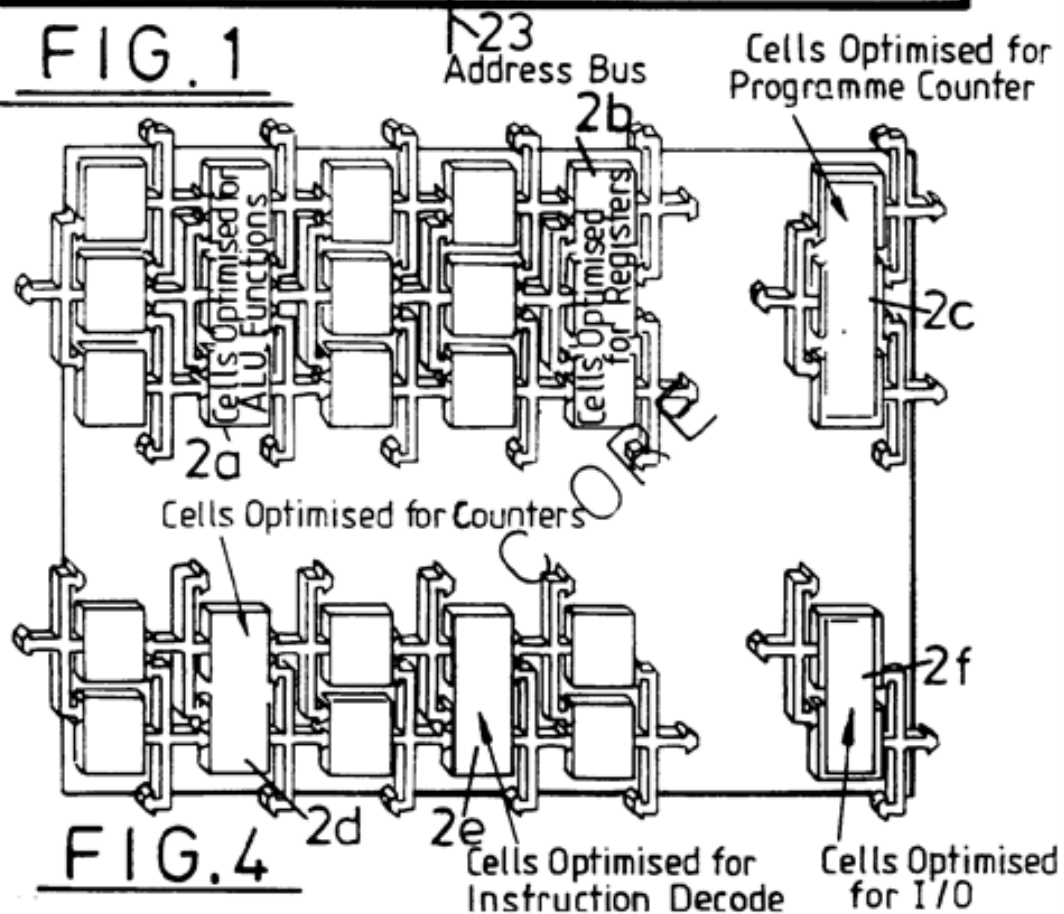
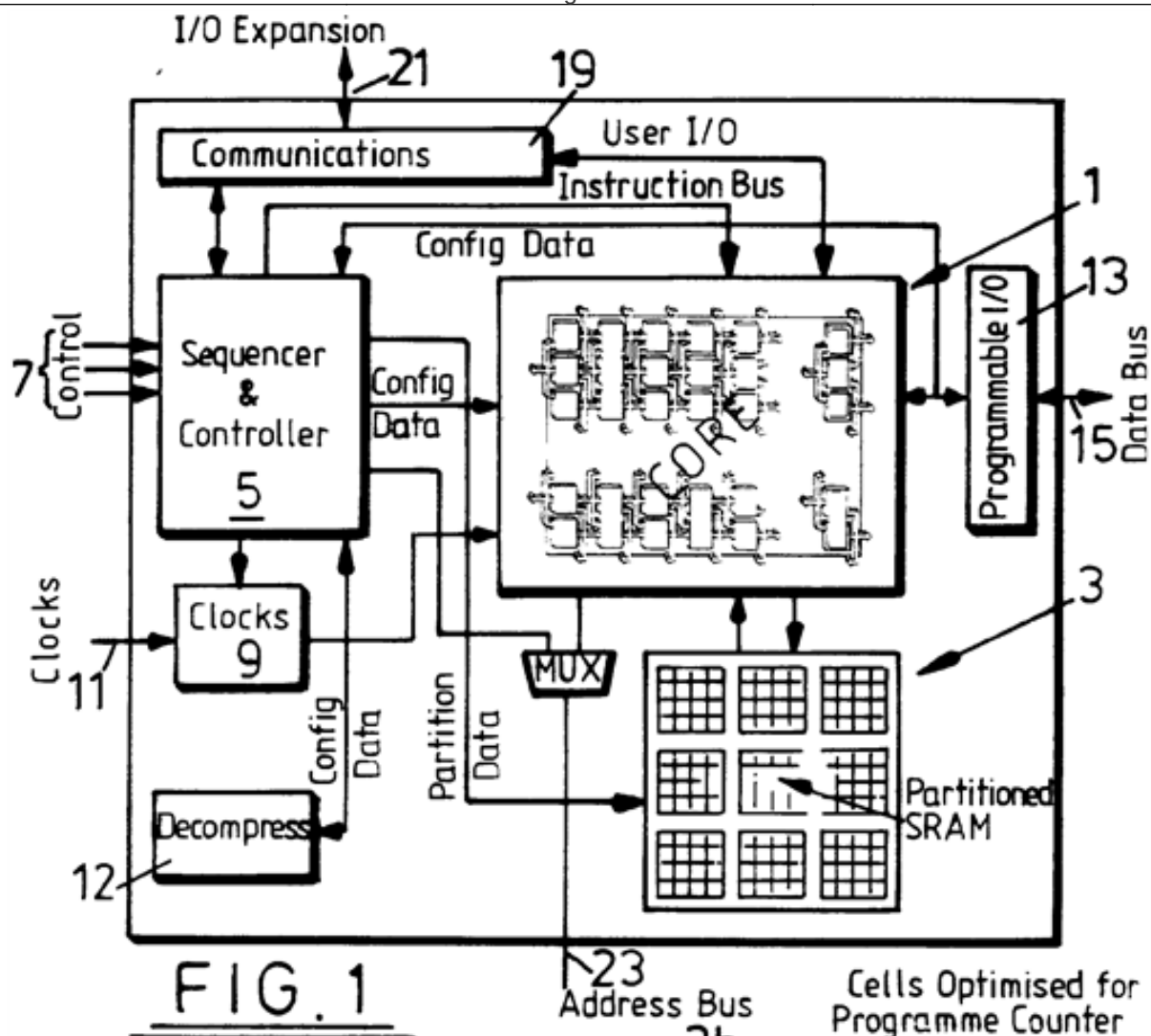
Family 16/20 - FAMPAT - ©Questel

Title

(EP-668659)

Reconfigurable ASIC.

Images



Publication numbers with kind code & date

TW357458
 RU95102140
 RU95102140

B 1999-05-01
 A 1997-01-10
 A1 1997-01-10

TW-357458
 RU95102140
 RU95102140



CN1126340	A	1996-07-10	CN1126340				
JP08101761	A	1996-04-16	JP08101761				
KR950034751	A	1995-12-28	KR19950034751				
BR9500680	A	1995-11-07	BR9500680				
AU1228695	A	1995-08-24	AU9512286				
EP0668659	A2	1995-08-23	EP-668659				
GB2286737	A	1995-08-23	GB2286737				
CA2142407	A1	1995-08-18	CA2142407				
BRPI9500680	A1	1995-04-11	BR9500680				
GB9503003	D0	1995-04-05	GB9503003				
GB9403030	D0	1994-04-06	GB9403030				

IPC - International classification

G06F-007/00; G06F-009/22; H01L-027/02; H01L-027/11; H03K-019/177

Abstract

(EP0668659)

A configurable semi-conductor integrated circuit, with particular application as a re-configurable application specific device. In order to be able to rapidly switch between two or more, preferably several, configurations, the invention provides a configurable semi-conductor integrated circuit in which an area (1) thereof is formed with a plurality of cells (2) each having at least one function and interconnections with at least some other said cells (2). At least some of the plurality of cells have interconnections (25) which are electrically selectable as to their conduction state, and at least some of the plurality cells have interconnections (YA-YD) which are pre-wired. Each cell has two or more possible configurations, each configuration being defined by the cell function and/or its interconnection with other cells according to cell configuration data, and further comprising means (36, 38, 40) storing configuration data for at least two cell configurations (per cell) and means (30, 32, 34, 42, 48) to enable one of the possible cell configurations according to the cell configuration data selected.

Inventors

AUSTIN KENNETH

Latest standardized assignees - inventors removed

PILKINGTON GERMANY NO 2

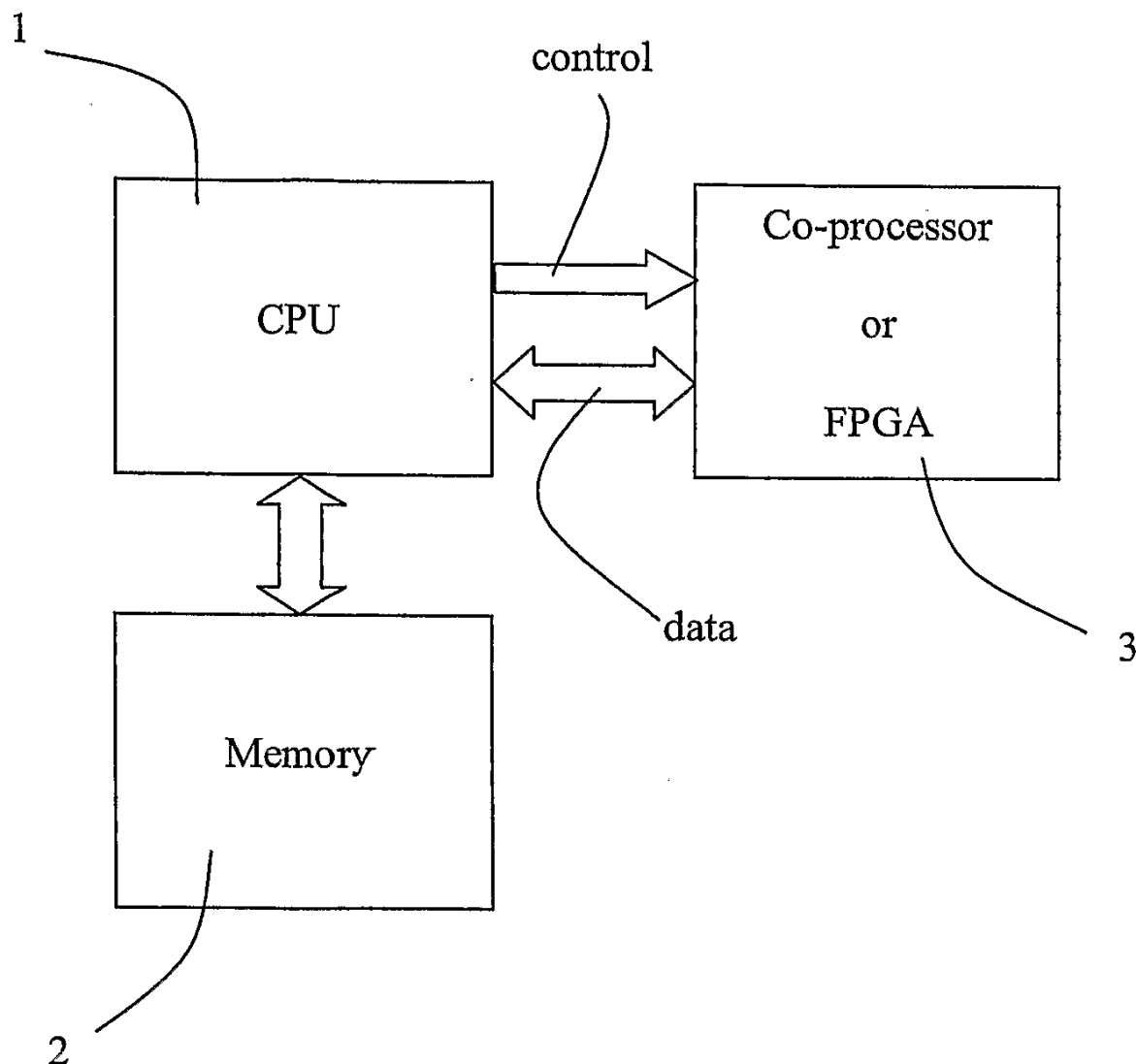
Family 17/20 - FAMPAT - ©Questel

Title

(WO200692556)

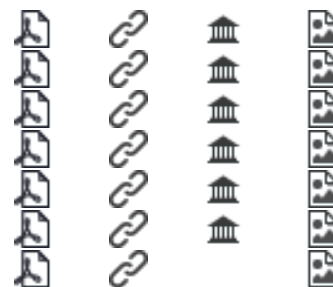
Reconfigurable logic in processors

Images



Publication numbers with kind code & date

JP2008532162	A	2008-08-14	JP2008532162
US20080189514	A1	2008-08-07	US20080189514
CN101133409	A	2008-02-27	CN101133409
WO2006/092556	A3	2006-12-21	WO200692556
WO2006/092556	A2	2006-09-08	WO200692556
GB2423840	A	2006-09-06	GB2423840
GB0504454	D0	2005-04-06	GB200504454



IPC - International classification

G06F-007/00; G06F-009/30; G06F-009/38; G06F-009/38; G06F-015/76; G06F-015/76; G06F-015/78; G06F-015/78; G06F-015/80; G06F-015/80

Abstract

(WO2006/092556)

A data processor comprises an array of processing elements (PEn 4), each element in the array comprising a respective configurable logic unit (CLU 11), whereby the logic capability of each processing element can be reconfigured at will. Memory (14, Figs 3, 4 not shown) may be pre-loaded with configuration instructions, whereby the configuration state of each processing element can be automatically sequenced from the pre-loaded memory. The memory may be global, in which case the CLUs may be reconfigured in parallel, to perform the same function. Alternatively, the memory may be local to each processing element so that different CLUs implement different functions. Configuration may be carried out under program control at a thread switch. Each respective processing element may select, at run time, a specific configuration from a number of configurations in a microcode store. The processor is preferably a SIMD processor.

Inventors

MCCONNELL RAYMOND MARK

Latest standardized assignees - inventors removed

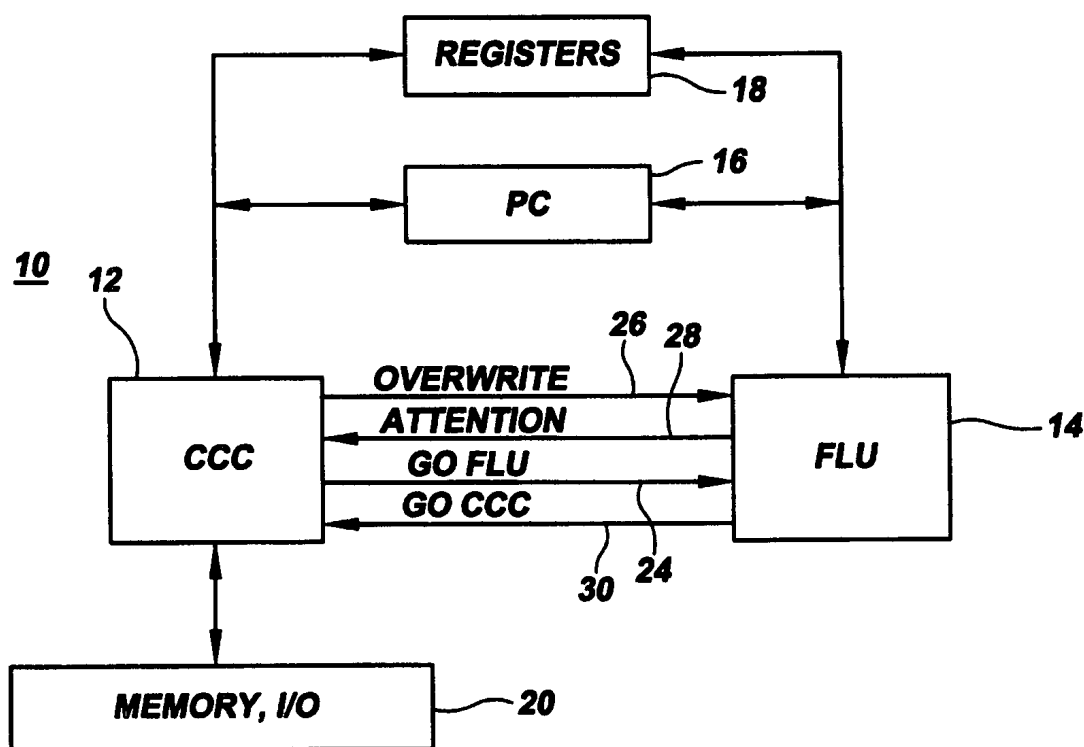
CLEAR SPEED TECHNOLOGY

Family 18/20 - FAMPAT - ©Questel

Title

(US7114062)

Processor which accelerates execution of binary programs intended for execution on a conventional processor core, using a reconfigurable combinational logic array, a function lookup unit, and a compatible conventional processor core, without requiring recompilation

Images**Publication numbers with kind code & date**[US7114062](#)

B2 2006-09-26

US7114062

[US20050149704](#)

A1 2005-07-07

US20050149704

**IPC - International classification**

G06F-009/00; G06F-009/318; G06F-009/38; G06F-009/42; G06F-009/45; G06F-015/16

Abstract

(US20050149704)

The invention uses a standard processor to execute an application program. As the instructions of the application program are executed in sequence, a program counter is incremented to contain an address indicator of the next instruction to be executed. The address indicator from the program counter is also fed to a function lookup unit where it is matched to the contents of a tag field. If there is no match, control returns to the processor which continues its normal sequence of operations and performs the function. If there is a match, function indicator identifiers from the function lookup table are fed to a reconfigurable combinational array which has logic functions. The function indicator identifiers select the logic function to be performed. The result of the performed function including the new program counter is then fed back to the processor. The processor then continues its normal operations.

Inventors

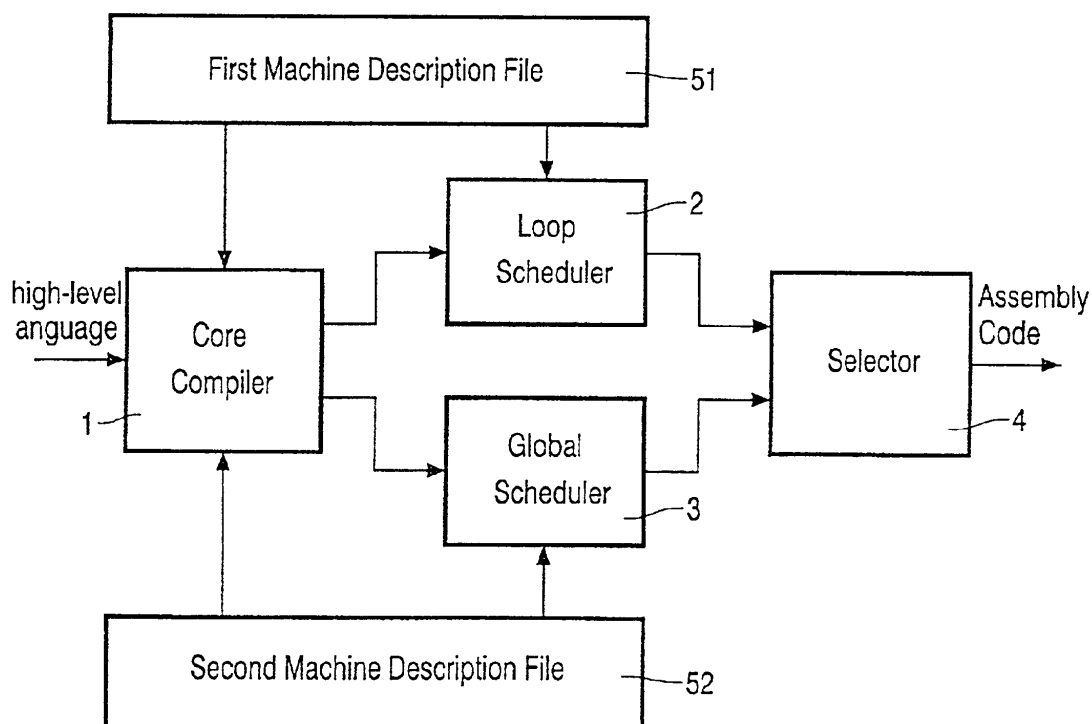
JOHNSON LUTHER A

Family 19/20 - FAMPAT - ©Questel

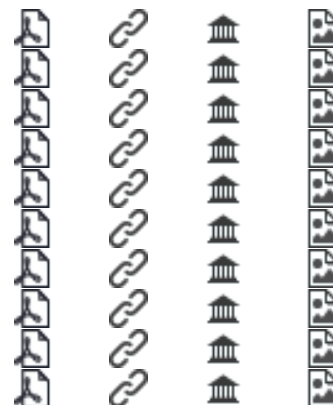
Title

(EP1417576)

Retargetable compiling system and method

Images**Publication numbers with kind code & date**

JP4979875	B2	2012-04-27	JP4979875
CN1296823	C	2007-01-24	CN1296823C
US6948158	B2	2005-09-20	US6948158
CN1518693	A	2004-08-04	CN1518693
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JP2004511043	A	2004-04-08	JP2004511043
WO02/29562	A3	2004-02-26	WO200229562
TW525091	B	2003-03-21	TW-525091
US20020042909	A1	2002-04-11	US20020042909
WO02/29562	A2	2002-04-11	WO200229562

**IPC - International classification**

G06F-008/41; G06F-008/41; G06F-009/38; G06F-009/45

Abstract

(EP1417576)

The present invention relates to a compiling method and system for generating a sequence of program instructions for use in a processing architecture with architecture resources executing instructions from a corresponding instruction set. A retargetable compiler is used to generate a code using at least two instruction sets in the same processing architecture. One instruction set for a compact code and one for a parallel high performance code. The compact instruction set (Compact Instruction Format) covers a subset (RF11, ALU1, L/S1, BU1) of the architecture, whereas the complete instruction set covers the entire architecture (RF1, UC1, UC2, RF2, UC3, UC4, RF3, UC5, UC6, RF4, UC7). By using the at least two instruction sets of different sizes, the compiler is able to reduce the processed average code length, since fewer bits are needed in the compact code to encode operations and registers.

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Latest standardized assignees - inventors removed

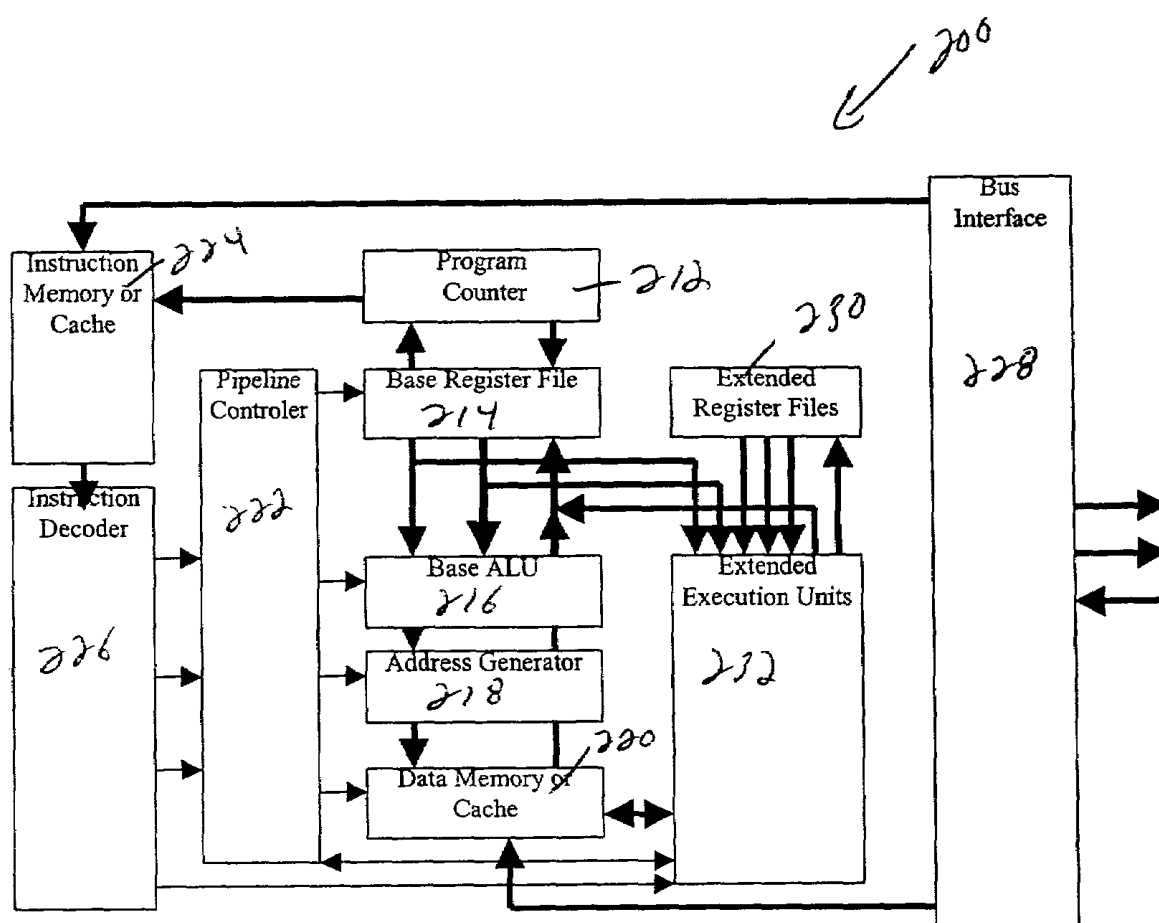
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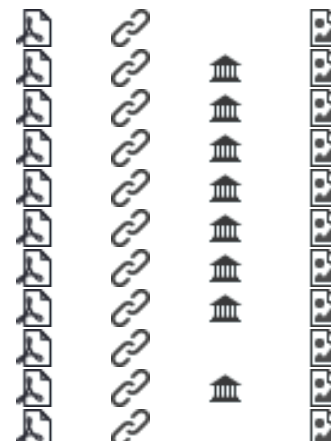
Title

(WO200388071)

High-performance hybrid processor with configurable execution units

Images**Publication numbers with kind code & date**

KR100998586	B1	2010-12-07	KR100998586
CN1653446	B	2010-05-05	CN1653446B
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AU2003222086	A1	2003-10-27	AU2003222086				
WO03/088071	A2	2003-10-23	WO200388071				

IPC - International classification

G06F-009/30; G06F-009/30; G06F-009/318; G06F-009/38; G06F-009/38; G06F-009/44; G06F-015/78; G06F-015/78; G06F-015/80; G06F-015/80; G06F-017/50; H03K-019/173

Abstract

(WO03/088071)

A new general method for building hybrid processors achieves higher performance in applications by allowing more powerful, tightly-coupled instruction set extensions to be implemented in reconfigurable logic. New set instructions can be discovered and designed by automatic and semi-automatic methods. Improved reconfigurable execution units support deep pipelining, addition of additional registers and register files, compound instructions with many source and destination registers and wide data paths. New interface methods allow lower latency, higher bandwidth connections between hybrid processors and other logic.

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