

Search query (1): [SP]: A reusable algorithmic pipelined core, comprising: a processing unit; an array of reconfigurable, field programmable gates, wherein the field programmable gates are programmed by an algorithmic matching pipelined compiler, such that the algorithmic matching pipelined compiler precompiles source code designed for operation on a standard processor without parallel processing for processing by the processing unit, and the processing unit and the algorithmic matching pipelined compiler configures the field programmable gates to operate as pipelined, parallel processors. 2. The core of claim 1, wherein the algorithmic matching pipelined compiler is a precompiler. 3. The core of claim 2, wherein the precompiler is configured to precompile a standard higher level software language written not for the core but for a type of conventional non-reconfigurable processor, and the precompiler generates machine code for the core by utilizing the type of conventional non-reconfigurable processor for which the standard higher level software language was written to generate machine code to configure the array of reconfigurable, field programmable gates. 4. The core of claim 3, wherein the standard higher level software language is C or C++. 5. The core of claim 2, wherein the core comprises a pool of computers configured to process algorithms as needed for a particular calculation, based on output from the precompiler. 5. The core of claim 1, wherein the field programmable gates are configured to complete tasks without any further overhead from the processing unit. 6. The core of claim 5, further comprising an intelligent bus controller or logical processor, wherein the intelligent bus controller or logical processor performs all of the logical functions processed by the core. 7. The core of claim 5, further comprising a logical processor and a master bus switch, and the logical processor comprises reconfigurable logic functions for controlling of the master bus switch. 8. The core of claim 7, further comprising a digital signal processor, wherein the digital signal processor comprises a reconfigurable mathematical processor for performing mathematical calculations. 9. The core of claim 8, wherein the master bus switch is a matrix bus router or switch comprising a circuit reconfigurably programmable by the precompiler and the processing unit, such that data and results are routed from the core to another core to complete an algorithm, without any further intervention from a central or peripheral processor during the processing of the algorithm, reducing overhead by pipelining compared to static, unconfigurable hardware, which requires intervention by a central processor or peripheral processor to direct data and results in and out of arithmetic processing units. 10. The core of claim 9, wherein the logical processor processes logical decisions and iterative loops and result memory is provided by the logical processor for learning algorithms. 11. A system comprising a plurality of the cores according to claim 1, comprising the steps of: processing all of the mathematical operations using digital signal processors of one or more of the plurality of cores; and processing all of the logic functions using one or more of the logic processors of one or more of the plurality of cores. 12. The system of claim 11, further comprising the step of configuring the plurality of cores as a pool of cores and each of the pool of cores are reconfigurable by programming, alone, without any change to the hardware. 13. The system of claim 12, wherein the step of configuring configures all of the plurality of cores to process algorithms in parallel without any further intervention from a central or peripheral processor to direct data and results in and out of arithmetic processing units. 14. The system of claim 13, wherein the algorithmic matching pipelined compiler is a precompiler, and the logic processor of each of the plurality of cores uses memory blocks configured by the precompiler, as look up tables and registers for constants or learned values. 15. The system of claim 14, further comprising setting up the look up table by the logic processor, wherein the look up table is an n-bit look up table, and the n-bit look up table is used to encode an n-bit Boolean logic function as truth tables. 16. The system of claim 11, further comprising: generating machine code from a standard higher level software language written for a conventional, non-reconfigurable and non-pipelined, general purpose computer processor, using the algorithmic matching pipelined compiler for one or more of the plurality of cores. 17. The system of claim 16, wherein the standard higher level software language is written for a type of conventional, non-reconfigurable processor, and the step of generating machine code comprises the algorithmic matching pipelined compiler, as a precompiler, utilizing the type of conventional, non-reconfigurable processor to generate machine code for configuring the array of reconfigurable, field programmable gates of each of the plurality of cores. 18. The system of claim 17, wherein the system comprises at least one processor of the type of conventional, non-reconfigurable processor for which the standard higher level software language is written, and the at least one processor of the type of conventional, non-reconfigurable processor for which the standard higher level software language is written generates the machine code for configuring the array of reconfigurable, field programmable gates of each of the plurality of cores. 19. The system of claim 18, wherein each of the plurality of cores is configured to independently solve complex mathematical and logic algorithms without further intervention by the at least one processor of the type of conventional, non-reconfigurable processor for which the standard higher level software language is written. 20. The system of claim 19, further comprising inputting values into the system, and the system outputs a solution to a master bus switch of the system, without further intervention. 21. The system of claim 20, wherein the plurality of cores comprises 2000 cores. 22. The system of claim 21, wherein the system operates 360 trillion instructions per second with a 500 MHz clock speed. 23. The system of claim 22, wherein the system has a latency for input of data, but pipelining reduces overhead such that the system is configured to execute a calculation and output a result on each clock from each core after the latency is initiated.

Results: 18

Search history

Search 1: [SP]: A reusable algorithmic pipelined core, comprising: a processing unit; an array of reconfigurable, field programmable gates, wherein the field programmable gates are programmed by an algorithmic matching pipelined compiler, such that the algorithmic matching pipelined compiler precompiles source code designed for operation on a standard processor without parallel processing for processing by the processing unit, and the processing unit and the algorithmic matching pipelined compiler configures the field programmable gates to operate as pipelined, parallel processors. 2. The core of claim 1, wherein the algorithmic matching pipelined compiler is a precompiler. 3. The core of claim 2, wherein the precompiler is configured to precompile a standard higher level software language written not for the core but for a type of conventional non-reconfigurable processor, and the precompiler generates machine code for the core by utilizing the type of conventional non-reconfigurable processor for which the standard higher level software language was written to generate machine code to configure the array of reconfigurable, field programmable gates. 4. The core of claim 3, wherein the standard higher level software language is C or C++. 5. The core of claim 2, wherein the core comprises a pool of computers configured to process algorithms as needed for a particular calculation, based on output from the precompiler. 5. The core of claim 1, wherein the field programmable gates are configured to complete tasks without any further overhead from the processing unit. 6. The core of claim 5, further comprising an intelligent bus controller or logical processor, wherein the intelligent bus controller or logical processor performs all of the logical functions processed by the core. 7. The core of claim 5, further comprising a logical processor and a master bus switch, and the logical processor comprises reconfigurable logic functions for controlling of the master bus switch. 8. The core of claim 7, further comprising a digital signal processor, wherein the digital signal processor comprises a reconfigurable mathematical processor for performing mathematical calculations. 9. The core of claim 8, wherein the master bus switch is a matrix bus router or switch comprising a circuit reconfigurably programmable by the precompiler and the processing unit, such that data and results are routed from the core to another core to complete an algorithm, without any further intervention from a central or peripheral processor during the processing of the algorithm, reducing overhead by pipelining compared to static, unconfigurable hardware, which requires intervention by a central processor or peripheral processor to direct data and results in and out of arithmetic processing units. 10. The core of claim 9, wherein the logical processor processes logical decisions and iterative loops and result memory is provided by the logical processor for learning algorithms. 11. A system comprising a plurality of the cores according to claim 1, comprising the steps of: processing all of the mathematical operations using digital signal processors of one or more of the plurality of cores; and processing all of the logic functions using one or more of the logic processors of one or more of the plurality of cores. 12. The system of claim 11, further comprising the step of configuring the plurality of cores as a pool of cores and each of the pool of cores are reconfigurable by programming, alone, without any change to the hardware. 13. The system of claim 12, wherein the step of configuring configures all of the plurality of cores to process algorithms in parallel without any further intervention from a central or peripheral processor to direct data and results in and out of arithmetic processing units. 14. The system of claim 13, wherein the algorithmic matching pipelined compiler is a precompiler, and the logic processor of each of the plurality of cores uses memory blocks configured by the precompiler, as look up tables and registers for constants or learned values. 15. The system of claim 14, further comprising setting up the look up table by the logic processor, wherein the look up table is an n-bit look up table, and the n-bit look up table is used to encode an n-bit Boolean logic function as truth tables. 16. The system of claim 11, further comprising: generating machine code from a standard higher level software language written for a conventional, non-reconfigurable and non-pipelined, general purpose computer processor, using the algorithmic matching pipelined compiler for one or more of the plurality of cores. 17. The system of claim 16, wherein the standard higher level software language is written for a type of conventional, non-reconfigurable processor, and the step of generating machine code comprises the algorithmic matching pipelined compiler, as a precompiler, utilizing the type of conventional, non-reconfigurable processor to generate machine code for configuring the array of reconfigurable, field programmable gates of each of the plurality of cores. 18. The system of claim 17, wherein the system comprises at least one processor of the type of conventional, non-reconfigurable processor for which the standard higher level software language is written, and the at least one processor of the type of conventional, non-reconfigurable processor for which the standard higher level software language is written generates the machine code for configuring the array of reconfigurable, field programmable gates of each of the plurality of cores. 19. The system of claim 18, wherein each of the plurality of cores is configured to independently solve complex mathematical and logic algorithms without further intervention by the at least one processor of the type of conventional, non-reconfigurable processor for which the standard higher level software language is written. 20. The system of claim 19, further comprising inputting values into the system, and the system outputs a solution to a master bus switch of the system, without further intervention. 21. The system of claim 20, wherein the plurality of cores comprises 2000 cores. 22. The system of claim 21, wherein the system operates 360 trillion instructions per second with a 500 MHz clock speed. 23. The system of claim 22, wherein the system has a latency for input of data, but pipelining reduces overhead such that the system is configured to execute a calculation and output a result on each clock from each core after the latency is initiated. (Results 18)

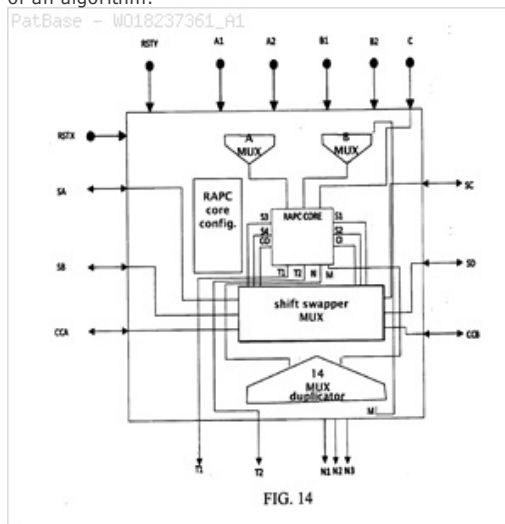
Title: HIGH THROUGHPUT PROCESSORS

Abstract: An algorithmic matching pipelined compiler and a reusable algorithmic pipelined core comprise a high throughput processor system. The reusable algorithmic pipelined core is a reconfigurable processing core with a pipelined structure comprising a processor with a setup interface for programming any of a plurality of operations as determined by setup data, a logic decision processor for programming a look up table, a loop counter and a constant register, and a block of memory. This can be used to perform functions. A reconfigurable, programmable circuit routes data and results from one core to another core and/or IO controller and/or interrupt generator, as required to complete an algorithm without further intervention from a central or peripheral processor during processing of an algorithm.

Classifications:

International (IPC 8-9): G06F7/38 (Advanced/Invention)

CPC: G06F15/7867 G06F7/38 H03K19/177

**Family:**

Publication number	Publication date	Application number	Application date
AU2018289605 AA	20181227	AU20180289605	20180622
CA3067827 AA	20191218	CA20183067827	20180622
CA3067827 AA	20181227	CA20183067827	20180622
WO18237361 A1	20181227	WO2018US39167	20180622

Priority:

US20170523528P 20170622 WO2018US39167 20180622

Probable Assignee: ICAT LLC

Assignee(s): (std): ICAT LLC

Assignee(s): ROIG DANIEL ; CATILLER ROBERT D ; ELUMALAI GNANASHANMUGAM

Inventor(s): (std): CATILLER ROBERT D ; ROIG DANIEL ; ELUMALAI GNANASHANMUGAM ; CATILLER ROBERT

Agent(s): IP GATEWAY PATENT AND TRADE MARK ATTORNEYS PTY LTD; CONNEELY PROFESSIONAL CORP; PARADIES CHRISTOPHER

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DJ DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JO JP KE KG KH KM KN KP KR KW KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: RECONFIGURABLE ARRAY TO COMPUTE DIGITAL ALGORITHMS

Abstract: An integrated circuit comprising a reconfigurable arrangement to compute digital algorithms by operating on digital data is described.

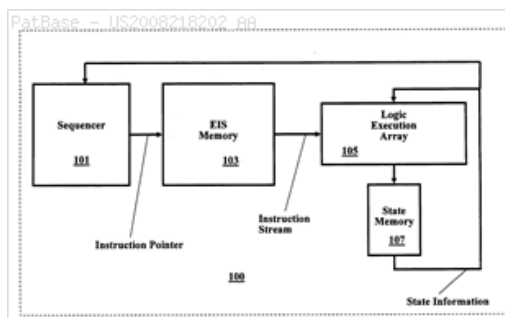
Classifications:

International (IPC 8-9): H03K19/173 (Advanced/Invention); H03K19/173 (Core/Invention)

CPC: H03K19/17758 H03K19/17736

European: H03K19/177F H03K19/177H7

US: 326/38 326/38P 326/47 708/232

**Family:**

Publication number	Publication date	Application number	Application date
US2008218202 AA	20080911	US20070004766	20071222

Agent(s): DONALD J LENKSZUS; LENKSZUS DONALD J; DONALD J

712/2271 712/229 712/38 712/37 7
712/E90.35S 716/117 716/16 718/1

Inventor(s): (std): CASSELMAN STEVEN ; CASSELMAN STEVEN MARK ; CASSELMAN STEVEN M

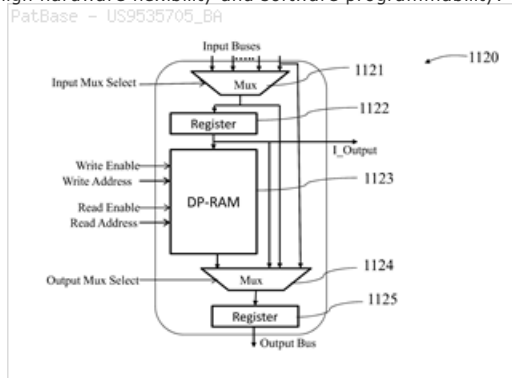
PatBase PDF Export - Page: 3 04/02/2020

inputs and outputs connected to MDDP-RAM blocks. The MDDP-RAM blocks provide the processing engine with different channels' data and coefficients. The processing engine and the MDDP-RAM blocks are controlled by a system processor (or other control scheme hardware) via the parameter blocks to enable high hardware flexibility and software programmability.

Classifications:

International (IPC 8-9): G06F9/30 G06F9/38 (Advanced/Invention)

CPC: G06F15/7867



Family:

Publication number	Publication date	Application number	Application date
US9535705 BA	20170103	US20140458972	20140813

Priority:

US20130865418P 20130813 US20140458972 20140813

Probable Assignee:

HAZANCHUK ASHER

Assignee(s): (std):

HAZANCHUK ASHER

Inventor(s): (std):

HAZANCHUK ASHER

Agent(s):

MASCHOFF BRENNAN

5) Family number: 28094092 (US2001032327A)

© PatBase

Title: SYSTEM AND METHOD OF PROCESSING MEMORY

Abstract: A method of processing memory, suitable for loading an executable object code compiled from a source code into the memory that includes defective memory cells. At first, set up a plurality of pre-compiled object codes that correspond to a source code, each pre-compiled object code having at least a skipped-code-address range. Then, test the memory and locate the defective addresses therein. According to the result of the test, the code-loading system selects an executable object that has the matching skipped-code-address range from the pre-compiled object codes, and loads the executable code into the memory. Since the skipped-code-address range covers the defective addresses in the memory, the defective memory cells in the memory won't affect the operation of loading a program.

Classifications:

International (IPC 8-9): G06F11/00 G06F11/273 G06F9/44

G11C29/00 (Advanced/Invention);

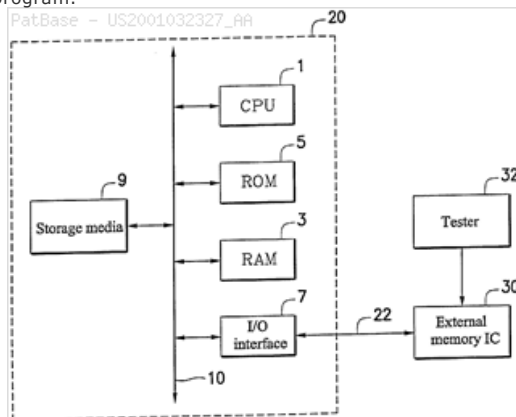
G06F11/00 G06F11/273 G06F9/44 G11C29/00 (Core/Invention)

International (IPC 1-7): G06F11/00 G06F9/44 G11C29/00

CPC: G06F11/1487 G06F11/2733

European: G06F11/14S2 G06F11/273E

US: 712/205 712/205S 714/6.13 714/723 714/723P 714/8 714/E11.171 714/E11.171S 717/124



Family:

Publication number	Publication date	Application number	Application date
TW463175 B	20011111	TW20000103568	20000301
US2001032327 AA	20011018	US20010821326	20010329
US6829722 BB	20041207	US20010821326	20010329

Priority:

TW20000103568 20000301

Probable Assignee:

WINBOND ELECTRONICS CORP

Assignee(s): (std):

WINBOND ELECTRONICS CORP

Inventor(s): (std):

LIN SHI TRON

6) Family number: 42998109 (US2011268137A)

© PatBase

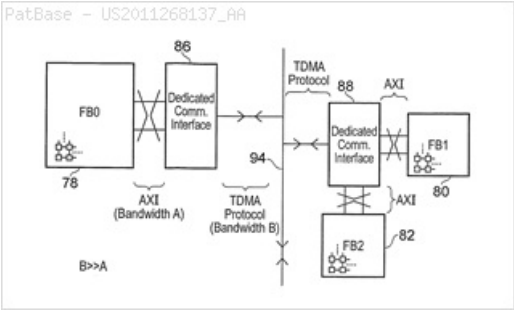
Title: COMMUNICATION WITHIN AN INTEGRATED CIRCUIT INCLUDING AN ARRAY OF INTERCONNECTED PROGRAMMABLE LOGIC ELEMENTS

Abstract: An integrated circuit includes an array of interconnected programmable logic elements (2) each logic element performing data processing control by a configuration. The logic elements may be part of a field programmable gate array. Embedded within the array are a plurality of dedicated communication interface circuits (36) providing access to one or more

shared communication channels (38) to provide intra-array communication. Communication transactions between functional unit (78, 80, 82, 84) are multiplexed (e.g. time-division-multiplexed) together to share a shared communication channel provided within the array.

Classifications:

International (IPC 8-9): H03K19/177 H04J1/00 H04J13/00 H04J3/00 H04J3/16 H04L27/00 (Advanced/Invention); H03K19/177 (Core/Invention)
CPC: H03K19/17736 H03K19/17732 H03K19/17744 H03K19/177
European: H03K19/177D4 H03K19/177F H03K19/177F4
US: 326/38 370/466 370/479 370/479P 370/480 370/480S 370/498 370/498S 375/259 375/259S



Family:

Publication number	Publication date	Application number	Application date
GB200900267 A0	20090211	GB20090000267	20090108
GB2466821 A1	20100714	GB20090000267	20090108
US2011268137 AA	20111103	US20100138109	20100106
US8675681 BB	20140318	US20100138109	20100106
WO10079326 A2	20100715	WO2010GB00012	20100106
WO10079326 A3	20100902	WO2010GB00012	20100106

Priority:

GB20090000267 20090108 WO2010GB00012 20100106

Probable Assignee: ARM LTD

Assignee(s): (std): ADVANCED RISC MACH LTD ; HILL STEPHEN JOHN ; MULLER MICHAEL PETER

Assignee(s): ARM LIMITED ; ARM LTD

Inventor(s): (std): MULLER MICHAEL PETER ; HILL STEPHEN JOHN

Inventor(s): STEPHEN JOHN HILL ; MICHAEL PETER MULLER

Agent(s): NIXON AND VANDERHYTE PC; ROBINSON NIGEL ALEXANDER JULIAN ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

7) Family number: 34501126 (US2007241772A)

© PatBase

Title: EMBEDDING MEMORY WITHIN TILE ARRANGEMENT OF A CONFIGURABLE IC

Abstract: Some embodiments of the invention provide a configurable IC that includes several configurable computational tiles and several memory tiles. Each computational tile has a set of configurable logic circuits for configurably performing a plurality of computations and a set of configurable routing circuits. The routing circuits of the tiles configurably route signals between configurable logic circuits. Each memory tile includes a set of routing circuits and a memory array for storing data on which the logic circuit perform computation. In this IC, at least a first memory tile has the same set of configurable routing circuits as at least a second computational tile.

Classifications:

International (IPC 8-9): G06F7/38 G06F7/48 G06F7/50 G06F7/506 H01L25/00 H03K19/0175 H03K19/173 H03K19/177 (Advanced/Invention); G06F7/38 G06F7/48 H01L25/00 H03K19/173 H03K19/177 (Core/Invention)

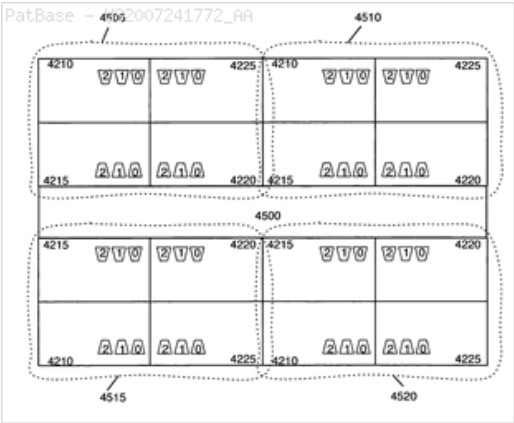
CPC: H01L2924/01019 H01L25/18 H01L2224/32145 H01L2224/48091 H01L2224/48227 H01L2224/73265 H01L2225/0651 H01L2924/15311 H01L2924/16152 H01L27/0207 H01L27/11803 H01L27/11898 H01L2224/32225 H03K19/173 H01L24/73 G06F2207/3868 H01L2924/14 G06F7/506 H03K19/1774 H03K19/17748 G11C5/025 H03K19/17736 H03K19/1776 H01L25/065 H03K19/17796 H03K19/17732 H03K19/17752 H01L25/0657 H03K19/17728 H03K19/17704 H03K19/17758 H03K19/17756

European: G06F7/506 G11C5/025 H01L25/065 H01L25/065S H01L25/18 H01L27/02B2 H01L27/118G H01L27/118P H03K19/177B H03K19/177D2 H03K19/177D4 H03K19/177F H03K19/177F2 H03K19/177H H03K19/177H1 H03K19/177H2 H03K19/177H3 H03K19/177H7 H03K19/177J8 S06F207/38A6B S06F7/506 T01L224/32145 T01L224/48091 T01L224/48227 T01L224/73265 T01L225/065S15 T01L924/15311 T01L924/16152

US: 1/1 257/E25.01 257/E25.010S 257/E25.013 257/E25.013S 257/E27.107 257/E27.107S 257/E27.11 257/E27.110S 326/113 326/37 326/38 326/38P 326/39 326/40 326/40P 326/41 326/41P 326/41S 326/46 326/46P 326/47 327/57 365/189.02 365/230.02 708/230 708/232 708/233 708/233P 708/700 708/700P 708/710 716/117 716/126 716/16

Family:

Publication number	Publication date	Application number	Application date
US2007241772 AA	20071018	US20050081867	20050315
US2007241774 AA	20071018	US20050082196	20050315
US2007241775 AA	20071018	US20050082203	20050315
US2007241778 AA	20071018	US20070733158	20070409
US2007241780 AA	20071018	US20050081877	20050315
US2007241782 AA	20071018	US20050081859	20050315
US2007241783 AA	20071018	US20050082193	20050315
US2007241785 AA	20071018	US20050082228	20050315



US2007244957 AA	20071018	US20050081878	20050315
US2007244958 AA	20071018	US20050082219	20050315
US2007244960 AA	20071018	US20050082222	20050315
US2007244961 AA	20071018	US20050082225	20050315
US2007285124 AA	20071213	US20070757982	20070604
US2007285125 AA	20071213	US20070781224	20070720
US2008018359 AA	20080124	US20070775218	20070709
US2008030227 AA	20080207	US20070871944	20071012
US2008036494 AA	20080214	US20070840963	20070818
US2008061823 AA	20080313	US20070856214	20070917
US2008100339 AA	20080501	US20070868959	20071008
US2008116931 AA	20080522	US20070926092	20071028
US2008164906 AA	20080710	US20070963771	20071221
US2008180131 AA	20080731	US20080021291	20080128
US2010007376 AA	20100114	US20090498356	20090706
US2010194429 AA	20100805	US20090644008	20091221
US2011031998 AA	20110210	US20100781789	20100517
US2011115523 AA	20110519	US20100901487	20101008
US2011202586 AA	20110818	US20100949775	20101118
US2012262201 AA	20121018	US20120424364	20120319
US2013038347 AA	20130214	US20120550589	20120716
US2015054546 AA	20150226	US20140222548	20140321
US2015137851 AA	20150521	US20140311359	20140623
US7224181 BA	20070529	US20050082201	20050315
US7242216 BA	20070710	US20050081809	20050315
US7259587 BA	20070821	US20050081861	20050315
US7268586 BA	20070911	US20050082230	20050315
US7276933 BA	20071002	US20050082196	20050315
US7282950 BA	20071016	US20050082228	20050315
US7295037 BB	20071113	US20050082193	20050315
US7301368 BB	20071127	US20050081867	20050315
US7317331 BB	20080108	US20050081877	20050315
US7330050 BB	20080212	US20050082203	20050315
US7342415 BB	20080311	US20050081859	20050315
US7420389 BB	20080902	US20070733158	20070409
US7518402 BB	20090414	US20070775218	20070709
US7525342 BB	20090428	US20070840963	20070818
US7532030 BB	20090512	US20070781224	20070720
US7545167 BB	20090609	US20080021291	20080128
US7564261 BB	20090721	US20070757982	20070604
US7570077 BB	20090804	US20070963771	20071221
US7573296 BB	20090811	US20050082225	20050315
US7576564 BB	20090818	US20070868959	20071008
US7652499 BB	20100126	US20070926092	20071028
US7656188 BB	20100202	US20070871944	20071012
US7743085 BB	20100622	US20050082222	20050315
US7825687 BB	20101102	US20090498356	20090706
US7839166 BB	20101123	US20070856214	20070917
US7917559 BB	20110329	US20050081878	20050315
US8159264 BB	20120417	US20100901487	20101008
US8183882 BB	20120522	US20090644008	20091221
US8248102 BB	20120821	US20100781789	20100517
US8350591 BB	20130108	US20100949775	20101118
US8698518 BB	20140415	US20120424364	20120319
US8797062 BB	20140805	US20120550589	20120716
US9048833 BB	20150602	US20140222548	20140321
US9489175 BB	20161108	US20140311359	20140623

Priority:

US20040883502	20040630	US20040626322P	20041108	US20050081809	20050315
US20050081859	20050315	US20050081867	20050315	US20050081861	20050315
US20050081878	20050315	US20050082219	20050315	US20050082196	20050315
US20050082203	20050315	US20050082193	20050315	US20050082201	20050315
US20050082222	20050315	US20050081877	20050315	US20050082225	20050315
US20050082228	20050315	US20050082230	20050315	US20070733158	20070409
US20070757982	20070604	US20070775218	20070709	US20070781224	20070720
US20070840963	20070818	US20070856214	20070917	US20070868959	20071008
US20070871944	20071012	US20070926092	20071028	US20070963771	20071221
US20080021291	20080128	US20090498356	20090706	US20090644008	20091221
US20100781789	20100517	US20100901487	20101008	US20100949775	20101118
US20120424364	20120319	US20120550589	20120716	US20140222548	20140321
US20140311359	20140623				

Probable Assignee: ALTERA CORP

Assignee(s): (std): ALTERA CORP ; CHANDRA VIKAS ; HUANG RANDY R ; HUTCHINGS BRAD ; HUTCHINGS BRAD L ; REDGRAVE JASON ; SCHMIT HERMAN ; TEIG STEVEN ; TABULA INC

Assignee(s): TABULA ASSIGNMENT FOR BENEFIT OF CREDITORS LLC

Inventor(s): (std): REDGRAVE JASON ; SCHMIT HERMAN ; CHANDRA VIKAS ; HUANG RANDY R ; HUTCHINGS BRAD L ; HUANG RANDY RENFU ; HUTCHINGS BRAD ; TEIG STEVEN

Inventor(s): HUANG RANDY

Agent(s): ADELI LAW GROUP A PROFESSIONAL LAW CORP; ADELI AND TOLLEN LLP; STATTLER JOHANSEN AND ADELI LLP; ADELI LAW GROUP; ADELI LAW GROUP PLC; ADELI LLP

Title: TRANSFERRING DATA IN A PARALLEL PROCESSING ENVIRONMENT

Abstract: An integrated circuit includes a plurality of tiles. Each tile includes a processor, a switch including switching circuitry to forward data over data paths from other tiles to the processor and to switches of other tiles, and a switch memory that stores instruction streams that are able to operate independently for respective output ports of the switch.

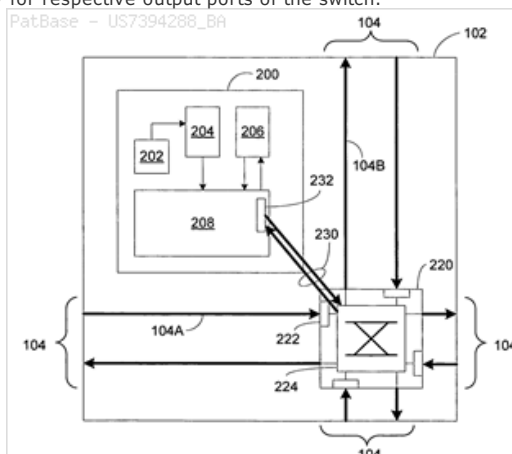
Classifications:

International (IPC 8-9): G06F13/32 G06F13/00 G06F13/14 G06F15/00 G06F15/76 G06F15/80 G06F17/50 G06F7/38 G06F9/45 H03K17/693 H03K19/00 H03K19/177 H04L12/50 H04Q11/00 (Advanced/Invention); G06F13/32 G06F13/14 G06F15/76 G06F17/50 G06F7/38 H03K17/693 H03K19/00 H03K19/177 (Core/Invention)

CPC: G06F15/8007 G06F15/17381 G06F15/7867 H03K19/177 H03K19/17704 G06F9/30123 G06F9/30189 G06F9/3851 Y02D10/12 Y02D10/13

European: G06F15/78R H03K19/177 H03K19/177B

US: 326/38 326/39 326/41 326/47 345/505 345/519 370/386 710/316 712/10 712/11 712/13 712/28 712/29 712/30 713/300 713/323 713/324 716/112 716/114 716/116 716/16 716/17 717/140 717/149 717/159

**Family:**

Publication number	Publication date	Application number	Application date
US7394288 BA	20080701	US20050302984	20051213
US7622949 BA	20091124	US20080130462	20080530
US7635987 BA	20091222	US20050302983	20051213
US7673164 BA	20100302	US20050300649	20051213
US7804504 BA	20100928	US20050302962	20051213
US8155113 BA	20120410	US20050302961	20051213
US8745604 BA	20140603	US20080036573	20080225

Priority:

US20040635546P	20041213	US20040636166P	20041214	US20050302983	20051213
US20050300649	20051213	US20050302962	20051213	US20050302961	20051213
US20050302984	20051213	US20080036573	20080225	US20080130462	20080530

Probable Assignee: MASSACHUSETTS INST OF TECHNOLOGY

Assignee(s): (std): AGARWAL ANANT ; MASSACHUSETTS INST TECHNOLOGY

Assignee(s): MASSACHUSETTS INSTITUTE OF TECHNOLOGY ; MASSACHUSETTS INST ; MASSACHUSETTS INST OF TECHNOLOGY ; MASSACHUSETTS INST OF TECHNOLOGY

Inventor(s): (std): AGARWAL ANANT

Agent(s): FISH AND RICHARDSON PC

Title: METHOD AND APPARATUS FOR AUTOMATICALLY GENERATING HARDWARE FROM ALGORITHMS DESCRIBED IN MATLAB

Abstract: Digital circuit is synthesized from algorithm described in the MATLAB programming language. A MATLAB program is compiled into RTL-VHDL, which is synthesizable using system-specific tools to develop ASIC or FPGA configuration.

Intermediate transformations and optimizations are performed to obtain highly optimized description in RTL-VHDL or RTL Verilog of given MATLAB program. Optimizations include levelization, scalarization, pipelining, type-shape analysis, memory optimizations, precision analysis and scheduling.

Classifications:

International (IPC 8-9): G06F17/50 G06F9/45 (Advanced/Invention); G06F17/50 G06F9/45 (Core/Invention)

International (IPC 1-7): G06F9/45

CPC: G06F30/30 G06F8/4434 G06F8/445

European: G06F17/50D G06F8/4434 G06F8/445

US: 716/103 716/104 716/18 716/3 716/4 717/140 717/141 717/15 717/150 717/150S 717/152 717/152P 717/159 717/159S

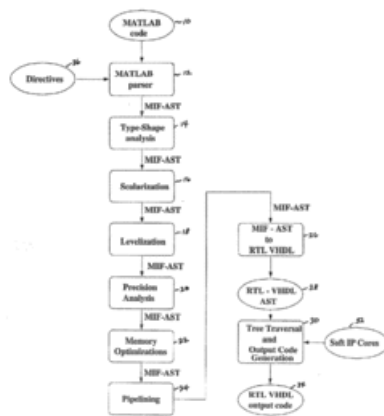


Figure 1: Synthesis flow.

Family:

Publication number	Publication date	Application number	Application date
US2004019883 AA	20040129	US20010770541	20010126
US7000213 BB	20060214	US20010770541	20010126

Priority:

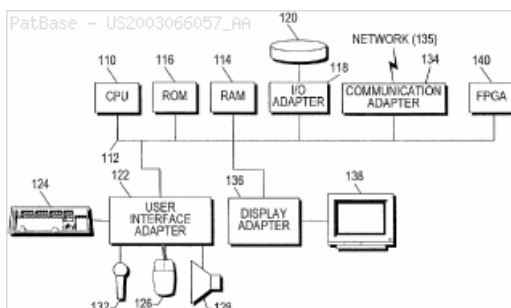
US20010770541 20010126

Probable Assignee: NORTHWESTERN UNIV**Assignee(s):** (std): UNIV NORTHWESTERN**Assignee(s):** AIR FORCE UNITED STATES ; NORTHWESTERN UNIV ; NORTHWESTERN UNIVERSITY**Inventor(s):** (std): BANERJEE PRITHVIRAJ ; CHOUDHARY ALOK ; HALDAR MALAY ; NAYAK ANSHUMAN**Agent(s):** LAW OFFICE OF DEEPTI PANCHAWAGH JAIN**10) Family number: 28437360 (US2003066057A)**

© PatBase

Title: SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR COLLABORATIVE HARDWARE DESIGN

Abstract: A system, method and article of manufacture are provided for providing one or more modules conforming to a hardware design specification. A user specification for at least a portion of a hardware design is received. One or more modules conforming to the specification are identified. The module(s) are retrieved and sent to the user. The module can be used to configure a configurable hardware device.

Classifications:**International (IPC 8-9):** G06F17/50 G06F9/45 (Advanced/Invention); G06F17/50 G06F9/45 (Core/Invention)**International (IPC 1-7):** G06F9/45**CPC:** G06F30/30 G06F30/327 G06F30/34 G06F2111/02**European:** G06F17/50D G06F17/50D2 G06F17/50D4**US:** 717/140**Family:**

Publication number	Publication date	Application number	Application date
US2003066057 AA	20030403	US20010791456	20010223

Priority:

US20010791456 20010223

Probable Assignee:

RUDUSKY DARYL

Assignee(s): (std):

RUDUSKY DARYL

Inventor(s): (std):

RUDUSKY DARYL

11) Family number: 44150449 (US2009320008A)

© PatBase

US19790052350 19790627 US19810240880 19810305
Probable Assignee: UNISYS CORP
Assignee(s): (std): BURROUGHS CORP
Assignee(s): UNISYS CORP ; BURROUGHS A CORP OF MI CORP
Inventor(s): (std): CATILLER ROBERT D ; FORBES BRIAN K

13) Family number: 28281627 (US2002157082A)

© PatBase

Title: INTER-DICE WAFER LEVEL SIGNAL TRANSFER METHODS FOR INTEGRATED CIRCUITS

Abstract: The present invention discloses novel methods to transfer data between a plurality of integrated circuit dice on a semiconductor wafer. Each individual die contains internal circuits to control data transfer to nearby dice. Wafer level data transfer is achieved by a series of inter-dice data transfers. It is therefore possible to use a small number of small area metal lines to support wafer level parallel processing activities. External connections are provided by a small number of bonding pads on each wafer. The load on each external bounding pad is by far lower than that of prior art wafer level connections. These inter-dice data transfer mechanism also can be programmed to avoid defective circuitry. This invention has been used to support wafer level functional tests and wafer level burn-in tests. A Testing system of the present invention can test thousands of dice in parallel using simple testing equipment. Testing costs for integrated circuits are therefore reduced dramatically. The present application also makes it possible to build large area IC containing multiple dice. Extremely powerful products are realized using parallel processing capability of such multiple die integrated circuits.

Classifications:

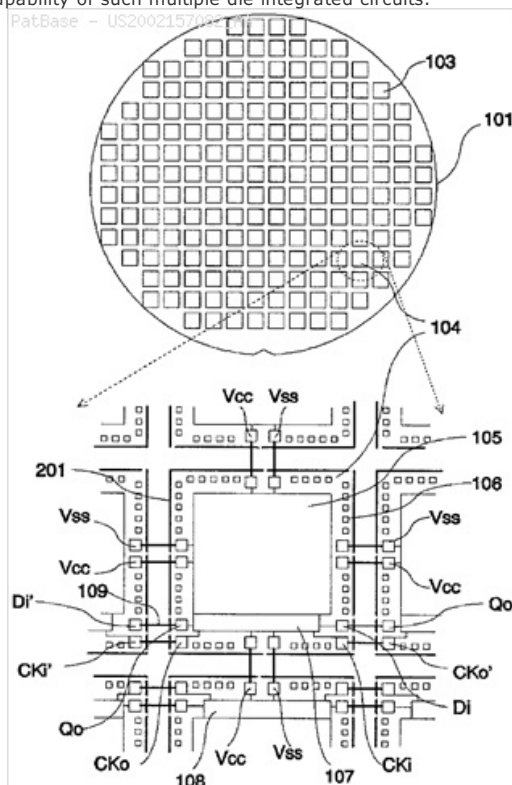
International (IPC 8-9): G01R31/28 G01R31/3185 G11C8/00
H01L23/48 H01L23/58 H01L29/40 (Advanced/Invention);
G01R31/28 H01L23/58 (Core/Invention)

International (IPC 1-7): G06F17/50 H01L23/58

CPC: G01R31/2831 G01R31/2856 G01R31/2884 H01L22/32
H01L2223/5448 H01L2924/3011 H01L2224/05554 H01L2224/0603
H01L2924/0002 G01R31/318511 G01R31/318505

European: G01R31/28G2 G01R31/28G2A G01R31/3185M
G01R31/3185M3 H01L22/32 H01L23/58T S01R31/28E11
S01R31/28G4 T01L223/544H2 T01L924/30110

US: 257/48 257/620 257/690 257/690P 257/734 257/734P 257/786
257/E21.521 257/E21.524 365/230.03 365/230.030S 438/18 716/12
716/19 716/4 716/5 716/50 716/50P



Family:

Publication number	Publication date	Application number	Application date
AU2002312430 AA	20031020	AU20020312430	20020610
US2002157082 AA	20021024	US20020115836	20020402
US2005151248 AA	20050714	US20050040921	20050121
US2006081971 AA	20060420	US20050163564	20051023
US6427222 BA	20020730	US19970941786	19970930
US7161175 BB	20070109	US20050040921	20050121
WO03085563 A1	20031016	WO2002US18324	20020610

Priority:

US19970941786 19970930 US19980115836 19980715 US20020115836 20020402
WO2002US18324 20020610 US20050040921 20050121 US20050163564 20051023

Probable Assignee: ALPHA OMEGA SEMICONDUCTOR LTD

Assignee(s): (std): ALPHA OMEGA SEMICONDUCTOR LTD ; SHAU JENG JYE

Assignee(s): ALPHA OMEGA SEMICONDUCTOR LIMITED

Inventor(s): (std): SHAU JENG JYE

Agent(s): BO-IN LIN; BO IN LIN; JENG JYE SHAU

Designated states: AE AM AT AU AZ BE BG BR BY BZ CA CH CN CO CR CY CZ DE DK DM EC EE ES FI FR GB GR HU ID IE
IL IN IS IT JP KG KP KR KZ LK LU MC MD MN MX NL NO NZ PH PL PT RO RU SE SG TJ TM TR UA VN YU
ZA

14) Family number: 31767631 (US2003018630A)

© PatBase

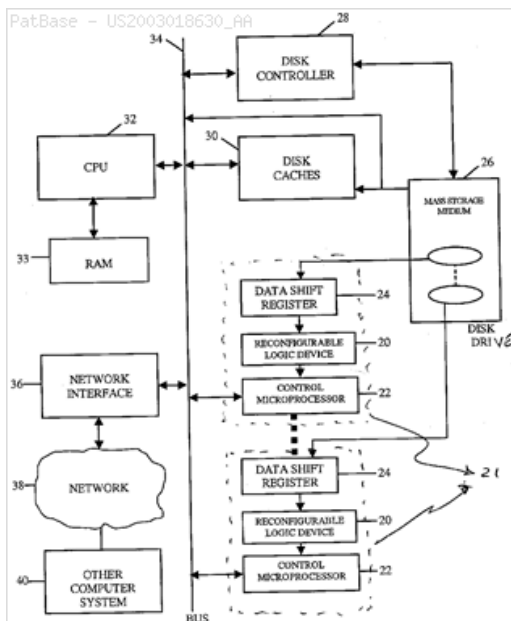
Title: ASSOCIATIVE DATABASE SCANNING AND INFORMATION RETRIEVAL USING FPGA DEVICES

Classifications:

International (IPC 1-7): G06F1/00 G06F1/730 G06F11/00 G06F15/78
G06F17/15 G06F17/30 G06F3/06 G06F7/00 G06T1/20

European: G06F17/30A G06F17/30E2A G06F17/30E2P G06F17/30H
G06F17/30S G06F17/30S4P4 G06F17/30Z2P3 G06F17/30Z2P5
G06F21/60A G06F21/72 G06F21/76 G06F21/85 G06F3/06A2P
G06F3/06A4T G06F3/06A6D G06F3/06A6L4 G06Q40/00 G06Q40/06
S06F3/06A S06F3/06D

US: 1/1 1/1P 705/35 705/35S /05/36.00RP 705/36R 707/1 707/10
707/200 707/3 707/6 707/636 707/690 707/690S 707/693 707/693P
707/693S 707/705 707/706 707/712 707/758 707/758P 707/797
707/812 707/823 707/825 707/999.001 707/999.001S 707/999.003
707/999.003S 707/999.006 707/999.006S 707/999.01 707/999.2 707/E1.001 707/E1.001S 707/E1.002 707/E1.002S
707/E1.005 707/E1.005S 707/E1.009 707/E1.009S 707/E1.01 707/E1.010S 707/E1.014 707/E1.014S 707/E1.017
707/E1.017S 707/E1.032 707/E1.032S 707/E1.039 707/E1.039S 707/E1.04 707/E1.040S 707/E1.058 707/E1.058S
707/E1.135 707/E1.135S 709/201 709/201S 709/225 711/1 711/112 712 711/4 712/207 712/207S 712/221 712/E9.047
712/E9.047S 713/100 713/100P 713/171 713/171P 714/746 714/746S 714/E11.021 714/E11.021S 718/102



Family:

Publication number	Publication date	Application number	Application date
AT411563 E	20081015	AT20010930450T	20010406
AU2001256986 AA	20011030	AU20010256986	20010406
AU2001256986 BB	20070614	AU20010256986	20010406
AU2001256986 CA	20080306	AU20010256986	20010406
AU200156986 A1	20011030	AU20010056986	20010406
AU200156986 A5	20011030	AU20010056986	20010406
AU2003233564 AA	20031212	AU20030233564	20030515
AU2003233564 BB	20080717	AU20030233564	20030515
AU2004273406 AA	20050324	AU20040273406	20040521
AU2004290281 AA	20050526	AU20040290281	20040521
AU2009200148 AA	20090219	AU20090200148	20090114
AU2009200148 BB	20120809	AU20090200148	20090114
CA2405464 AA	20021007	CA20012405464	20010406
CA2405464 C	20120103	CA20012405464	20010406
CA2486359 AA	20041109	CA20032486359	20030515
CA2486359 C	20121120	CA20032486359	20030515
CA2522862 AA	20051018	CA20042522862	20040521
CA2523548 AA	20051024	CA20042523548	20040521
CA2523548 C	20140204	CA20042523548	20040521
CA2755373 AA	20011025	CA20012755373	20010406
CA2755373 C	20140909	CA20012755373	20010406
CA2759064 AA	20050324	CA20042759064	20040521
CA2759064 C	20170404	CA20042759064	20040521
CA2836758 AA	20050526	CA20042836758	20040521
CA2836758 C	20170627	CA20042836758	20040521
DE60136224 D1	20081127	DE20016036224	20010406
DE602004051597 D1	20170907	DE200460051597T	20040521
DE602004051836 D1	20171102	DE200460051836T	20040521
EP1368750 A2	20031210	EP20010930450	20010406
EP1368750 B1	20081015	EP20010930450	20010406
EP1506501 A2	20050216	EP20030729000	20030515
EP1627284 A2	20060222	EP20040752943	20040521
EP1627284 B1	20181024	EP20040752943	20040521
EP1627331 A2	20060222	EP20040753259	20040521
EP1627331 B1	20170920	EP20040753259	20040521
EP2511787 A1	20121017	EP20120165819	20040521
EP2511787 B1	20170920	EP20120165819	20040521
EP2528000 A1	20121128	EP20120165559	20040521
EP2528000 B1	20170726	EP20120165559	20040521
EP3560135 A1	20191030	EP20170883314	20171220
JP2004502996 T2	20040129	JP20010577212T	20010406

JP2005527043 T2	20050908	JP20040508044T	20030515
JP2006526227 T2	20061116	JP20060514919T	20040521
JP2007524923 T2	20070830	JP20060533393T	20040521
JP2012014705 A2	20120119	JP20110156373	20110715
JP5439651 B2	20140312	JP20110156373	20110715
US2003018630 AA	20030123	US20020153151	20020521
US2004111392 AA	20040610	US20030722691	20031124
US2006294059 AA	20061228	US20040550323	20040521
US2007078837 AA	20070405	US20060561615	20061120
US2007118500 AA	20070524	US20070621001	20070108
US2007277036 AA	20071129	US20040550326	20040521
US2008109413 AA	20080508	US20070932391	20071031
US2008114760 AA	20080515	US20070932434	20071031
US2008126320 AA	20080529	US20070932596	20071031
US2008133453 AA	20080605	US20070932652	20071031
US2008133519 AA	20080605	US20070932321	20071031
US2011252008 AA	20111013	US20110165155	20110621
US2012109849 AA	20120503	US20120345011	20120106
US2012110316 AA	20120503	US20120344986	20120106
US2012116998 AA	20120510	US20110301387	20111121
US2012130922 AA	20120524	US20110301340	20111121
US2012215801 AA	20120823	US20120410997	20120302
US2014025656 AA	20140123	US20130039128	20130927
US2014310717 AA	20141016	US20140315560	20140626
US2016070583 AA	20160310	US20150929791	20151102
US2017102950 AA	20170413	US20160388498	20161222
US2018157504 AA	20180607	US20180882679	20180129
US2019324770 AA	20191024	US20190503244	20190703
US6711558 BA	20040323	US20000545472	20000407
US7139743 BB	20061121	US20020153151	20020521
US7181437 BB	20070220	US20030722691	20031124
US7552107 BB	20090623	US20070621001	20070108
US7680790 BB	20100316	US20070932321	20071031
US7949650 BB	20110524	US20070932652	20071031
US7953743 BB	20110531	US20070932391	20071031
US8069102 BB	20111129	US20060561615	20061120
US8095508 BB	20120110	US20040550323	20040521
US8131697 BB	20120306	US20070932596	20071031
US8549024 BB	20131001	US20120410997	20120302
US8620881 BB	20131231	US20110165155	20110621
US8751452 BB	20140610	US20120345011	20120106
US8768888 BB	20140701	US20120344986	20120106
US9020928 BB	20150428	US20130039128	20130927
US9176775 BB	20151103	US20140315560	20140626
US9898312 BB	20180220	US20150929791	20151102
US10346181 BB	20190709	US20180882679	20180129
WO0180082 A2	20011025	WO2001US11255	20010406
WO0180082 A3	20030918	WO2001US11255	20010406
WO0180082 C1	20020103	WO2001US11255	20010406
WO03100662 A2	20031204	WO2003US15638	20030515
WO03100662 A3	20040624	WO2003US15638	20030515
WO05026925 A2	20050324	WO2004US16021	20040521
WO05026925 A3	20051006	WO2004US16021	20040521
WO05048134 A2	20050526	WO2004US16398	20040521
WO05048134 A3	20050804	WO2004US16398	20040521
WO18119035 A1	20180628	WO2017US67515	20171220

Priority:

US20000545472	20000407	CA20012405464	20010406	CA20012755373	20010406
WO2001US11255	20010406	US20020153151	20020521	AU20030233564	20030515
WO2003US15638	20030515	US20030473077P	20030523	US20030722691	20031124
CA20042522862	20040521	CA20042523548	20040521	EP20040752943	20040521
EP20040753259	20040521	CA20042759064	20040521	CA20042836758	20040521
JP20120165559	20040521	US20040550326	20040521	US20040550323	20040521
EP20060533393	20040521	JP20060533393T	20040521	EP20120165819	20040521
WO2004US16021	20040521	WO2004US16398	20040521	US20060550323	20060901
US20060561615	20061120	US20070621001	20070108	US20070550326	20070109
US20070932391	20071031	US20070932434	20071031	US20070932321	20071031
US20070932596	20071031	US20070932652	20071031	AU20090200148	20090114
US20110165155	20110621	CA20112405464	20111101	US20110301387	20111121
US20110301340	20111121	CA20112522862	20111206	US20120345011	20120106
US20120344986	20120106	US20120410997	20120302	US20130039128	20130927
CA20142523548	20140113	US20140315560	20140626	US20150929791	20151102
US20160388498	20161222	WO2017US67515	20171220	US20180882679	20180129
US20190503244	20190703				

Probable Assignee: IP RESERVOIR LLC

Assignee(s): (std): BRINK BENJAMIN M ; CHAMBERLAIN ROGER D ; CHOLLETI SHARATH R ; CYTRON RON K ; CYTRON RON KAPLAN ; DATA SEARCH SYSTEMS INC ; CYTRON RONALD K ; EXEGY INC A CORP OF STATE ; EXEGY INC ; INDECK RONALD S ; FRANKLIN MARK ALLEN ; UNIV WASHINGTON ; FRANKLIN MARK A ; WASHINGTON UNIV A CORP O ; WASHINGTON UNIV ; IP RESERVOIR LLC ; WHITE JASON R

Assignee(s): WASHINGTON UNIVONE BROOKINGS DRIVEST. LOUISMO63130US ; EXEGY INC A OF STATE OFDELAWARE CORP ; IP RESERVOIR LLC100 - 349 MARSHALL AVE.ST LOUISMO63119US ; EXEGY INC4041 FOREST PARK AVENUEST. LOUISMO53108US ; IP RESERVOIR LLC CREVE COEUR ; WASHINGTON UNIV SCHOOL OF MEDICINE ; WASHINGTON UNIV A OF STATEOF CORP ; WASHINGTON UNIV A OF STATE OF MISSOURI CORP ; WASHINGTON UNIV A OF STATEOF MISSOURI CORP ; CYTRON SHARATH R ; DATA SEARCH SYSTEMS INC4041 FOREST PARK AVENUEA CORPORATION OF THE STATE

OF DELAWARE. LOUISMO63108US ; EXEGY INC A OF STATE OF DELAWARE CORP

Inventor(s): (std): BENJAMIN M BRINK ; MARK ALLEN FRANKLIN ; SHARATH R CHOLLETI ; ROGER D CHAMBERLAIN ; RONALD S INDECK ; RONALD K CYTRON ; CYTRON RON ; CYTRON RONALD K ; FRANKLIN MARK A ; WHITE JASON R ; BRINK BENJAMIN M ; CHAMBERLAIN ROGER D ; INDECK RONALD ; FRANKLIN MARK ; MARK A FRANKLIN ; RON K CYTRON ; JASON R WHITE ; RON KAPLAN CYTRON ; CHOLLETI SHARATH R ; CYTRON RON K ; FRANKLIN MARK ALLEN ; CYTRON RON KAPLAN ; INDECK RONALD S ; CYTRON SHARATH R ; RON K SCITRON ; CYTRON RONALD KAPLAN

Inventor(s): RONALD KAPLAN CYTRON ; CYTRON RONALD K ST LOUIS ; FRANKLIN MARK A ST LOUIS ; WHITE JASON R FENTON ; BRINK BENJAMIN M ST LOUIS ; CHAMBERLAIN ROGER D ST LOUIS ; INDECK RONALD SUS ; FRANKLIN MARK ALLENUS ; CYTRON RON KAPLANUS ; CHOLLETI SHARATH ; CHAMBERLAIN ROGER ; WHITE JASON ; BRINK BENJAMIN ; WHITE JASON RUS ; CYTRON RONALD KUS ; FRANKLIN MARK AUS ; BRINK BENJAMIN MUS ; CHAMBERLAIN ROGER DUS

Agent(s): PIZZEYS PATENT AND TRADE MARK ATTORNEYS PTY LTD ; PIZZEYS PATENT AND TRADE MARK ATTORNEYS ; PIZZEYS ; OSLER HOSKIN AND HARCOURT LLP ; MCFADDEN FINCHAM ; HACKNEY NIGEL JOHN ET AL ; HACKNEY NIGEL JOHN ; MEWBURN ELLIS LLP ; HITOSHIO AKIO ; TSUBOKURA MICHIAKI ; ONO MAKOTO ; OSAKI KATSUMASA ; KAWAGUCHI YOSHIO ; KANAYAMA MASATAKA ; KAWAGUTI AND PARTNERS ; THOMPSON COBURN LLP ; THOMPSON COBURN LLP ATTN RICHARD E HAFERKAMP ; THOMAS COBURN LLP ; BENJAMIN L ; VOLK BENJAMIN L JR ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DJ DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JO JP KE KG KH KM KN KP KR KW KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

15) Family number: 47108638 (US7818725B)

© PatBase

Title: MAPPING COMMUNICATION IN A PARALLEL PROCESSING ENVIRONMENT

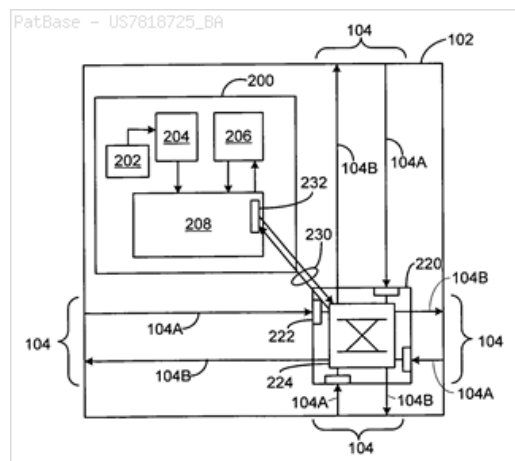
Abstract: An the integrated circuit comprises a plurality of processor cores interconnected by an interconnection network. A method for generating instructions to be executed in the integrated circuit comprises accepting a plurality of programs, at least some of the programs including one or more communication operations to communicate with other programs; mapping each program to one or more of the processor cores; determining correspondence among communication operations in the programs; and mapping communication for corresponding communication operations to resources associated with the interconnection network.

Classifications:

International (IPC 8-9): G06F9/45 (Advanced/Invention)

CPC: G06F15/17318

US: 717/136



Family:

Publication number	Publication date	Application number	Application date
US7818725 BA	20101019	US20060414473	20060428

Priority:

US20050675804P 20050428 US20060414473 20060428

Probable Assignee: MASSACHUSETTS INST OF TECHNOLOGY

Assignee(s): (std): MASSACHUSETTS INST TECHNOLOGY

Assignee(s): MASSACHUSETTS INSTITUTE OF TECHNOLOGY ; DARPA ; MASSACHUSETTS INST OF TECHNOLOGY

Inventor(s): (std): AGARWAL ANANT ; GRIFFIN PATRICK ROBERT

Agent(s): FISH AND RICHARDSON PC

16) Family number: 66452805 (US2017212739A)

© PatBase

Title: PROCESSOR WITH RECONFIGURABLE PIPELINED CORE AND ALGORITHMIC COMPILER

Abstract: An algorithmic matching pipelined compiler and a reusable algorithmic pipelined core comprise a system. The reusable algorithmic pipelined core is a reconfigurable processing core with a pipelined structure comprising a processor with a setup interface for programming any of a plurality of operations as determined by setup data, a logic decision processor for programming a look up table, a loop counter and a constant register, and a block of memory. This can be used to perform functions. A reconfigurable, programmable circuit routes data and results from one core to another core and/or IO controller and/or interrupt generator, as required to complete an algorithm without further intervention from a central or peripheral processor during processing of an algorithm.

Classifications:

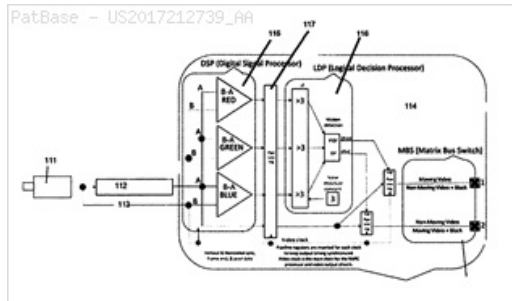
International (IPC 8-9): G06F G06F13/40 G06F15/78 G06F15/80

G06F17/50 G06F19/00 G06F7/57 G06F8/40 G06F8/41 G06F9/30

G06F9/38 G06F9/44 G06F9/45 G06F9/451 (Advanced/Invention)

International (IPC 1-7): G06F19/00 G06F9/45

CPC: G06F30/331 G06F9/3001 G06F9/3867 G06F9/3885 G06F8/447
G06F13/4022 G06F15/7889 G06F15/7867 Y02D10/14 Y02D10/151
US: 1/1 717/140



Family:

Publication number	Publication date	Application number	Application date
AU2017211781 AA	20180913	AU20170211781	20170126
BR112018015276 A2	20181218	BR20181115276	20170126
CA3012781 AA	20180725	CA20173012781	20170126
CL2018002025 A1	20190208	CL20180002025	20180726
CN108885543 A	20181123	CN201780020270	20170126
CO20180008835 A2	20181113	CO20180008835	20180824
EP3408737 A1	20181205	EP20170744897	20170126
EP3408737 A4	20190911	EP20170744897	20170126
ID201813203 A	20181231	ID2018P0006491	20170126
IL260778 A0	20180920	IL20170260778	20170126
IN201817031832 A	20190104	IN201817031832	20180824
JP2019506695 T2	20190307	JP20180558111T	20170126
KR20180132044 A	20181211	KR20187024664	20170126
MX2018009255 A1	20190318	MX20180009255	20170126
PH2018501591 A	20190408	PH20180501591	20180726
SG11201806395S A1	20180830	SG20181106395	20170126
TR201810673 T1	20181022	TR20180010673T	20170126
US2017212739 AA	20170727	US20170416972	20170126
US2018246834 AA	20180830	US20180919885	20180313
US10515041 BB	20191224	US20180919885	20180313
WO17132385 A1	20170803	WO2017US15143	20170126

Priority:

US20160287265P 20160126 US20170416972 20170126 WO2017US15143 20170126
US20180919885 20180313

Probable Assignee: ICAT LLC

Assignee(s): (std): ICAT LLC

Assignee(s): CATILLER ROBERT

Inventor(s): (std): ROBERT CATILLER ; CATILLER ROBERT

Agent(s): FB RICE PTY LTD; IP GATEWAY PATENT AND TRADE MARK ATTORNEYS PTY LTD; CONNEELY PROFESSIONAL CORP; ESTUDIO CLARKE MODET AND CO CHILE LIMITADA; WLASZENKO JOZEF; BAGUS LESTANTO SH LLM; HANDE MUMCUOGLU; PARADIES CHRISTOPHER; PARADIES LAW PA

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DJ DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KH KM KN KP KR KW KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

17) Family number: 15253823 (US2001042188A)

© PatBase

Title: MULTIPLE-THREAD PROCESSOR FOR THREADED SOFTWARE APPLICATIONS

Abstract: A processor has an improved architecture for multiple-thread operation on the basis of a highly parallel structure including multiple independent parallel execution paths for executing in parallel across threads and a multiple-instruction parallel pathway within a thread. The multiple independent parallel execution paths include functional units that execute an instruction set including special data-handling instructions that are advantageous in a multiple-thread environment.

Classifications:

International (IPC 8-9): G06F1/035 G06F7/38 G06F7/552 G06F9/30 G06F9/302 G06F9/38 G06F9/44 G09G5/30 (Advanced/Invention); G06F1/02 G06F7/38 G06F7/48 G06F9/30 G06F9/302 G06F9/38 (Core/Invention)

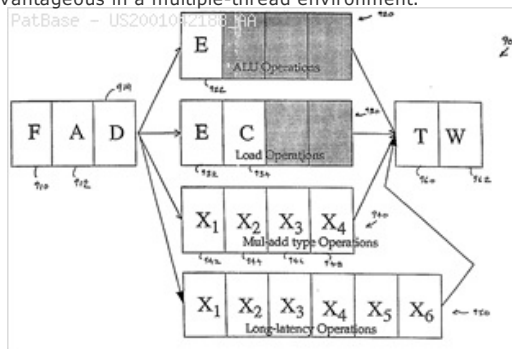
International (IPC 1-7): G06F15/00 G06F7/00 G06F7/38 G06F7/552 G06F9/00 G06F9/30 G06F9/38 G06F9/46

CPC: G06F1/0356 G06F7/483 G06F7/5525 G06F9/30014 G06F9/30036 G06F9/30098 G06F9/3012 G06F9/3838 G06F9/3853 G06F9/3877 G06F9/3885 G06F2101/08 G06F2207/3824 G06F2207/3828 G06F2207/5521 G06F9/3001 G06F9/30123 G06F9/30141 G06F9/30145 G06F9/3826 G06F9/3824 G06F9/3851

European: G06F1/035D G06F7/552R G06F9/30A1A G06F9/30A1A1 G06F9/30A1P G06F9/30R G06F9/30R5 G06F9/30R5C G06F9/30R6 G06F9/38D G06F9/38D1 G06F9/38E1 G06F9/38E4 G06F9/38E6 G06F9/38S G06F9/38T S06F101/08 S06F207/38A4D3 S06F207/38A4M S06F207/552A S06F7/483

US: 345/590 345/620 708/100 708/490 708/500 708/502 708/605 712/10 712/10P 712/11 712/11P 712/212 712/221 712/221P 712/E09.017 712/E09.026 712/E09.027 712/E09.053 712/E09.054 712/E09.069 712/E09.071 712/E9.017 712/E9.026 712/E9.027 712/E9.053 712/E9.054 712/E9.069 712/E9.071 712/E90.17S 712/E90.26S 712/E90.27S 712/E90.53S 712/E90.69S 718/107 718/107S

Family:



Publication number	Publication date	Application number	Application date
DE69909829 D1	20030828	DE19996009829T	19991203
DE69909829 D1	20030828	DE19996009829	19991203
DE69909829 T2	20040527	DE19996009829T	19991203
EP1137984 A2	20011004	EP19990963017	19991203
EP1137984 B1	20030723	EP19990963017	19991203
US2001042188 AA	20011115	US19980204480	19981203
US2005010743 AA	20050113	US20040818785	20040406
US2006282650 AA	20061214	US20060382203	20060508
US6341300 BA	20020122	US19990240977	19990129
US6718457 BB	20040406	US19980204480	19981203
US7042466 BA	20060509	US20000589039	20000606
US7587582 BA	20090908	US20000640901	20000816
WO0033185 A2	20000608	WO1999US28821	19991203
WO0033185 A3	20001012	WO1999US28821	19991203
WO0045251 A2	20000803	WO2000US01578	20000124
WO0045251 A3	20001214	WO2000US01578	20000124

Priority:

US19980204480 19981203 US19990240977 19990129 WO1999US28821 19991203
US20000589039 20000606 US20000640901 20000816 US20040818785 20040406
US20060382203 20060508

Probable Assignee: ORACLE CORP

Assignee(s): (std): SUN MICROSYSTEMS INC ; TREMBLAY MARC

Assignee(s): JOY WILLIAM ; ORACLE AMERICA INC ; ORACLE CORP

Inventor(s): (std): SHANKAR RAVI ; SUDHARSANAN SUBRAMANIA I ; CHAN JEFFREY M W ; JOY N ; NELSON SCOTT R ; SUDHARSANAN SUBRAMANIA ; DEERING MICHAEL F ; JOY WILLIAM ; JOY WILLIAM N ; TREMBLAY MARC ; CHAN JEFFREY MENG WAH

Inventor(s): DEERING MICHAEL ; CHAN JEFFREY MW ; CHAN JEFFREY

Agent(s): ZAGORIN OBRIEN AND GRAHAM LLP; ZAGORIN O'BRIEN GRAHAM LLP (004); ZAGORIN OBRIEN GRAHAM LLP 004; ZAGORIN OBRIEN GRAHAM LLP; FORREST; GUNNISON MCKAY AND HODGSON LLP

Designated states: AT BE CH CY DE DK ES FI FR GB GR IE IT JP KR LI LU MC NL PT SE

18) Family number: 55727909 (US2014040552A)

© PatBase

Title: MULTI-CORE COMPUTE CACHE COHERENCY WITH A RELEASE CONSISTENCY MEMORY ORDERING MODEL

Abstract: A method includes storing, with a first programmable processor, shared variable data to cache lines of a first cache of the first processor. The method further includes executing, with the first programmable processor, a store-with-release operation, executing, with a second programmable processor, a load-with-acquire operation, and loading, with the second programmable processor, the value of the shared variable data from a cache of the second programmable processor.

Classifications:

International (IPC 8-9): G06F12/00 G06F12/08

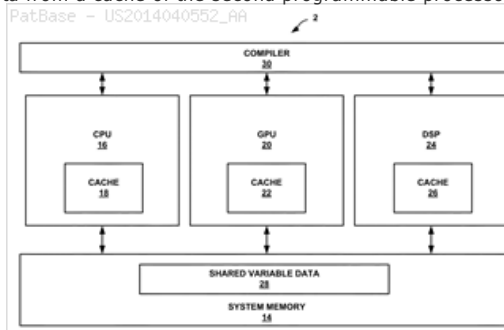
G06F12/0877 (Advanced/Invention);

G06F13/00 G06F13/28 (Advanced/Non-invention)

CPC: G06F12/0833 G06F12/0815 G06F12/0811 G06F12/0837

G06F12/0891 G06F2212/302

US: 1/1 711/122 711/135 711/141 711/146



Family:

Publication number	Publication date	Application number	Application date
CN104520825 A	20150415	CN201380041399	20130805
CN104520825 B	20180202	CN201380041399	20130805
IN00210CN2015 A	20160701	IN2015CN00210	20150109
JP2015524597 T2	20150824	JP20150526608T	20130805
JP6062550 B2	20170118	JP20150526608T	20130805
KR101735222 B1	20170524	KR20157004705	20130805
KR20150040946 A	20150415	KR20157004705	20130805
US2014040552 AA	20140206	US20130958399	20130802
US9218289 BB	20151222	US20130958399	20130802
WO14025691 A1	20140213	WO2013US53626	20130805

Priority:

US20120680201P 20120806 US20130800441P 20130315 US20130958399 20130802
WO2013US53626 20130805

Probable Assignee: QUALCOMM INC

Assignee(s): (std): QUALCOMM INC

Assignee(s): TZENG TZUNG REN ; RYCHLIK BOHUSLAV ; QUALCOMM INC5775 MOREHOUSE DRIVEINTERNATIONAL IP ADMINISTRATIONSAN DIEGOCA92121-1714US ; SHARP COLIN CHRISTOPHER ; BOURD ALEXEI V ; DEMERS ERIC ; GRUBER ANDREW EVAN

Inventor(s): (std): TZENG TZUNG REN ; RYCHLIK BOHUSLAV ; DEMERS ERIC ; SHARP COLIN CHRISTOPHER ; GRUBER ANDREW EVAN ; BOURD ALEXEI V

Inventor(s): DEMERS ERICUS ; GRUBER ANDREW EVANUS ; TZENG TZUNG RENU ; RYCHLIK BOHUSLAVUS ;

SHARP COLIN CHRISTOPHERUS ; BOURD ALEXEI VUS

Agent(s):

SHUMAKER AND SIEFFERT PA; CREERON KERRY T

Designated states:

AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR
CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID
IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR
MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI
SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW