

1) Family number: 51087282 (US2016006439A)

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Title: PROGRAMMABLE INPUT/OUTPUT CIRCUIT

Abstract: A apparatus, having a processing system and an input buffer coupled with both the processing system and one of two IO pads, and a reference buffer coupled to both the input buffer and the second of the IO pads such that the reference generator controls the input threshold of the input buffer in response to an analog voltage received from an external circuit on the second of the IO pads.

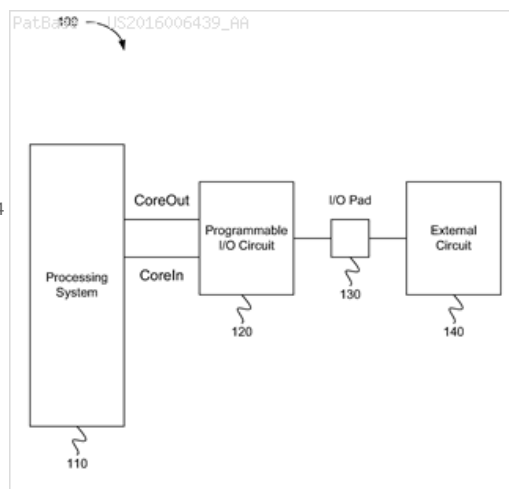
Classifications:

International (IPC 8-9): G01R31/317 G01R31/3177 G06F12/02 G06F13/28 G06F5/06 G11C16/10 G11C7/10 H03K19/0175 H03K19/094 H03K19/173 (Advanced/Invention); G06F13/40 (Advanced/Non-invention)

CPC: G06F13/4072 H03K19/017581 G06F12/0246 G11C16/102 G06F2212/7201 G11C7/1084 G11C7/1057 G01R31/3177 G01R31/31721 H03K19/01759 G06F5/065 G06F13/28 H03K19/173

European: H03K19/0175R

US: 1/1 326/38 326/82 326/83 326/86 327/109 327/112 710/302 714/724



Family:

Publication number	Publication date	Application number	Application date
US2016006439 AA	20160107	US20150690106	20150417
US2017194963 AA	20170706	US20160369674	20161205
US2018292454 AA	20181011	US20180944244	20180403
US2019214990 AA	20190711	US20180193261	20181116
US8179161 BA	20120515	US20100753657	20100402
US8487655 BA	20130716	US20100774680	20100505
US8558578 BA	20131015	US20120427264	20120322
US9013209 BA	20150421	US20130054657	20131015
US9143134 BA	20150922	US20130916386	20130612
US9515659 BB	20161206	US20150690106	20150417
US9952282 BA	20180424	US20150860515	20150921
US10153770 BB	20181211	US20160369674	20161205
US10345377 BB	20190709	US20180944244	20180403
US10634722 BA	20200428	US20190420910	20190523

Priority:

US20090175586P	20090505	US20090175586P	20090506	US20090176933P	20090510
US20100753657	20100402	US20100774680	20100505	US20120427264	20120322
US20130916386	20130612	US20130054657	20131015	US20150690106	20150417
US20150860515	20150921	US20160369674	20161205	US20180944244	20180403
US20180193261	20181116	US20190420910	20190523		

Probable Assignee: CYPRESS SEMICONDUCTOR CORP

Assignee(s): (std): VERGE GREGORY J ; WILLIAMS TIMOTHY J ; WRIGHT DAVID G ; WILLIAMS TIMOTHY ; THIAGARAJAN EASHWAR ; SULLAM BERT ; SNYDER WARREN S ; SHUTT JAMES ; SEGUINE DENNIS ; MAR MONTE ; KUTZ HAROLD ; KOHAGEN NATHAN ; HASTINGS MARK ; CYPRESS SEMICONDUCTOR CORP ; BYRKETT BRUCE E ; BYRKETT BRUCE

Assignee(s): MORGAN STANLEY SENIOR FUNDING INC ; MORGAN STANLEY SENIOR FUNDING INC COLLATERAL AGENT AS ; CYPRESS SEMICONDUCTOR A OF DELAWARE CORP ; MUFG UNION BANK NA ; MORGAN STANLEY SENIOR FUNDING

Inventor(s): (std): BYRKETT BRUCE E ; VERGE GREGORY J ; WILLIAMS TIMOTHY J ; WRIGHT DAVID G ; WILLIAMS TIMOTHY JOHN ; WILLIAMS TIMOTHY ; VERGE GREGORY JOHN ; THIAGARAJAN EASHWAR ; SULLAM BERT S ; SULLAM BERT ; SNYDER WARREN S ; SHUTT JAMES H ; SHUTT JAMES ; SEGUINE DENNIS RAYMOND ; SEGUINE DENNIS R ; SEGUINE DENNIS ; MAR MONTE ; KUTZ HAROLD M ; KUTZ HAROLD ; KOHAGEN NATHAN WAYNE ; KOHAGEN NATHAN ; HASTINGS MARK E ; HASTINGS MARK ; BYRKETT BRUCE

2) Family number: 46422614 (US2010199077A)

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Abstract: Under the direction of a first party, an integrated circuit (IC) device is configured to temporarily enable access to a debug interface of the IC device via authentication of the first party by a challenge/response process using a key of the IC device and a challenge value generated at the IC device. The first party then may conduct a software evaluation of the IC device via the debug interface. In response to failing to identify an issue with the IC device from the software evaluation, the first party can permanently enable open access to the debug interface while authenticated and provide the IC device to a second party. Under the direction of the second party, a hardware evaluation of the IC device is conducted via the debug interface that was permanently opened by the first party.

Classifications:

International (IPC 8-9): G06F11/36 G06F21/00 G06F21/22 G06F21/44

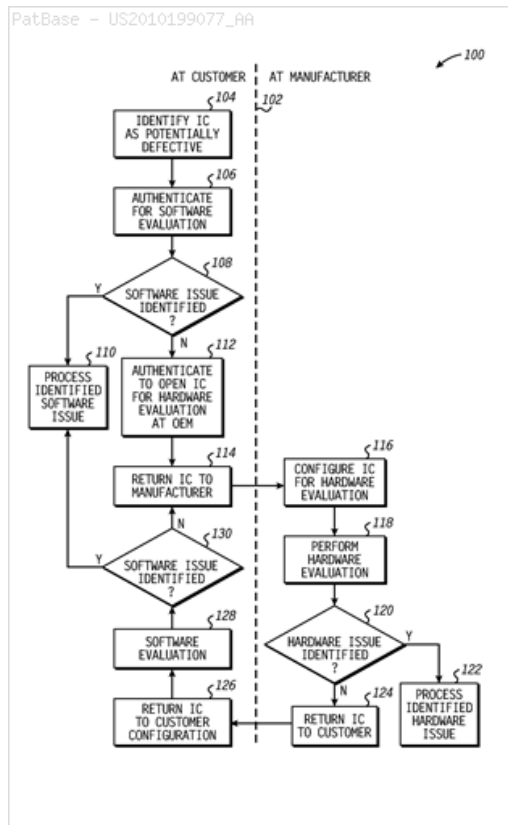
G06F9/00 H04L9/32 (Advanced/Invention);

G06F11/36 G06F21/00 G06F9/00 (Core/Invention)

CPC: G06F11/3656 H04L9/3247 H04L9/3271

European: G06F11/36B7H

US: 713/1 713/168 713/182 713/182S 713/185 713/1P 726/2



Family:

Publication number	Publication date	Application number	Application date
CN102301375 A	20111228	CN201080006319	20100113
CN102301375 B	20140910	CN201080006319	20100113
EP2391969 A2	20111207	EP20100736189	20100113
EP2391969 A4	20120627	EP20100736189	20100113
EP2391969 B1	20170802	EP20100736189	20100113
KR101587309 B1	20160120	KR20117020042	20100113
KR20110114687 A	20111019	KR20117020042	20100113
US2010199077 AA	20100805	US20090363259	20090130
US8332641 BB	20121211	US20090363259	20090130
WO10088043 A2	20100805	WO2010US20855	20100113
WO10088043 A3	20100923	WO2010US20855	20100113

Priority:

US20090363259 20090130 WO2010US20855 20100113

Probable Assignee: NXP SEMICONDUCTORS NV

Assignee(s): (std): MUIR ALISTAIR N ; HARTLEY DAVID H ; MACKIE TROY E ; FREESCALE SEMICONDUCTOR INC ; ASHKENAZI ASAF ; CASE LAWRENCE L ; CHHABRA RUCHIR ; COVEY CARLIN R ; VAGLICA JOHN J ; TKACIK THOMAS E ; ZIOLKOWSKI RODNEY D ; REDMAN MARK D ; NXP USA INC ; NXP SEMICONDUCTORS NV

Assignee(s): SHENZHEN XINGUODU TECHNOLOGY CO LTD ; CITIBANK NA ; CITIBANK NA NOTES COLLATERAL AGENT AS ; MORGAN STANLEY SENIOR FUNDING INC ; NXP BV ; NXP F K A FREESCALE SEMICONDUCTOR INC BV

Inventor(s): (std): ASHKENAZI ASAF ; CASE LAWRENCE L ; CHHABRA RUCHIR ; COVEY CARLIN R ; HARTLEY DAVID H ; MACKIE TROY E ; MUIR ALISTAIR N ; REDMAN MARK D ; TKACIK THOMAS E ; VAGLICA JOHN J ; ZIOLKOWSKI RODNEY D

Agent(s): FERRO FRODO NUNES; FREESCALE LAW DEPARTMENT EMEA PATENT OPS; LARSON NEWMAN AND ABEL LLP; KING ROBERT L ET AL

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PE PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

Title: DEBUG ARCHITECTURE

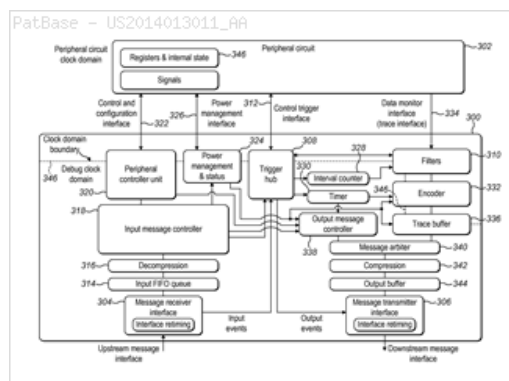
Abstract: Roughly described, an integrated circuit chip comprises a plurality of peripheral circuits, each peripheral circuit connected to a respective debug unit; a shared hub; and between each respective debug unit and the shared hub, a single physical interface configured to transport both configuration data and event data, wherein the interface is configured such that if an event occurs whilst the interface is transporting configuration data, the interface interrupts the transport of the configuration data in order to transport the event data.

Classifications:

International (IPC 8-9): G01R31/28 G01R31/317 G06F1/00 G06F1/24 G06F1/26 G06F1/30 G06F1/32 G06F11/00 G06F11/22 G06F11/263 G06F11/267 G06F11/27 G06F11/34 G06F11/36 G06F12/00 G06F13/40 G06F21/44 G06F21/62 G06F21/70 G06F21/85 G06F3/00 G06F9/44 G11C7/00 H04L29/12 (Advanced/Invention); B01J23/04 B01J38/48 G06F11/34 G06F11/36 G06F12/14 G06F15/78 (Advanced/Non-invention)

CPC: G06F9/4411 G06F21/70 G06F13/404 G06F13/4022 H04L61/6004 H04L47/2408 H04L47/245 G06F11/3466 G06F15/7807 G06F11/2205 B01J23/04 B01J38/485 G06F11/3632 G06F11/3656 G06F1/24 G06F1/30 G06F1/32 G06F1/3203 G06F1/3206 G06F1/3234 G06F1/3246 G06F1/325 G06F1/3287 G06F11/263 G06F11/267 G06F11/36 G06F11/362 G06F11/3636 G06F11/3648 G01R31/31721 G06F1/26 G01R31/2884 G01R31/31719 G01R31/31705 G06F11/348 G06F21/44 G06F21/62 G06F21/85 G06F2201/835 G06F2201/86 G06F2201/88 G06F11/27 G06F11/3024 G06F11/3041 G06F11/3051

US: 1/1 710/14 710/8 713/330 714/30 714/32 714/724 714/733 726/17

**Family:**

Publication number	Publication date	Application number	Application date
GB201212175 A0	20120822	GB20120012175	20120709
GB201212177 A0	20120822	GB20120012177	20120709
GB201212178 A0	20120822	GB20120012178	20120709
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GB201212180 A0	20120822	GB20120012180	20120709
GB201212181 A0	20120822	GB20120012181	20120709
GB2500074 A1	20130911	GB20120012181	20120709
GB2500074 B2	20140820	GB20120012181	20120709
GB2500441 A1	20130925	GB20120012177	20120709
GB2500441 B2	20140305	GB20120012177	20120709
GB2501135 A1	20131016	GB20120012175	20120709
GB2501135 B2	20150826	GB20120012175	20120709
GB2501333 A1	20131023	GB20120012180	20120709
GB2501333 B2	20140305	GB20120012180	20120709
GB2503881 A1	20140115	GB20120012178	20120709
GB2503881 B2	20140618	GB20120012178	20120709
GB2503882 A1	20140115	GB20120012179	20120709
GB2503882 B2	20140702	GB20120012179	20120709
US2014013011 AA	20140109	US20130938046	20130709
US2014013145 AA	20140109	US20130938077	20130709
US2014013157 AA	20140109	US20130938053	20130709
US2014013161 AA	20140109	US20130938065	20130709
US2014013172 AA	20140109	US20130938088	20130709
US2014013421 AA	20140109	US20130938098	20130709
US2015377965 AA	20151231	US20150843745	20150902
US2016356841 A1	20161208	US20160241805	20160819
US2017277883 AA	20170928	US20170617953	20170608
US9003232 BB	20150407	US20130938065	20130709
US9026871 BB	20150505	US20130938088	20130709
US9032109 BB	20150512	US20130938046	20130709
US9176552 BB	20151103	US20130938077	20130709
US9218258 BB	20151222	US20130938053	20130709
US9703944 BB	20170711	US20130938098	20130709
US9927486 BB	20180327	US20160241805	20160819
US9928361 BB	20180327	US20170617953	20170608
US10132863 BB	20181120	US20150843745	20150902
WO14009323 A2	20140116	WO2013EP64407	20130708
WO14009323 A3	20140417	WO2013EP64407	20130708

Priority:

GB20120012175 20120709	GB20120012177 20120709	GB20120012178 20120709
GB20120012179 20120709	GB20120012181 20120709	GB20120012180 20120709
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US20170617953 20170608		

Probable Assignee: ULTRASOC TECHNOLOGIES LTD

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Inventor(s): ARNAB BANERJEE ; KLAUS DIETER MCDONALD MAIER ; STEPHEN JOHN BARLOW ; ANDREW BRIAN THOMAS HOPKINS

Agent(s): WARREN S; HAYNES DEFFEL AND WOLFELD LLP; HAYNES BEFFEL AND WOLFELD LLP; DEBORAH L; SLINGSBY PARTNERS LLP

Designated states: AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW