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..SEMSEARCH "BROWNOUT SIGNAL" 14 "BULKY CIRCUIT" 2 "CIRCUIT" 100 "CIRCUIT BREAKER" 2 "COMPLICATED SAMPLING" 15 "COMPUTATION COMPLEXITY" 14 "CONTROL" 12 "CONTROL CIRCUIT" 27 "CONTROL CIRCUIT OUTPUT" 14 "CONTROL CIRCUITRY" 2 "DIVISION" 13 "FAILURE" 11 "FEEDBACK CIRCUIT" 41 "FILTER" 10 "HYSTERESIS EFFECT" 14 "HYSTERESIS SIGNAL" 14 "INPUT CIRCUIT" 38 "INSULATION PROTECTION" 28 "MINIATURIZATION" 2 "OPERATIONAL AMPLIFIER GENERATING" 16 "OUTPUT CIRCUIT" 54 "OUTPUT POWER" 13 "OUTPUT VOLTAGE" 26 "OVERVOLTAGE SIGNAL" 14 "POSITIVE FEEDBACK" 13 "POSITIVE FEEDBACK SIGNAL" 15 "POWER INPUT" 12 "POWER REFERENCE" 15 "POWER SUPPLY" 27 "POWER SUPPLY CIRCUIT" 100 "RECTIFIED INPUT" 13 "REFERENCE VOLTAGE" 14 "RESISTOR VOLTAGE" 14 "SAMPLING CIRCUIT" 14 "SAMPLING CIRCUIT COMBINATION" 15 "SWITCH" 44 "SWITCH CIRCUIT" 15 "SWITCH OUTPUT" 12 "TYPE SWITCH" 2

20 Documents

Publication numbers	Title	Current assignees
EP3484035 A1	Hysteresis power supply circuit	SEARI ELECTRIC TECHNOLOGY, ...
CN205864260U U	Sluggish type power supply circuit	NOARK ELECTRICS, ...
CN204993057U U	Step -down direct current transducer	SHANGHAI CHENGYI PACKAGE TECHNOLOGY
CN103532378 A	Voltage converter capable of suppressing output voltage overshooting	ELITE SEMICONDUCTOR MEMORY TECHNOLOGY
CN104852577 A	Step-down DC converter	SHANGHAI CHENGYI PACKAGE TECHNOLOGY
WO2011137707 A2	Conversion circuit with hysteresis control and power supply system	HUAWEI TECHNOLOGIES
CN204334322U U	Transition system with soft start circuit	HANGZHOU KUANFU TECHNOLOGY
CN103414341 A	Loop circuit compensating circuit used for Buck converter	UNIVERSITY OF ELECTRONIC SCIENCE & TECHNOLOGY OF CHINA
CN109375690 A	Tandem type switch voltage stabilizing circuit	JIANGMEN CITY XINHUI DISTRICT ANTENIC ELECTRONIC
CN105099159 A	Quick starting circuit for DC-DC converter	UNIVERSITY OF ELECTRONIC SCIENCE & TECHNOLOGY OF CHINA
CN110581639 A	Quick response method and quick response circuit for light and heavy load mode switching of current type buck converter	MORNSUN GUANGZHOU SCIENCE & TECHNOLOGY
EP1931026 A2	Method and system for shared high-power transmit path for a multi-protocol transceiver	AVAGO TECHNOLOGIES
US20130278239 A1	Precharge circuits and methods for DC-DC boost converters	SILERGY
CN2927487U Y	DC converter with wide inputting-voltage range	HISENSE
US5912552 A	DC to DC converter with high efficiency for light loads	TOYOTA INDUSTRIES
WO201956275 A1	Programmable gain amplifier and delta sigma analog-to-digital converter containing pga	TEXAS INSTRUMENTS
US20050237037 A1	Switching power supply controller system and method	INTERSIL
US20150116035 A1	Digital calibration of programmable gain amplifiers	NXP
CN104753330 A	Soft start method of power management	SHENZHEN INNOPOWER TECHNOLOGY
US4761702 A	CMOS latch-up recovery circuit	MITEL NETWORKS

Family 1/20 - FAMPAT - ©Questel

Images

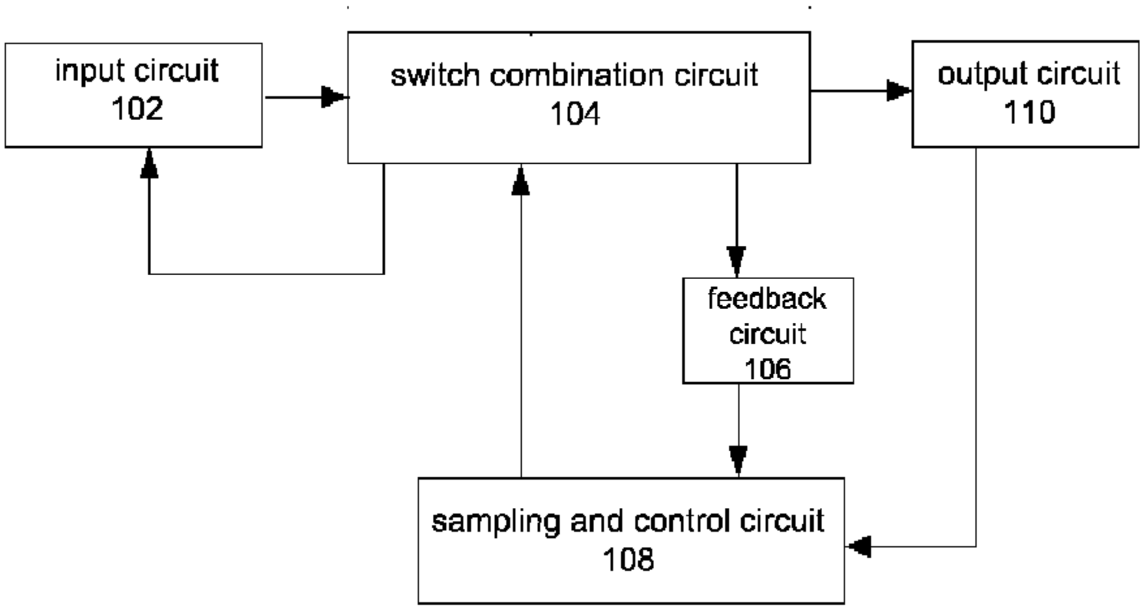

FIG 1

Publication numbers

EP3484035

MX2019000229

CL2019000021

EP3484035

BR112019000283

PE20190461

CO2019000048

CN106026656

BR112019000283

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A4

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A1

A1

A2

A1

A2

B

A1

A1

A

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2020-02-26

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2019-05-17

2019-05-15

2019-04-16

2019-04-03

2019-03-29

2019-01-25

2019-01-15

2018-01-11

2016-10-12

Earliest priority date

2016-07-08

Title

(EP3484035)

Hysteresis power supply circuit

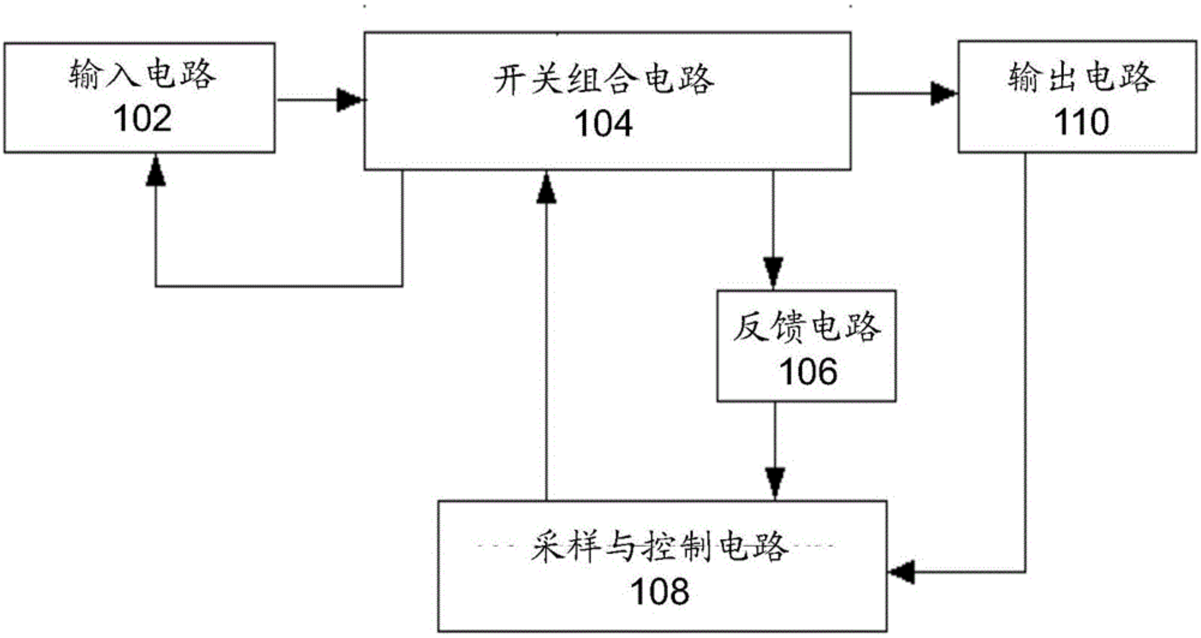
Abstract

(EP3484035)

A hysteresis power supply circuit, comprising: an input circuit (102), a switch combination circuit (104), a sampling and control circuit (108), a feedback circuit (106) and an output circuit (110). The input circuit (102) is connected to a power supply input terminal, and rectifies a power supply input and provides isolation protection for the input terminal. The switch combination circuit (104) is connected to the input circuit (102), and is turned on or off to control the output power of the power supply output terminal. The sampling and control circuit (108) samples the output voltage and compares the output voltage with the reference voltage, and controls the switch combination circuit to be turned on or off according to the result of the comparison. The feedback circuit (106) is connected between the switch combination circuit (104) and the sampling and control circuit (108). The switch combination circuit (104) outputs a positive feedback signal to the sampling and control circuit (108) through the feedback circuit (106), and the positive feedback signal causes a hysteresis effect on the comparison action of a reference power supply chip. The output circuit (110) is connected to the switch combination circuit (104), filters the output of the switch combination circuit (104) and provides isolation protection for the output terminal, and its output serves as an output of a hysteresis power supply circuit.

Family 2/20 - FAMPAT - ©Questel

Images



Publication numbers

CN205864260

Publication kind codes

U

Publication dates

2017-01-04

Earliest priority date

2016-07-08

Title

(CN205864260U)

Sluggish type power supply circuit

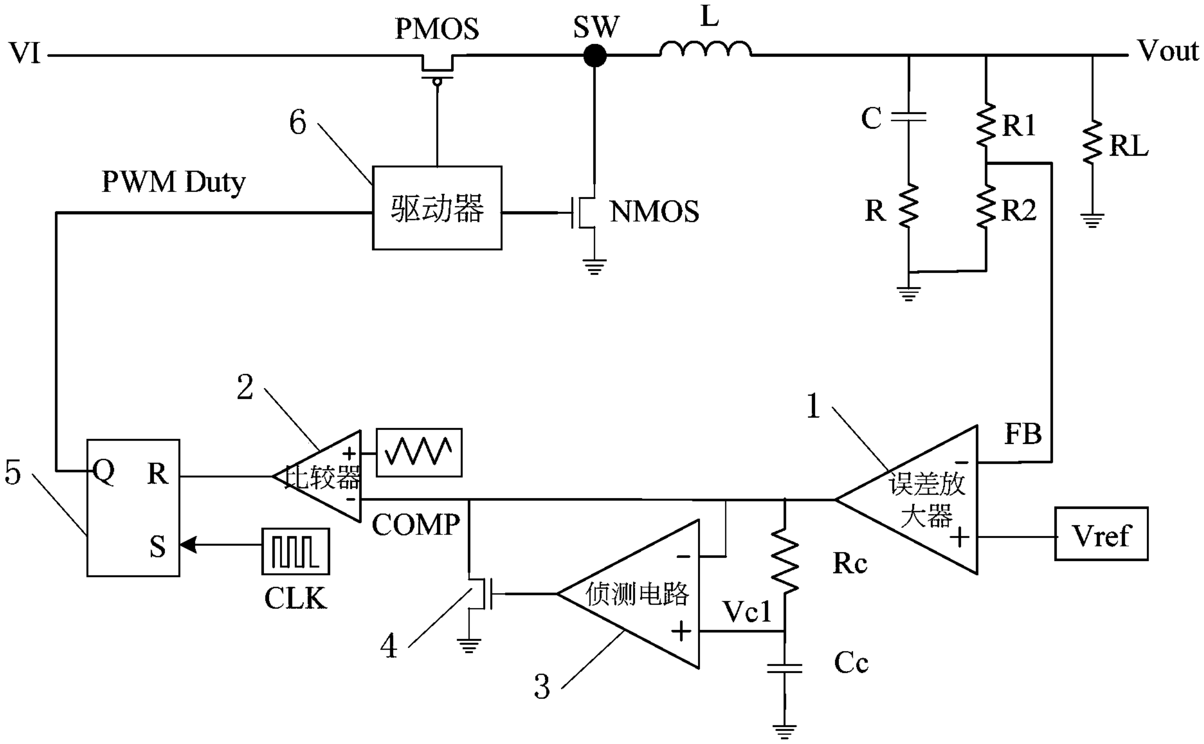
Abstract

(CN205864260)

The utility model discloses a sluggish type power supply circuit, include: input circuit, switch combinatorial circuit, sampling and control circuit, feedback circuit and output circuit. Input circuit is connected to power input end, carries out the rectification and provides the insulation blocking of input the power input. Switch combinatorial circuit is connected to input circuit, opens or turn -off the output with control power output end. Opening or turn -offing according to control switch combinatorial circuit is as a result relatively compared with control circuit sampling output voltage and with output voltage and reference voltage to the sampling. Feedback circuit connects between switch combinatorial circuit and sampling and control circuit, and switch combinatorial circuit passes through feedback circuit makes the comparison action of reference power supply chip produce sluggish effect to sampling and the positive feedback signal of control circuit output, positive feedback signal. Output circuit is connected to switch combinatorial circuit, carries out filtering and provides the insulation blocking of output switch combinatorial circuit's output, and its output is as output of sluggish type power supply circuit.

Family 3/20 - FAMPAT - ©Questel

Images



Publication numbers

CN204993057

Publication kind codes

U

Publication dates

2016-01-20

Earliest priority date

2015-06-10

Title

(CN204993057U)

Step -down direct current transducer

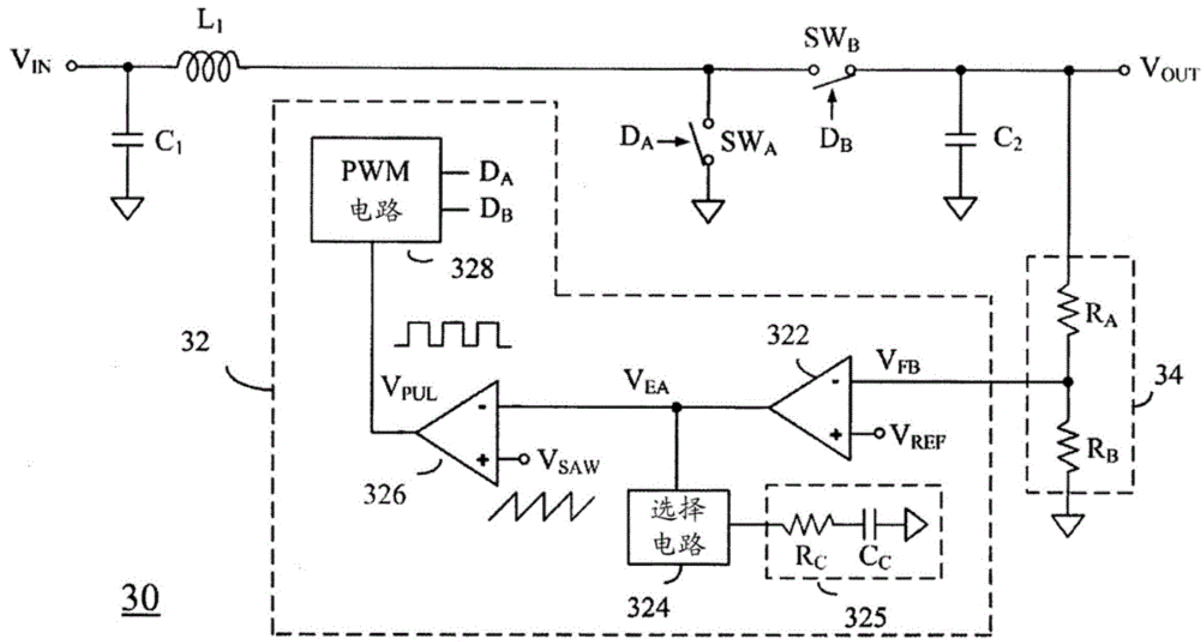
Abstract

(CN204993057)

The utility model relates to a step -down direct current transducer, it includes an error amplifier, a comparator, a compensated resistance and a building -out capacitor, wherein, a feedback voltage is received to error amplifier's negative input end, and its positive input terminal receives a reference voltage, and its output is connected to the negative input end of comparator, compensated resistance is connected with the building -out capacitor each other in series between error amplifier's the output and ground, the converter still includes: one listens the circuit, and its negative input end is connected to error amplifier's output, its positive input terminal connects compensated resistance with between the building -out capacitor, and a MOS pipe, its grid with listen the output of circuit and connect, its drain electrode and source electrode respectively with error amplifier's output and being connected with ground. The utility model discloses the output voltage peak value of traditional buck framework step -down converter when dynamic load changes has been improved for light / heavy load conversion during output can obtain littleer voltage peak.

Family 4/20 - FAMPAT - ©Questel

Images



Publication numbers

CN103532378

CN103532378

Publication kind codes

B

A

Publication dates

2016-12-21

2014-01-22

Earliest priority date

2012-07-05

Title

(CN103532378)

Voltage converter capable of suppressing output voltage overshooting

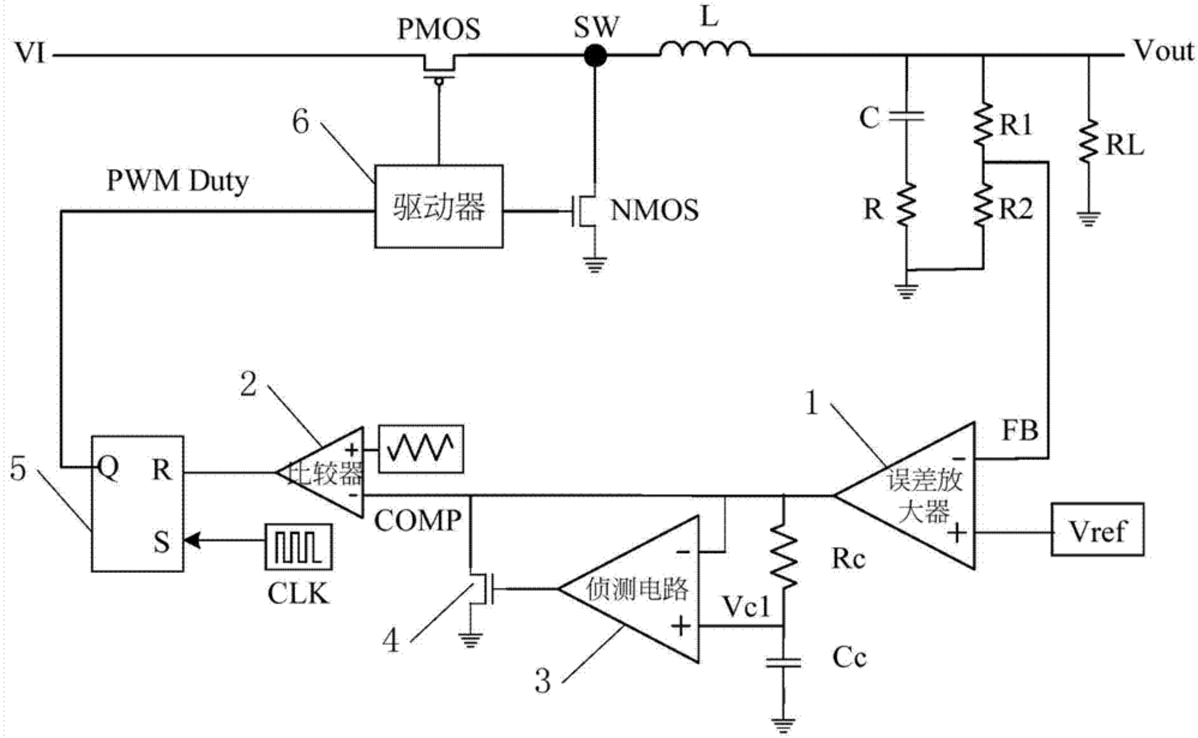
Abstract

(CN103532378)

The invention discloses a voltage converter capable of suppressing output voltage overshooting. The voltage converter is used for receiving an input voltage and adjusting the input voltage to generate an output voltage. In one embodiment of the invention, the voltage converter comprises an error amplifier, a compensation network and a selection circuit. The error amplifier has a positive-phase input end used for receiving a reference voltage, a reverse-phase input end used for receiving a feedback voltage associated with the output voltage, and an output end used for providing an error voltage. The compensation network is used for compensating the stability of the error amplifier. The selection circuit is used for selectively connecting the compensation network to the output end of the error amplifier according to the voltage level of the error voltage. In operation, when the voltage level of the feedback voltage is smaller than the voltage level of the reference voltage, the compensation network is not connected to the output end of the error amplifier; and when the voltage level of the feedback voltage is substantially equal to the voltage level of the reference voltage, the compensation network is connected to the output end of the error amplifier.

Family 5/20 - FAMPAT - ©Questel

Images



Publication numbers

CN104852577

CN104852577

Publication kind codes

B

A

Publication dates

2017-06-27

2015-08-19

Earliest priority date

2015-06-10

Title

(CN104852577)

Step-down DC converter

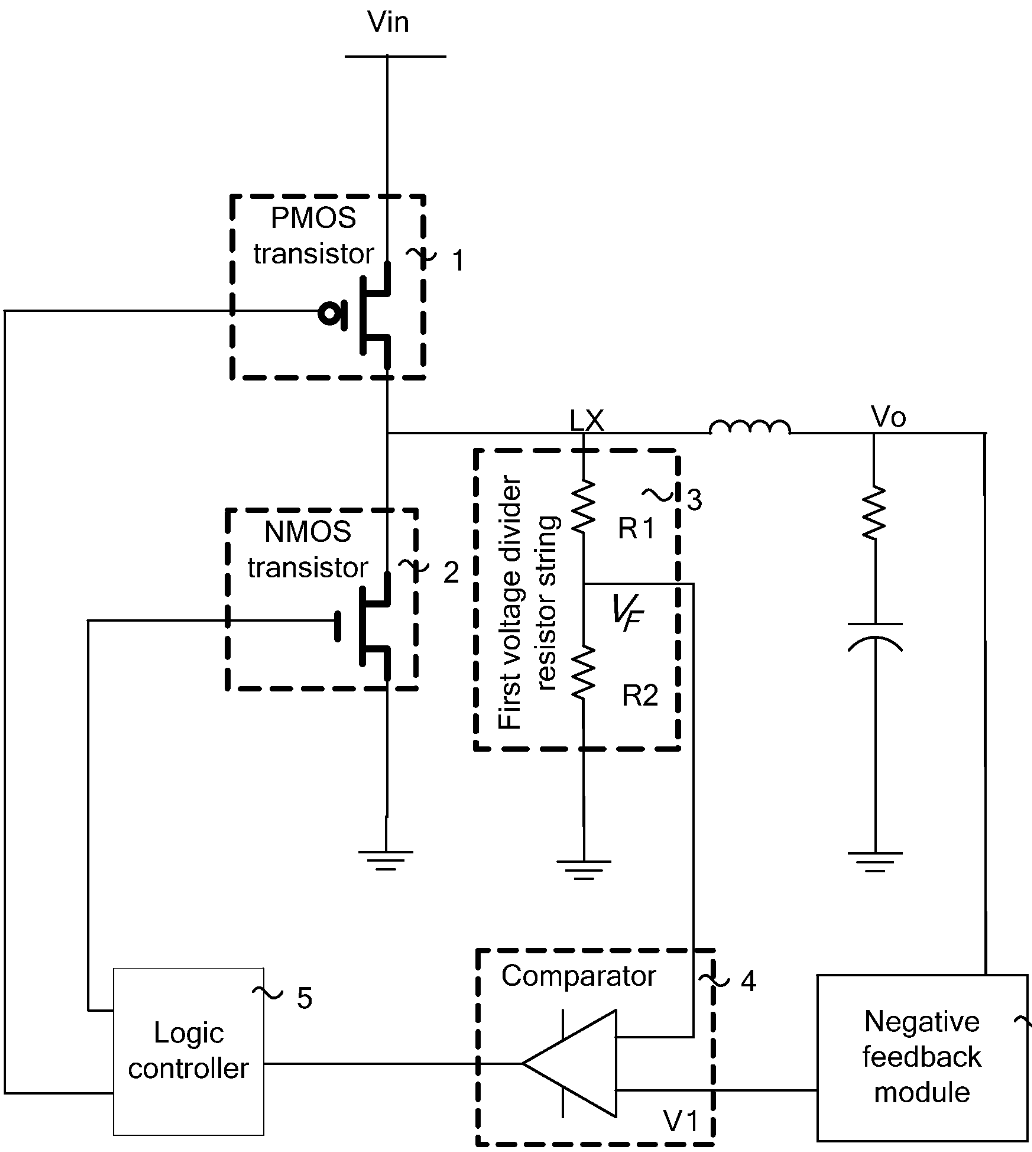
Abstract

(CN104852577)

The invention relates to a step-down DC converter, and the converter comprises an error amplifier, a comparator, a compensation resistor, and a compensation capacitor. The negative input end of the error amplifier receives a feedback voltage, and the positive input end of the error amplifier receives a reference voltage. The output end of the error amplifier is connected to the negative input end of the comparator. The compensation resistor and the compensation capacitor, which are in series connection, are connected between the output end of the error amplifier and the ground. The converter also comprises a detection circuit, wherein the negative input end of the detection circuit is connected to the output end of the error amplifier, and the positive input end of the detection circuit is connected between the compensation resistor and the compensation capacitor; and an MOS tube, wherein the grid electrode of the MOS tube is connected with the output end of the detection circuit, and the drain electrode source electrode of the MOS tube are respectively connected with the output end of the error amplifier and the ground. The converter improves the output voltage peak of a conventional step-down converter in buck configuration during dynamic load conversion, and can obtain a smaller voltage peak value of light/heavy load conversion during the output.

Family 6/20 - FAMPAT - ©Questel

Images



Publication numbers

US9209692

US20140035544

CN102204072

WO2011/137707

WO2011/137707

CN102204072

Publication kind codes

B2

A1

B

A3

A2

A

Publication dates

2015-12-08

2014-02-06

2013-06-12

2012-03-08
2011-11-10
2011-09-28

Earliest priority date

2011-04-13

Title

(WO2011137707)

Conversion circuit with hysteresis control and power supply system

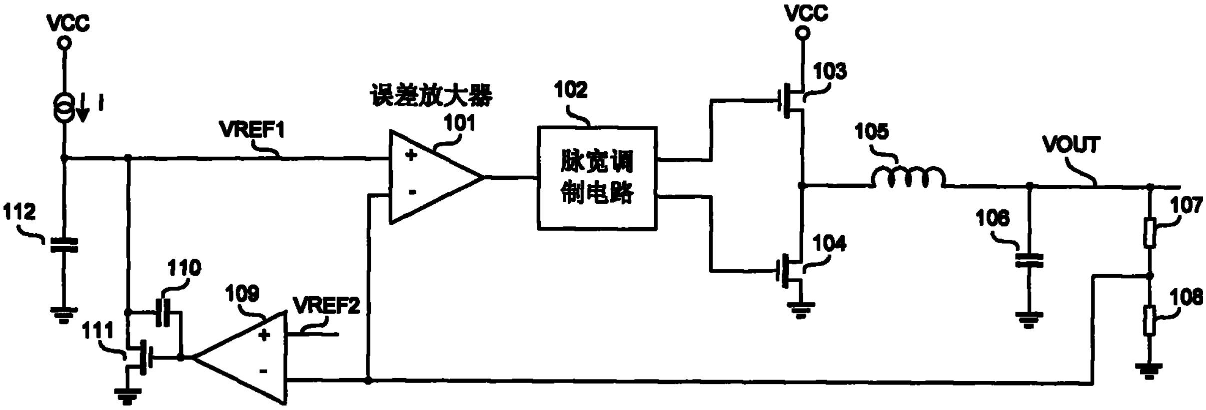
Abstract

(WO2011/137707)

A conversion circuit with hysteresis control and a power supply system. The circuit comprises a PMOS tube (1) and an NMOS tube (2) connected in series between a voltage input terminal and a ground, a first voltage-dividing resistor bank (3) connected in series between a voltage output terminal and the ground, a comparator (4) and a logic controller (5). The output terminal of the comparator is connected to the input terminal of the logic controller. Both of the output terminals of the logic controller are respectively connected to the gates of the PMOS tube and the NMOS tube. The conversion circuit further comprises a negative feedback module (6) connected between the voltage output terminal and the input terminal of the comparator. The negative feedback module (6) performs a negative feedback control for the output voltage of the conversion circuit so as to clamp the output voltage to a preset reference voltage. With the conversion circuit, errors in the output voltage of a hysteresis BUCK converter are eliminated.

Family 7/20 - FAMPAT - ©Questel

Images



Publication numbers

CN204334322

Publication kind codes

U

Publication dates

2015-05-13

Earliest priority date

2015-01-20

Title

(CN204334322U)

Transition system with soft start circuit

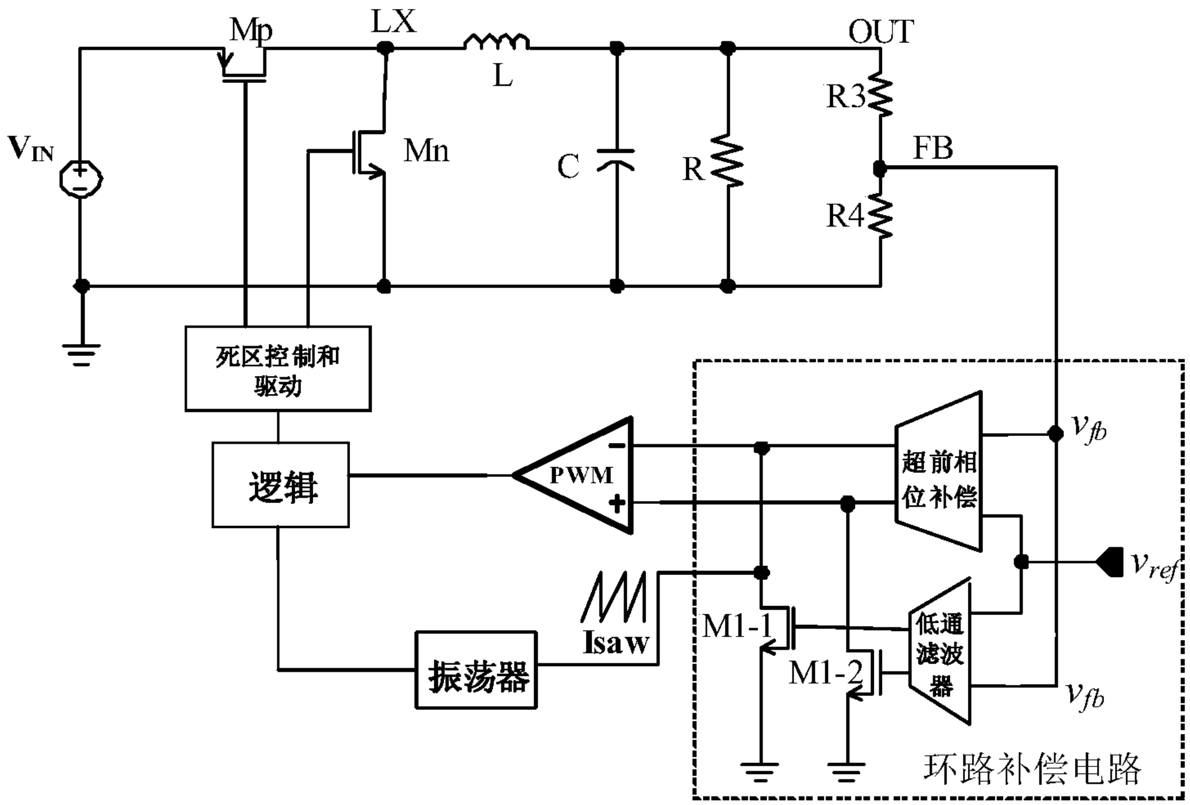
Abstract

(CN204334322)

The utility model discloses a transition system with a soft start circuit. The transition system with the soft start circuit comprises an error amplifier, a pulse width modulation circuit, a power tube, a synchronization tube, an energy storage inductor, a filter capacitor, a first resistor, a second resistor, a first comparator, a first capacitor, a first NMOS transistor, a first current source I and a second capacitor. The transition system with the soft start circuit can effectively reduce the area of the starting capacitor.

Family 8/20 - FAMPAT - ©Questel

Images



Publication numbers

CN103414341

CN103414341

Publication kind codes

B

A

Publication dates

2015-05-27

2013-11-27

Earliest priority date

2013-08-21

Title

(CN103414341B)

Loop circuit compensating circuit used for Buck converter

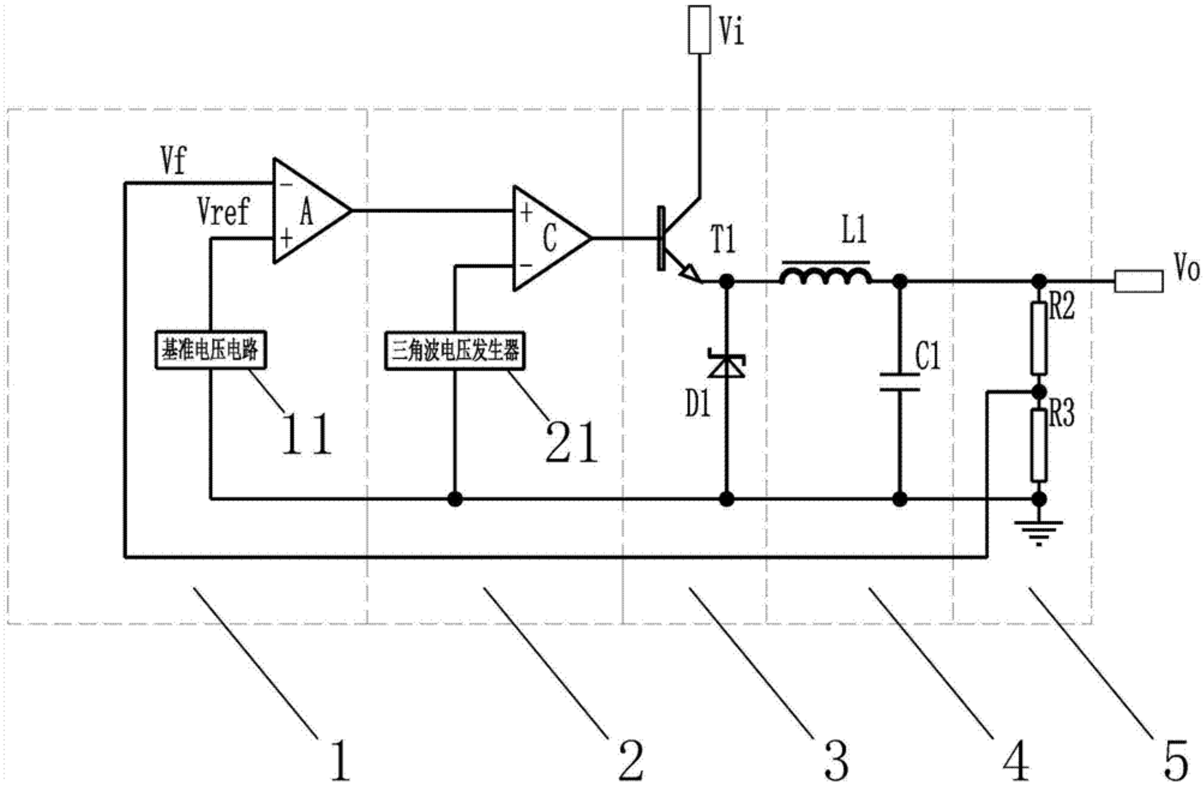
Abstract

(CN103414341)

The invention discloses a loop circuit compensating circuit used for a Buck converter, and belongs to the technical field of electronics. The loop circuit compensating circuit used for the Buck converter comprises a leading phase compensating circuit and a full-differential low-pass filter circuit. The leading phase compensating circuit generates a zero point and two high-frequency poles to provide leading phase compensating; the full-differential low-pass filter circuit provides a pole and high lower-frequency gain; the output voltage of the leading phase compensating circuit and the output voltage of the full-differential low-pass filter circuit are added in a linear mode to acquire a voltage signal required by III-type compensating; because the high lower-frequency gain and two lower-frequency zero points are acquired, the defects that lower-frequency gain is low and steady-state errors are large in leading phase compensating are overcome. According to the loop circuit compensating circuit used for the Buck converter, because full-differential input and output structures are adopted in the leading phase compensating circuit and the low-pass filter circuit respectively, power supply rejection ratio (PSRR) is increased, the crosstalk problem among DC-DC converters in all paths of a PMU can be effectively solved.

Family 9/20 - FAMPAT - ©Questel

Images



Publication numbers

CN109375690

Publication kind codes

A

Publication dates

2019-02-22

Earliest priority date

2018-10-17

Title

(CN109375690)

Tandem type switch voltage stabilizing circuit

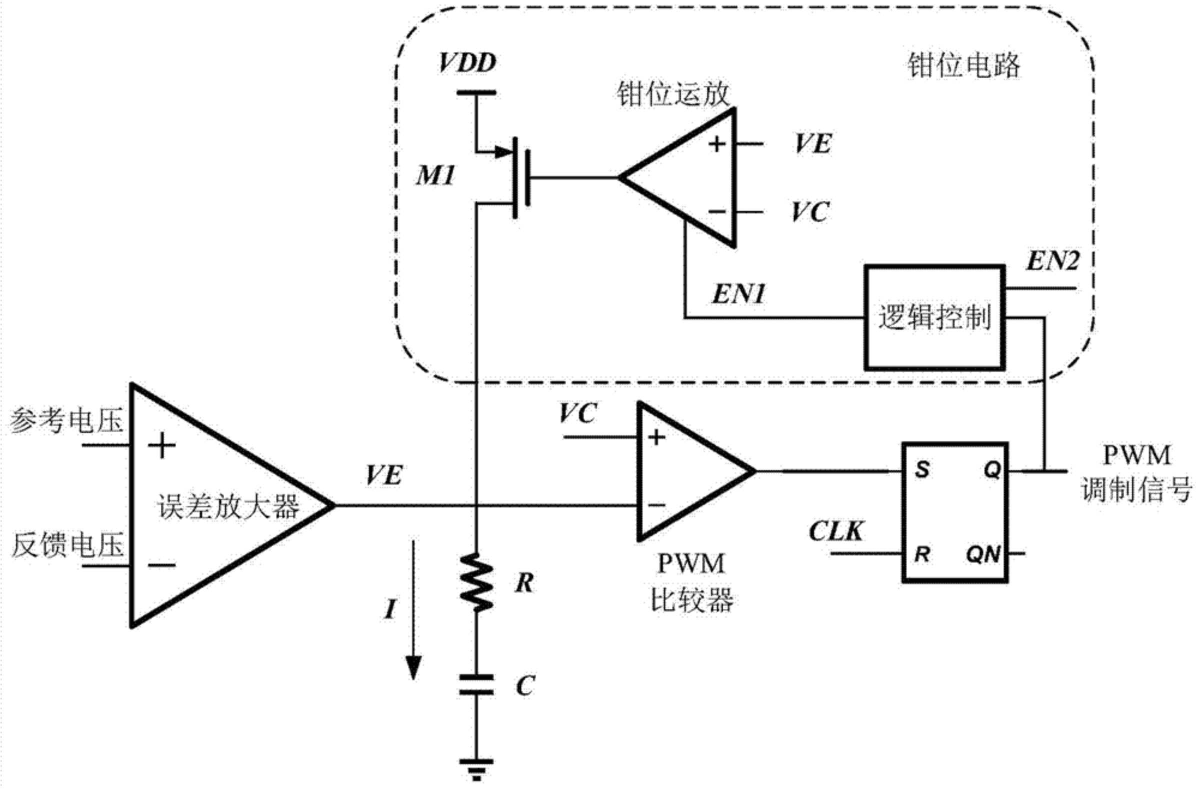
Abstract

(CN109375690)

The invention discloses a tandem type switch voltage stabilizing circuit. The circuit comprises a comparison amplifying circuit, a control circuit, a switch regulating circuit, an LC filter circuit, asampling circuit, an input voltage end and an output voltage end. The input voltage end, the switch regulating circuit, the LC filter circuit and the output voltage end are sequentially connected, the output voltage end is further connected with the sampling circuit, the sampling circuit feeds back sampling voltage to the comparison amplifying circuit, the comparison amplifying circuit is connected to the control circuit, the control circuit is connected to the control end of the switch regulating circuit, a transistor of the switch regulating circuit for regulating the output voltage mainlyworks in the two states of saturation connection and disconnection, due to the fact that the pipe voltage drop during saturation connection and the connection current during connection are both low, pipe consumption is low, the power efficiency is high, heating is small, no huge cooling device needs to be arranged, the size is small, and the weight is low.

Family 10/20 - FAMPAT - ©Questel

Images



Publication numbers

CN105099159

CN105099159

Publication kind codes

B

A

Publication dates

2017-08-29

2015-11-25

Earliest priority date

2015-08-21

Title

(CN105099159)

Quick starting circuit for DC-DC converter

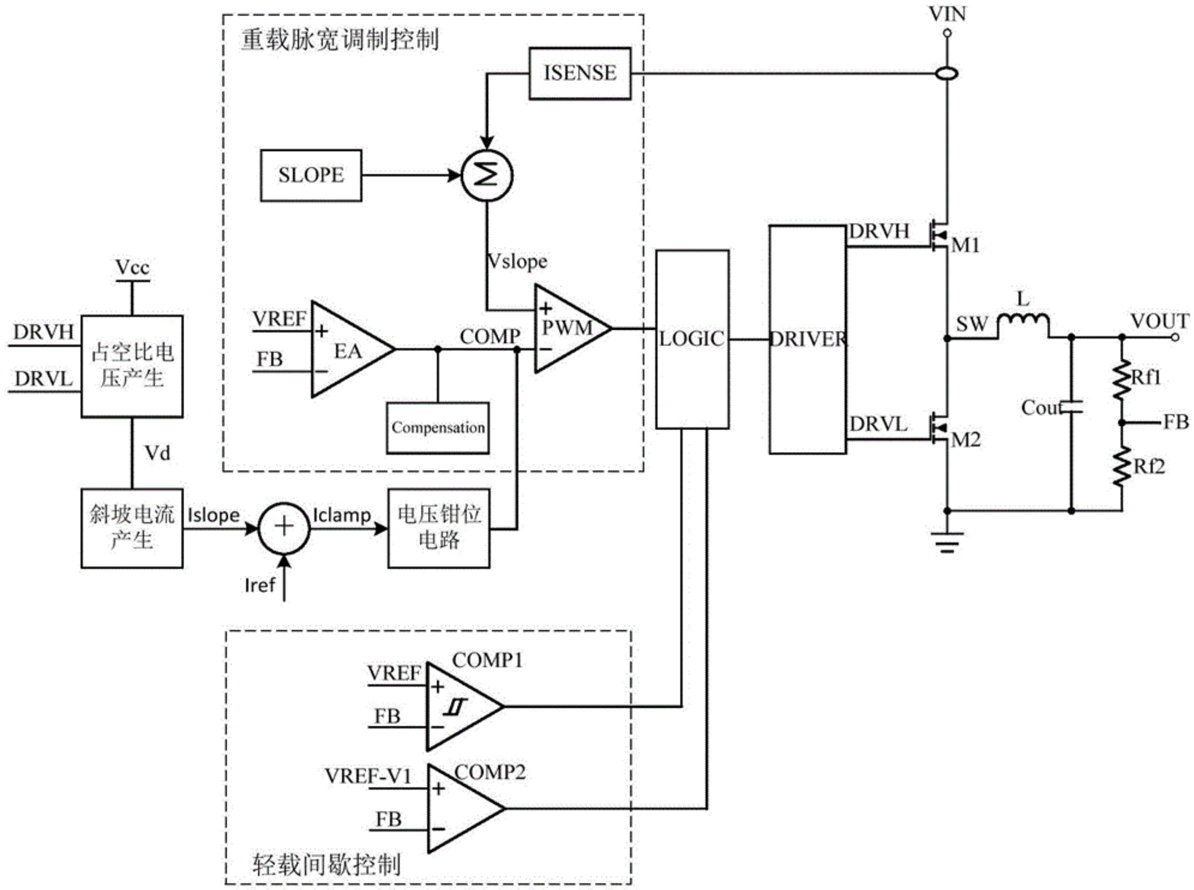
Abstract

(CN105099159)

The invention belongs to the electronic circuit technical field and relates to a quick starting circuit for a DC-DC converter. According to the quick starting circuit provided by the invention, a clamping circuit composed of an operational amplifier, a power switch tube and a logic control module is additionally adopted in a traditional DC converter control circuit; based on the clamping circuit, an error amplifier can output direct-current working voltage which is quickly clamped to load current sampling information, and therefore, starting can be accelerated; after detecting that the power switch tube is switched on for a plurality of times, a logic control circuit switches off the clamping circuit, so that the clamping circuit can be disconnected from a loop. With the quick starting circuit for the DC-DC converter of the invention adopted, the starting speed of the DC-DC converter can be effectively improved, and the starting time of the converter can be saved, and the converter can be more flexible; and when the converter works normally, the quick starting circuit of the invention can be disconnected from the loop, and therefore, the quick starting circuit will not affect the stability of the converter.

Family 11/20 - FAMPAT - ©Questel

Images



Publication numbers

CN110581639

Publication kind codes

A

Publication dates

2019-12-17

Earliest priority date

2019-09-04

Title

(CN110581639)

Quick response method and quick response circuit for light and heavy load mode switching of current type buck converter

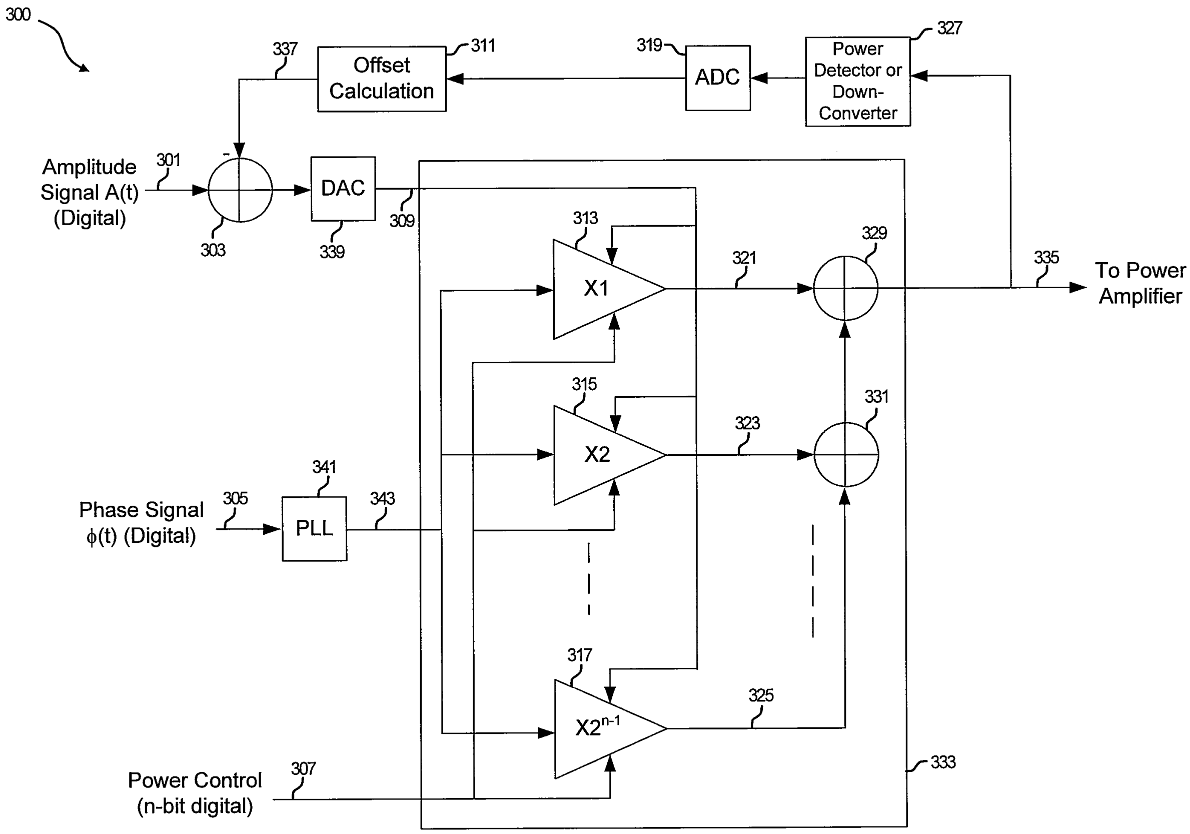
Abstract

(CN110581639)

The invention discloses a quick response method and a quick response circuit for light and heavy load mode switching of a current type buck converter. The method comprises steps that when the currenttype buck converter works in a light-load intermittent mode, a self-adaptive clamping voltage is generated through a self-adaptive COMP voltage clamping circuit according to different input voltages and an output voltage duty ratios to serve as initial voltage of a heavy-load pulse width modulation mode control circuit. The method is advantaged in that the response speed of switching from a lightload mode to a heavy load mode under different input voltage and output voltage conditions is increased, so performance of chips is improved, and smaller light load and heavy load mode switching output voltage ripples are realized.

Family 12/20 - FAMPAT - ©Questel

Images



Publication numbers

EP1931033

EP1931051

EP1933455

CN101212441

TWI477069

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US8948700

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US8838166

US8831543

CN101207399

US20140132346

US8676139

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Publication dates
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2008-06-11
2008-06-11

Earliest priority date

2006-12-06

Title

(EP1931053)

Method and system for shared high-power transmit path for a multi-protocol transceiver

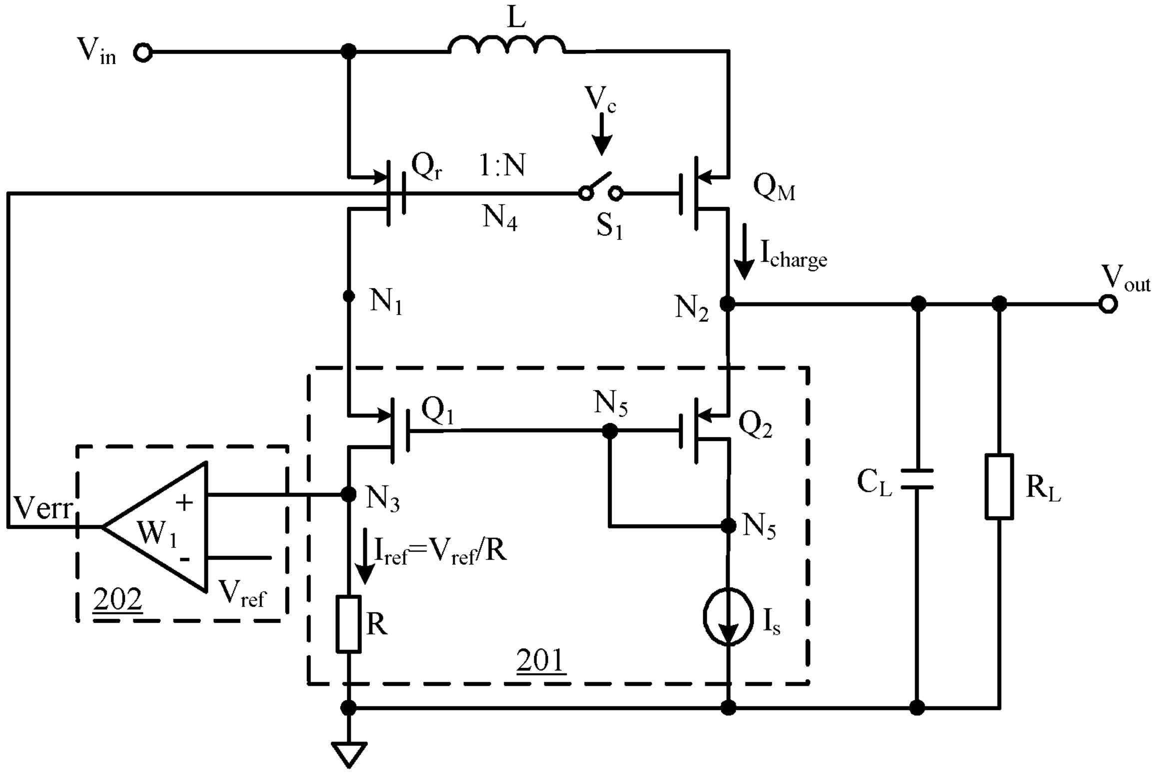
Abstract

(EP1931053)

Aspects of a method and system for a shared high-power transmit path for a multi-protocol transceiver are disclosed. Aspects of one method may include sharing a first power amplifier with a WLAN signal and a Bluetooth signal. The first power amplifier may amplify the WLAN signal and/or the Bluetooth signal simultaneously, or individually.

Family 13/20 - FAMPAT - ©Questel

Images



Publication numbers

US9214852

CN102624232

US20130278239

CN102624232

Publication kind codes

B2

B

A1

A

Publication dates

2015-12-15

2014-06-25

2013-10-24

2012-08-01

Earliest priority date

2012-04-20

Title

(US9214852)

Precharge circuits and methods for DC-DC boost converters

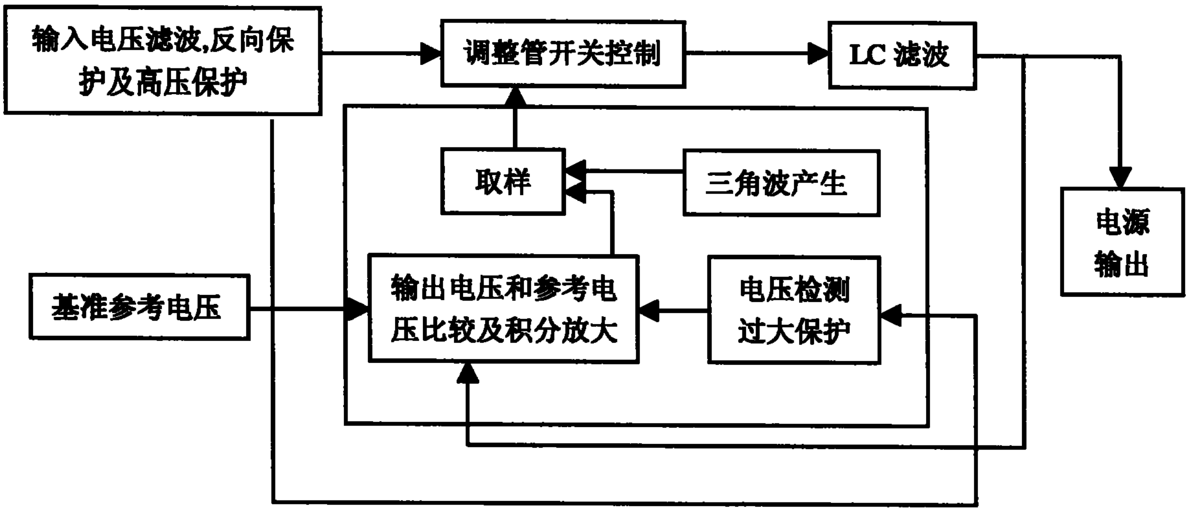
Abstract

(US20130278239)

The present invention discloses precharge circuits and methods for DC-DC boost converters. In one embodiment, a precharge method for a DC-DC boost converter having a current mirror circuit that includes a reference transistor and a power transistor, can include: (i) maintaining a reference current flowing through the reference transistor as substantially constant; (ii) maintaining a drain-source voltage of the reference transistor and a drain-source voltage of the power

transistor as substantially equal; and (iii) obtaining a substantially constant mirror current by reflecting the reference current through the power transistor to operate as a precharging current of a precharge circuit.

Images



Publication numbers

CN2927487

Publication kind codes

Y

Publication dates

2007-07-25

Earliest priority date

2006-01-19

Title

(CN2927487U)

DC converter with wide inputting-voltage range

Abstract

(CN2927487)

The utility model relates to a DC/DC conversion device with wide input voltage arrange, comprising an input filter and protection circuit, a norm reference voltage circuit and a triangle-wave generation circuit, the input voltage is passed through the input filter and protection circuit and then an over-voltage protection circuit, sampling is performed in the comparing circuit and is compared with the norm reference voltage value, the integral amplification is performed, then the amplified signal is outputted to the sampling circuit, the wave form generated by the triangle wave generation circuit is sampled and amplified, finally the square wave generated by the sampling circuit will control the switch of an adjusting tube to realize the stabilized output, so that the requirements of both the cost and the power supply quality are met.

Family 15/20 - FAMPAT - ©Questel

Images

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Publication numbers

US5912552

JP10225105

Publication kind codes

A

A

Publication dates

1999-06-15

1998-08-21

Earliest priority date

1997-02-12

Title

(US5912552)

DC to DC converter with high efficiency for light loads

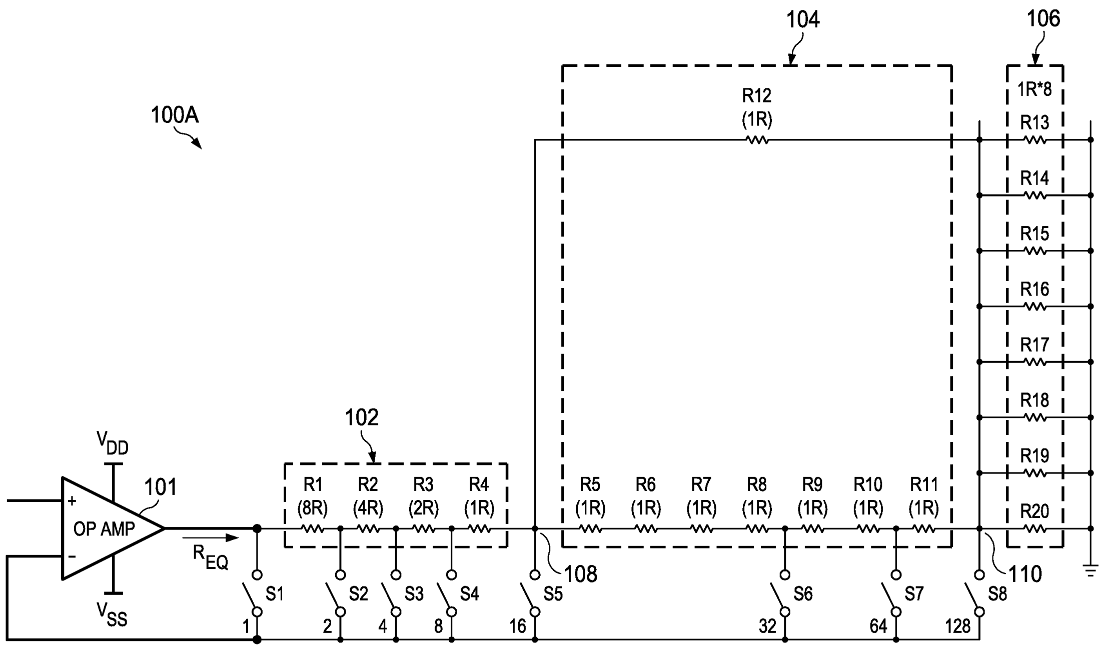
Abstract

(US5912552)

A DC to DC converter which maintains high efficiency over broad current ranges in a current mode switching regulator circuit without changing operational mode. A low ripple voltage is maintained over the entire load range and good voltage regulation is maintained with high efficiency. This is possible because the switching frequency is adjusted in accordance with the load without changing operational states, thus making it unnecessary to define plural states of operation. The timing of turning on the switch(es) varies since the switch(es) is (are) turned on when two set (ready) signals both become ready. For fixed frequency switching applications, switching pulses from a fixed frequency oscillator as a first set signal are skipped when a second set signal is not ready. On the other hand, for a variable frequency switching scheme which is implemented by driving the switching with a one-shot having a constant OFF time, the switching pulse is created after both set signals become active. A low pass filter is also used to dynamically adjust the minimum peak inductor current and to minimize ripple voltage for low load conditions so that a smaller output capacitor may be used.

Family 16/20 - FAMPAT - ©Questel

Images



Publication numbers

US10720937

CN111034035

US20190288702

US10312931

WO2019/056275

US20190089367

Publication kind codes

B2

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A1

B2

A1

A1

Publication dates

2020-07-21

2020-04-17

2019-09-19

2019-06-04

2019-03-28

2019-03-21

Earliest priority date

2017-09-21

Title

(WO201956275)

Programmable gain amplifier and delta sigma analog-to-digital converter containing pga

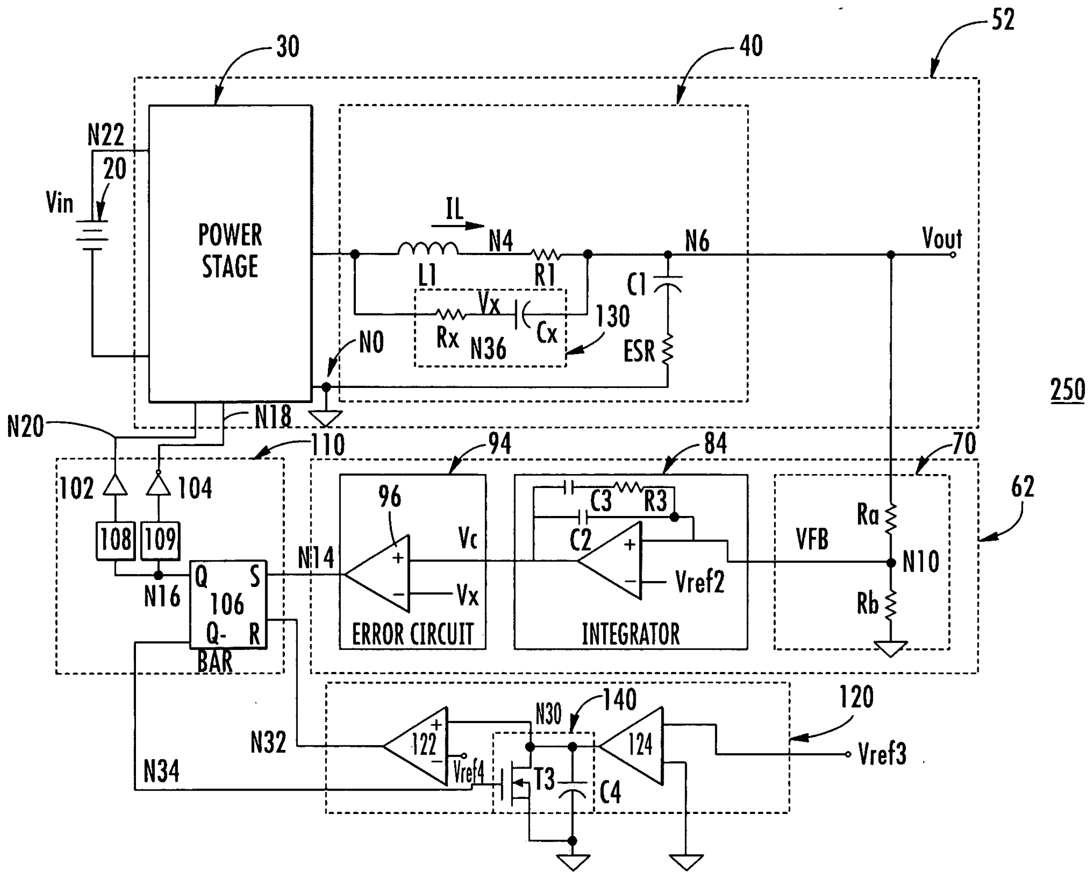
Abstract

(WO2019/056275)

A programmable gain amplifier (400A) includes an operational amplifier (402A) and a resistor network (405A) coupled to the output node (404A) of the operational amplifier. The resistor network includes a first plurality of resistors (410A) coupled in series between the output node and a first network node (406A). A second plurality of resistors (415A) is coupled in series between the first network node and a second network node (408A). A unit resistor (418A) is coupled in parallel with the second plurality of resistors between the first and second resistor network nodes and a third plurality of resistors (420A) is coupled in parallel between the second resistor network node and a reference voltage (VREF). Each resistor of the second and third pluralities of resistors comprises a unit resistor. The third plurality of resistors contains N resistors and the second plurality of resistors contains (N-1) resistors.

Family 17/20 - FAMPAT - ©Questel

Images



Publication numbers

US20050237037

Publication kind codes

A1

Publication dates

2005-10-27

Earliest priority date

2004-04-23

Title

(US20050237037)

Switching power supply controller system and method

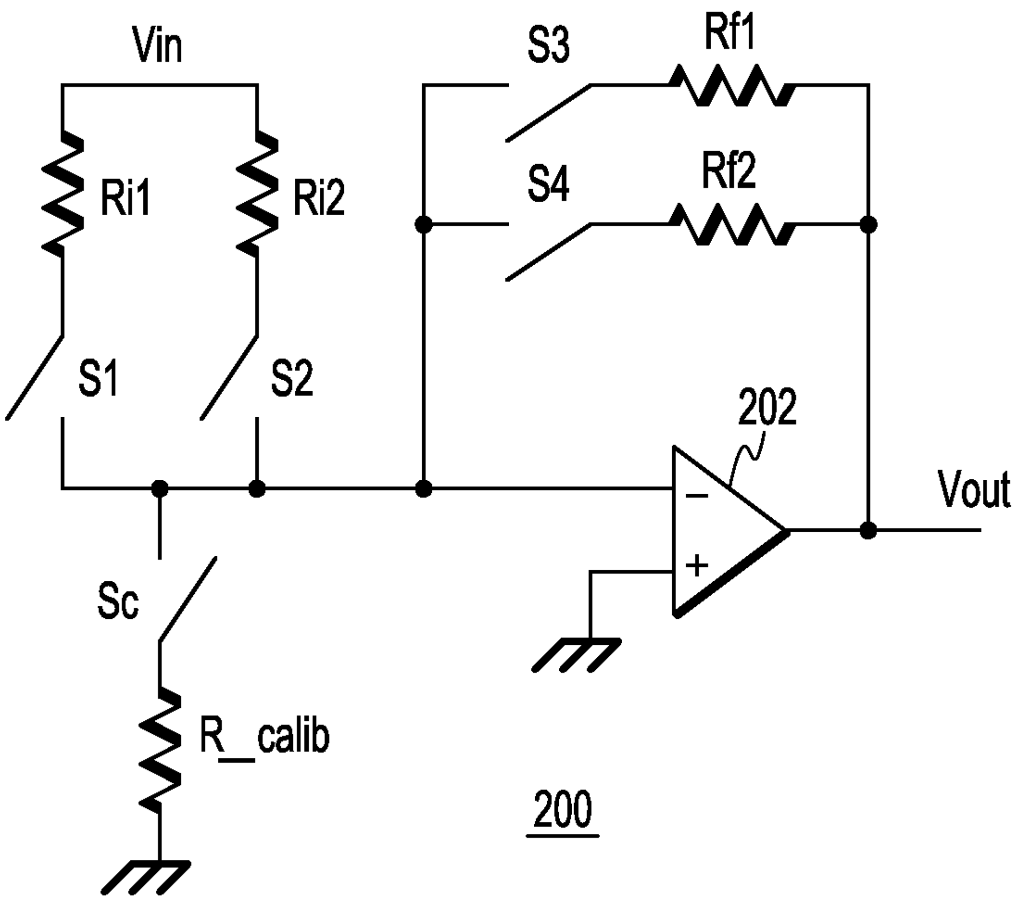
Abstract

(US20050237037)

A regulated output voltage is generated by a switching power supply having a constant voltage-second PWM control signal. During each switching cycle, a control circuit determines the pulse width such that a rapid response and light-load efficiency is provided. This control scheme can maintain accurate output voltage regulation at both light and heavy load conditions with small output voltage ripple. The control circuit also provides a constant switching frequency for a given input voltage and load.

Family 18/20 - FAMPAT - ©Questel

Images



Publication numbers

US9112465

US20150116035

Publication kind codes

B2

A1

Publication dates

2015-08-18

2015-04-30

Earliest priority date

2013-10-31

Title

(US9112465)

Digital calibration of programmable gain amplifiers

Abstract

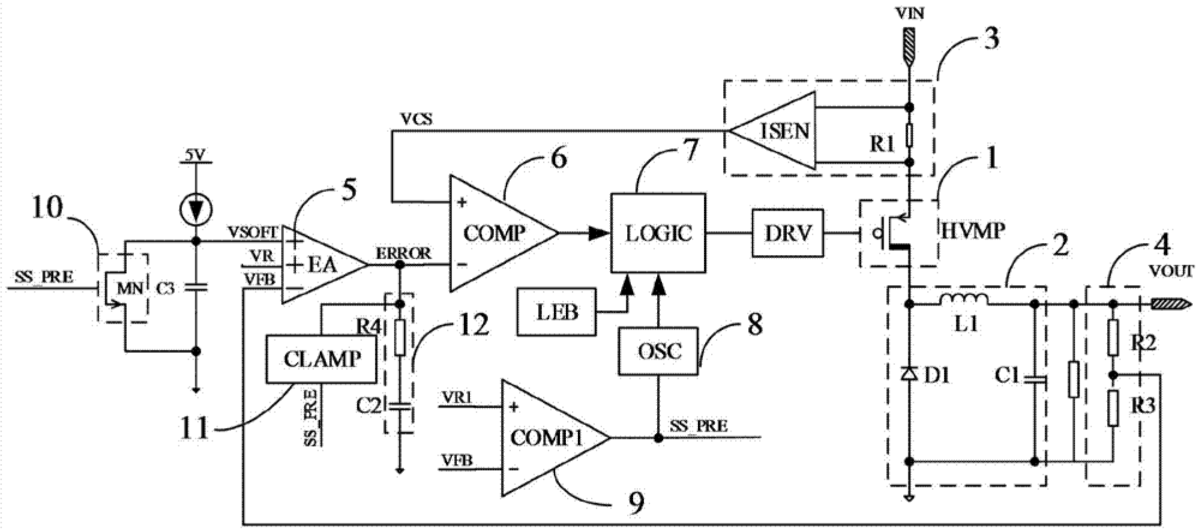
(US20150116035)

A programmable gain amplifier (PGA) includes an op amp, an input circuit, a feedback circuit, and a calibration circuit. The input circuit is connected between a PGA input node and an op-amp input node and selectively applies the analog input signal to the op-amp input node. The feedback circuit is connected between an op-amp output node and the op-amp input node and applies the amplified analog output signal as a feedback signal to the op-amp input node. The calibration circuit

is connected between a calibration reference node and the op-amp input node and selectively connects the calibration reference node directly to the op-amp input node without traversing any of the input circuit. The PGA may be implemented as a single-ended or differential amplifier. The PGA avoids reduced linearity resulting from series combinations of switches in the input circuit when configured for its normal operating mode.

Family 19/20 - FAMPAT - ©Questel

Images



Publication numbers

CN104753330

CN104753330

Publication kind codes

B

A

Publication dates

2018-02-23

2015-07-01

Earliest priority date

2015-04-08

Title

(CN104753330)

Soft start method of power management

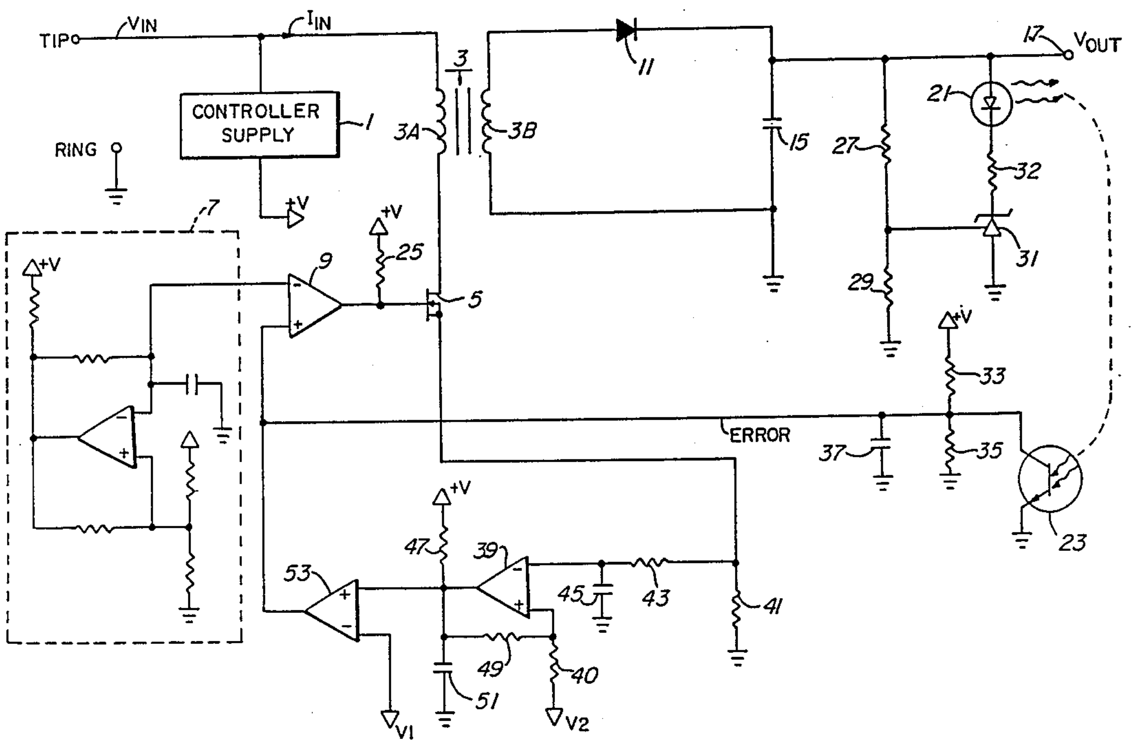
Abstract

(CN104753330)

The invention discloses a soft start circuit of power management, comprising a first switch tube, an energy conversion circuit, a sampling circuit, a feedback circuit, an error amplifying circuit, a first comparison circuit, a control circuit, an oscillation circuit, a second comparison circuit, a second switch tube and a clamp circuit. The control circuit adjusts a control signal output, according to a comparison result signal output by the first comparison circuit so as to adjust on and off of the first switch tube. On startup of a power supply, circuit current is easily deceased to zero by lowering oscillation frequency of the oscillation circuit, bypass start voltage and clamp error amplifying voltage, thus damage of power components caused by overshoot current is avoided.

Family 20/20 - FAMPAT - ©Questel

Images



Publication numbers

CA1287103

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US4761702

FR2599870

GB2191050

CN87100300

JPS62250827

DE3713378

GB8627880

IT8622486

Publication kind codes

C

B

B

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A1

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A1

D0

D0

Publication dates

1991-07-30

1990-09-19

1988-12-21

1988-08-02

1987-12-11

1987-12-02

1987-11-04

1987-10-31

1987-10-29

1986-12-31

1986-11-27

Earliest priority date

1986-04-22

Title

(US4761702)

CMOS latch-up recovery circuit

Abstract

(US4761702)

An overcurrent shut down circuit for use in a switching regulator power supply comprised of circuitry for detecting the average current of a pulse width modulated input signal, comparing the average current with a predetermined threshold level and reducing the duty cycle of the pulse width modulated signal to zero thereby shutting off the power supply, in the event the detected current exceeds the threshold level, indicating excess current being drawn from an output circuit of the supply. Time delay circuitry is provided for resetting the shut down circuit and restoring the regulator to normal operation after a predetermined amount of time as elapsed subsequent to the power supply being shut down. The overcurrent shut down circuit provides for recovery from CMOS latch-up and other excess current drawing fault conditions without requiring that the power supply be manually turned off. The circuit is of straightforward and inexpensive design and occupies very little circuit board area.