

1) Family number: 38524543 (US2007230640 AA)

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Title: HIGH DEFINITION MULTI-MEDIA INTERFACE

**Abstract:** A receiver for a multi-channel system such as a HDMI system is presented. In accordance with the present invention, the receiver receives one of the plurality of channels and includes an analog portion, a digital-to-analog converter, and a digital control block that provides digital control signals to the analog portion. Equalization can be accomplished partially or wholly in the analog domain and digitally controlled by a digital control loop. A digital equalizer can also be included. A decision feedback equalizer can be implemented that sums an analog output signal into the analog data stream. Timing recovery can be accomplished by digital control of a phase interpolator or delay locked loop that receives a plurality of phases from a timing circuit coupled to receive a clock signal.

Classifications:

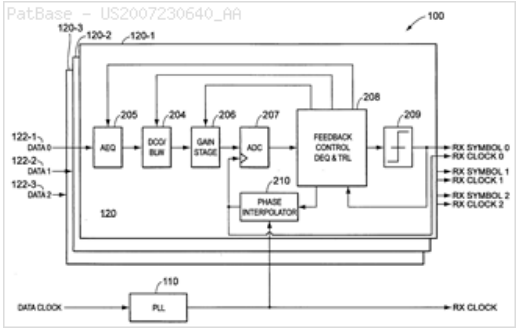
**International (IPC 8-9):** H04B1/06 H04B1/10 H04L27/02 H04L27/06 H04L27/08 H04N5/44 H04N7/173

**CPC:** H04L25/03057 H04L25/03878 H04L7/0062 H04L7/0334

**US:** 375/219 375/229 375/344 375/344S 375/345 375/345S 375/349 375/349P

**JP F-Term:** 5C025 5C164 5C025/BA18 5C025/BA21 5C025/DA08 5C164/UA21 5C164/UB71

**JP F-Index:** H04N21/426 H04N21/436 H04N5/44@Z H04N5/44,001 H04N7/173,630



Family:

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| JP2009531974 T2    | 20090903         | JP20090502871T     | 20070321         |
| KR101361364 B1     | 20140210         | KR20087025680      | 20070321         |
| KR20090008252 A    | 20090121         | KR20087025680      | 20070321         |
| US2007230640 AA    | 20071004         | US20060391903      | 20060328         |
| US7746969 BB       | 20100629         | US20060391903      | 20060328         |
| WO07126675 A2      | 20071108         | WO2007US07132      | 20070321         |
| WO07126675 A3      | 20080703         | WO2007US07132      | 20070321         |

Priority:

US20060391903 20060328 WO2007US07132 20070321

**Probable Assignee:** ENTROPIC COMMUNICATIONS LLC

**Assignee(s):** (std): BRYAN THOMAS ; ENTROPIC COMMUNICATIONS INC ; MANICKAM THULASINATH ; MANICKAM TULSI ; RAGHAVAN SREEN ; RAGHAVAN SREEN ; SALLAWAY PETER ; VATIV TECHNOLOGIES INC ; WEBB STEWART

**Assignee(s):** ENTROPIC COMMUNICATIONS LLC ; JPMORGAN CHASE BANK NA COLLATERAL AGENT AS ; MUFG UNION BANK NA

**Inventor(s):** (std): BRYAN THOMAS ; MANICKAM THULASINATH ; MANICKAM TULSI ; RAGHAVAN SREEN ; RAGHAVAN SREEN ; SALLAWAY PETER ; WEBB STEWART

**Agent(s):** BRUCE W; FINNEGAN HENDERSON FARABOW GARRETT AND DUNNER LLP; FINNEGAN HENDERSON FARABOW GARRETT AND DUNNER, LLP

**Designated states:** AE AG AL AM AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN SV SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

2) Family number: 41848942 (US2008123729 AA)

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Title: ADAPTIVE CABLE EQUALIZER

**Abstract:** An adaptive cable equalizer includes a data signal input unit, a clock signal input unit, a variable equalizer that inputs a data signal input from the data signal input unit, and a transition time measuring portion that measures a transition time of a data signal output from the variable equalizer, with an equalizer control loop being configured that controls characteristics of the variable equalizer based on the output signal of the transition time measuring portion. The adaptive cable equalizer further includes a control circuit that controls response characteristics of the control loop according to the frequency of a clock signal input from the clock signal input unit. This enables a quick response at fast transfer rates by making the relationship between the response time of the control loop and the number of data bits substantially constant even when the transfer rate changes from a slow transfer rate to a fast transfer rate.

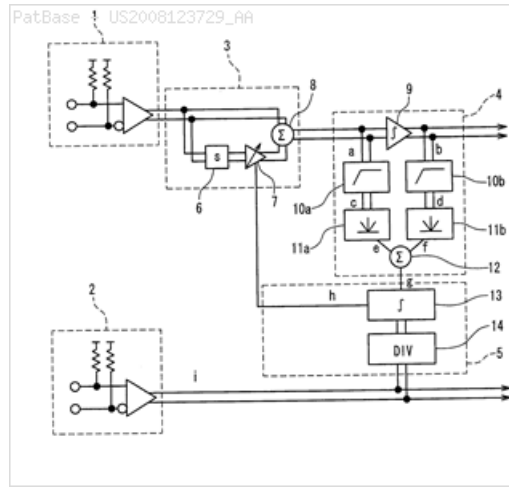
Classifications:

**International (IPC 8-9):** H03H7/30 H04B3/04 H04L27/01

**CPC:** H04L25/03885

**US:** 333/171 333/174 333/18 375/229 375/230 375/231 375/232

375/232P 375/316 375/317 375/376 375/376S  
**JP F-Term:** 5K004 5K046 5K004/AA01 5K004/BD01 5K046/AA01  
 5K046/EE05 5K046/EE46  
**JP F-Index:** H04B3/04@A H04L27/00@K H04L27/01



#### Family:

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| JP2008135947 A2        | 20080612         | JP20060320282      | 20061128         |
| <b>US2008123729 AA</b> | 20080529         | US20070946381      | 20071128         |
| <b>US8155179 BB</b>    | 20120410         | US20070946381      | 20071128         |

#### Priority:

JP20060320282 20061128

**Probable Assignee:** PANASONIC CORP

**Assignee(s):** (std): KOBAYASHI HITOSHI ; MATSUSHITA ELECTRIC IND CO LTD ; PANASONIC CORP

**Assignee(s):** MATSUSHITA ELECTRIC INDUSTRIAL CO ; MATSUSHITA ELECTRIC INDUSTRIAL CO LTD

**Inventor(s):** (std): KOBAYASHI HITOSHI

**Agent(s):** HAMRE SCHUMANN MUELLER AND LARSON PC ; IKEUCHI SATO AND PARTNER PATENT ATTORNEYS

### 3) Family number: 66152654 (US2017180002 AA)

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**Title:** M-ARY PULSE AMPLITUDE MODULATION DIGITAL EQUALIZER

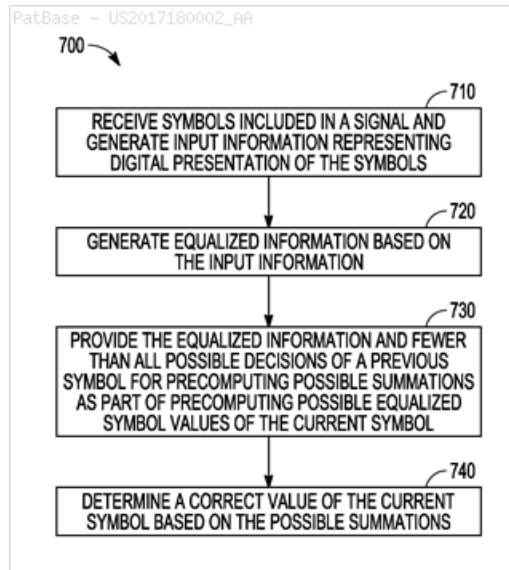
**Abstract:** Some embodiments include apparatus and methods using an input node, an analog to digital converter (ADC) including an input coupled to the input node, a first feedforward equalizer (FFE) including an input coupled to an output of the ADC, a second FFE including an input coupled to the output of the ADC, and a decision feedback equalizer (DFE) including a first input, a second input, and an output, the first input coupled to an output of the first FFE, and the second input coupled to an output of the second FFE.

#### Classifications:

**International (IPC 8-9):** H04B1/00 H04B1/12 H04B14/02 H04B3/14 H04L25/03 H04L25/49

**CPC:** H04B1/0007 H04B1/123 H04B14/023 H04B3/145 H04L25/03878

**US:** 1/1 375/233



#### Family:

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| <b>CN107026658 A</b>   | 20170808         | CN201611049785     | 20161117         |
| CN107026658 B          | 20191119         | CN201611049785     | 20161117         |
| US10263663 BB          | 20190416         | US20150973163      | 20151217         |
| <b>US2017180002 AA</b> | 20170622         | US20150973163      | 20151217         |
| <b>WO17105752 A1</b>   | 20170622         | WO2016US62509      | 20161117         |

**Priority:**

US20150973163 20151217

**Probable Assignee:** INTEL CORP**Assignee(s):** (std): INTEL CORP ; INTEL IP CORP**Inventor(s):** (std): HSUEH TZU CHIEN ; JAUSSE JAMES E ; KIRAN SHIVA**Agent(s):** PERDOK MONIQUE M ET AL; SCHWEGMAN LUNDBERG AND WOESSNER PA

**Designated states:** AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DJ DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KW KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

**4) Family number: 44816577 (US2010080111 AA)**

© PatBase

**Title:** METHOD AND SYSTEM FOR ETHERNET SWITCHING, CONVERSION, AND PHY OPTIMIZATION BASED ON LINK LENGTH IN AUDIO/VIDEO SYSTEMS

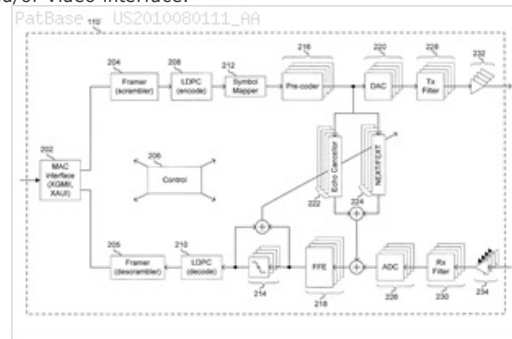
**Abstract:** Aspects of a method and system for Ethernet Switching, Conversion, and PHY optimization based on link length in Audio/Video Systems are provided. In this regard, the length of a link over which a first communication device communicates with a second communication device may be determined and Ethernet PHY's residing in the communication devices may be configured based on the determination. One or both of the communication devices may comprise an Ethernet switch operable to switch packetized audio and/or video content. The packetized audio and/or video may be switched between the configured Ethernet PHY and one or more other Ethernet PHYs. Audio and/or video data may be received via the one or more corresponding Ethernet PHYs, the received audio and/or video data may be reformatted to be compatible with an audio and/or video interface, and the reformatted audio and/or video data may be transmitted via the audio and/or video interface.

**Classifications:****International (IPC 8-9):** H04J3/02 H04J3/10 H04J3/14 H04L12/56**CPC:** H04B3/23 H04B3/32 H04L2025/03356 H04L2025/03535

H04L25/03006 H04L41/0803

**US:** 370/201 370/201P 370/252 370/287 370/290 370/389 370/389S

370/465 725/127

**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| <b>US2010080111 AA</b> | 20100401         | US20090495496      | 20090630         |
| <b>US8565105 BB</b>    | 20131022         | US20090495496      | 20090630         |

**Priority:**

US20080101072P 20080929 US20090495496 20090630

**Probable Assignee:** AVAGO TECHNOLOGIES LTD**Assignee(s):** (std): BROADCOM CORP ; BROWN KEVIN ; DIAB WAEEL WILLIAM ; POWELL SCOTT ; TEENER MICHAEL JOHAS

**Assignee(s):** AVAGO TECHNOLOGIES GENERAL IP SINGAPORE PTE LTD ; AVAGO TECHNOLOGIES INT SALES PTE LTD ; AVAGO TECHNOLOGIES LTD ; BANK OF AMERICA NA COLLATERAL AGENT AS

**Inventor(s):** (std): BROWN KEVIN ; DIAB WAEEL WILLIAM ; POWELL SCOTT ; TEENER MICHAEL JOHAS**Agent(s):** FARJAMI AND FARJAMI LLP; MCANDREWS HELD AND MALLOY LTD**5) Family number: 51430559 (US2012170637 AA)**

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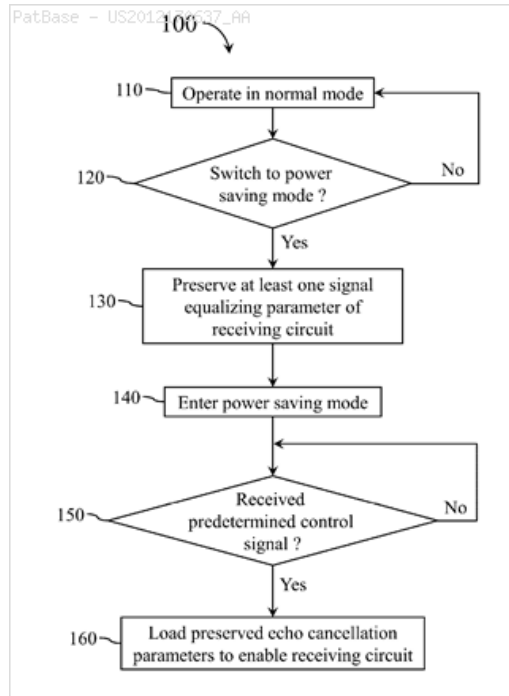
**Title:** METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION OF COMMUNICATION DEVICE

**Abstract:** A communication device is disclosed including: an analog-to-digital converter (ADC) for converting an analog input signal into a digital input signal; an equalizer module coupled with the ADC for processing the digital input signal to generate an equalized signal; a data slicer coupled with the equalizer module for generating an output signal based on the equalized signal; and a control unit coupled with the equalizer module and the data slicer; wherein the control unit or the equalizer module preserves at least one signal equalizing parameter of the equalizer module before the equalizer module enters power saving mode, and the equalizer module loads the at least one signal equalizing parameter to operate when the communication device receives a predetermined control signal.

**Classifications:****International (IPC 8-9):** H03H7/30 H03H7/40 H04L12/10 H04L12/28

H04L27/01 H04L7/00

**CPC:** H04L25/03057 H04N21/4383 H04N21/4432 H04N5/211**US:** 375/231 375/231P 375/232 375/232S 375/350

**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| <b>CN102571366 A</b>   | 20120711         | CN201110046911     | 20110225         |
| CN102571366 B          | 20161214         | CN201110046911     | 20110225         |
| <b>TW201228284 A</b>   | 20120701         | TW20100146590      | 20101229         |
| <b>TWI462519 B</b>     | 20141121         | TW20100146590      | 20101229         |
| <b>US2012170637 AA</b> | 20120705         | US20110336690      | 20111223         |
| <b>US8787436 BB</b>    | 20140722         | US20110336690      | 20111223         |

**Priority:**

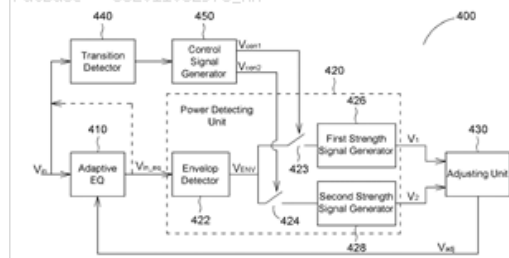
TW20100146590 20101229

**Probable Assignee:** REALTEK SEMICONDUCTOR CORP**Assignee(s):** (std): HUANG LIANG WEI ; LEE CHIEN SHENG ; REALTEK SEMICONDUCTOR CORP ; RUIYU SEMICONDUCTOR CO LTD ; WANG FANG RU ; YU TING FA**Assignee(s):** RUIYU SEMICONDUCTOR CO**Inventor(s):** (std): CHIEN SHENG LEE ; FANG RU WANG ; HUANG LIANG WEI ; LEE CHIEN SHENG ; LIANG WEI HUANG ; TING FA YU ; TING YU FA ; WANG FANG RU ; YU TING FA**Agent(s):** BIRCH STEWART KOLASCH AND BIRCH LLP**6) Family number: 48276907 (US2011032978 AA)**

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**Title:** RECEIVER AND METHOD FOR ADJUSTING ADAPTIVE EQUALIZER OF RECEIVER

**Abstract:** A receiver includes an adaptive equalizer, a power detecting unit and an adjusting unit. The adaptive equalizer is for receiving a signal and generating an equalized signal. The power detecting unit, coupled to the adaptive equalizer, is for detecting the strength of the equalized signal during a first period to generate a first strength signal, and detecting the strength of the equalized signal during a second period to generate a second strength signal. The adjusting unit, coupled to the power detecting unit and the adaptive equalizer, is for adjusting the compensation strength for the adaptive equalizer according to the first and second strength signals.

**Classifications:****International (IPC 8-9):** H03H7/30 H03H7/40 H03K5/159 H04L25/03 H04L27/01**CPC:** H04L25/03076**US:** 375/229 375/230 375/232 375/232P 382/270 455/240.1**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| TW201106662 A          | 20110216         | TW20090126372      | 20090805         |
| TWI440339 B            | 20140601         | TW20090126372      | 20090805         |
| <b>US2011032978 AA</b> | 20110210         | US20100769905      | 20100429         |

|              |          |               |          |
|--------------|----------|---------------|----------|
| US8532168 BB | 20130910 | US20100769905 | 20100429 |
|--------------|----------|---------------|----------|

**Priority:**

TW20090126372 20090805

**Probable Assignee:** MSTAR SEMICONDUCTOR INC

**Assignee(s):** (std): LIN PO NIEN ; MSTAR SEMICONDUCTOR INC ; SMITH STERLING

**Assignee(s):** MEDIATEK INC

**Inventor(s):** (std): LIN PO NIEN ; SMITH STERLING

**Agent(s):** JUSTIN; WPAT PC; WPAT PC INTELLECTUAL PROPERTY ATTORNEYS

**7) Family number: 50793861 (US2012070004 AA)**

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**Title:** DIGITAL AUDIO DISTRIBUTION

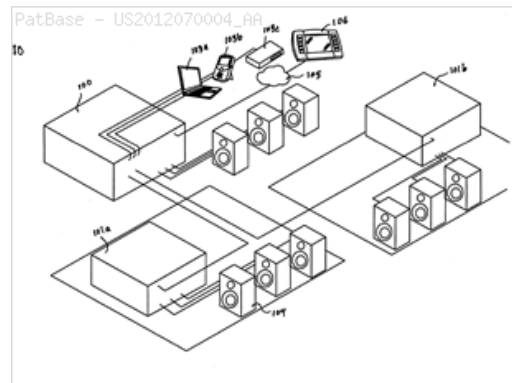
**Abstract:** A master transmitter distributes a plurality of audio channels to one or more expansion receivers as a multiplexed audio stream. Control information is also transmitted between the master transmitter and the expansion receivers. Both the control information and the multiplexed audio stream are transmitted on the same cable allowing for reduced clutter and cheaper material and installation costs.

**Classifications:**

**International (IPC 8-9):** H04B3/00 H04H20/30 H04H20/63 H04H20/82 H04H20/88 H04J3/00 H04J3/02 H04R5/00

**CPC:** H04H20/30 H04H20/63 H04H20/82 H04J3/02 H04R5/00

**US:** 1/1 370/498 370/535 381/2 381/2P 381/80 381/80S



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| US2012070004 AA    | 20120322         | US20110241052      | 20110922         |
| US8837529 BB       | 20140916         | US20110241052      | 20110922         |
| US2014334625 AA    | 20141113         | US20140339977      | 20140724         |
| US9301051 BB       | 20160329         | US20140339977      | 20140724         |

**Priority:**

US20100385364P 20100922

US20110241052 20110922

US20140339977 20140724

**Probable Assignee:** CRESTRON ELECTRONICS INC

**Assignee(s):** (std): CRESTRON ELECTRONICS INC ; LABOSCO MARK ; PAGANO DARIO

**Inventor(s):** (std): LABOSCO MARK ; PAGANO DARIO

**Agent(s):** CRESTRON ELECTRONICS INC

**8) Family number: 51776565 (US2012213256 AA)**

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**Title:** TRANSCEIVER DEVICE AND RELATED METHOD THEREOF

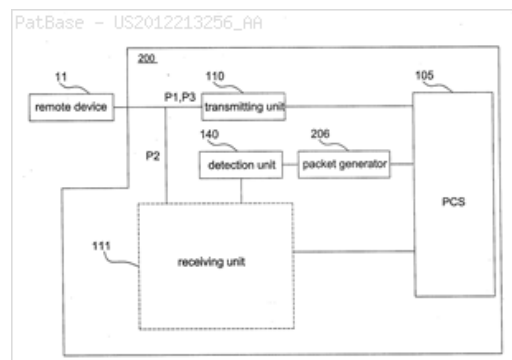
**Abstract:** A transceiver device includes a transmitting unit, a receiving unit, and a detection unit. The transmitting unit transmits a first packet; the receiving unit receives a second packet and at least one receiving parameter; the detection unit is coupled to the transmitting unit and the receiving unit, and detects the first and the second packets to adjust the receiving parameter. When the detection unit detects that the first and the second packets are substantially the same, the detection unit pauses adjusting the receiving parameter.

**Classifications:**

**International (IPC 8-9):** H04B1/10 H04B1/38 H04B17/00 H04L5/16

**CPC:** H04W52/52

**US:** 375/219 375/219P



**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| TW201236383 A          | 20120901         | TW20110105911      | 20110223         |
| TWI445327 B            | 20140711         | TW20110105911      | 20110223         |
| <b>US2012213256 AA</b> | 20120823         | US20120402286      | 20120222         |
| <b>US8675716 BB</b>    | 20140318         | US20120402286      | 20120222         |

**Priority:**

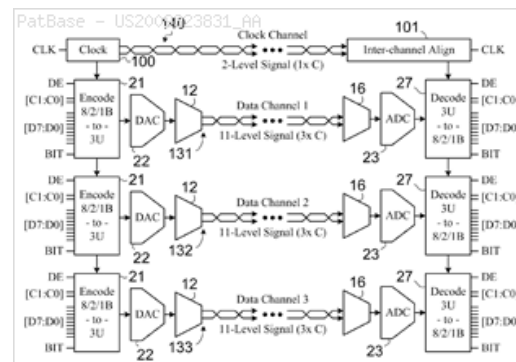
TW20110105911 20110223

**Probable Assignee:** REALTEK SEMICONDUCTOR CORP**Assignee(s):** (std): CHO WEN JEN ; HUANG LIANG WEI ; KUO SHIEH HSING ; LIU CHUN HUNG ; REALTEK SEMICONDUCTOR CORP**Inventor(s):** (std): CHO WEN JEN ; HUANG LIANG WEI ; KUO SHIEH HSING ; LIU CHUN HUNG**Agent(s):** MUNCY GEISSLER OLDS AND LOWE PC**9) Family number: 44152707** (US2009323831 AA)

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**Title:** DIGITAL VIDEO PHYSICAL LAYER USING A MULTI-LEVEL DATA CODE

**Abstract:** Digital video data is transmitted from a video source (61) to a video sink (62) as a group of three multilevel symbols (611, 612, and 613) per pixel color with each associated symbol being sent at a rate of three times the pixel clock (601). When eleven levels are used per symbol (611) and undesirable symbol groups having excess DC residual or minimal energy are eliminated, and a built-in-test symbol group is added for pixel alignment; there results a one-to-one correspondence between the remaining symbol groups available and the two-hundred and sixty possible states that are used in the TMDS physical layer that is in widespread commercial use.

**Classifications:****International (IPC 8-9):** H03M7/00 H04B3/00 H04B3/50 H04L25/49**CPC:** G09G2370/12 G09G5/008 H03M5/145 H04L25/0272 H04L25/49 H04N21/4122 H04N21/43632**US:** 327/52 341/143 341/52 341/52S 375/257 375/257S 375/258 375/258P 375/286 375/287 375/288 375/288S 375/293 375/293S**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| <b>US2009323831 AA</b> | 20091231         | US20080163409      | 20080627         |
| <b>US8081705 BB</b>    | 20111220         | US20080163409      | 20080627         |
| <b>US2012057642 AA</b> | 20120308         | US20110293737      | 20111110         |
| <b>US8798189 BB</b>    | 20140805         | US20110293737      | 20111110         |

**Priority:**

US20080163409 20080627 US20110293737 20111110

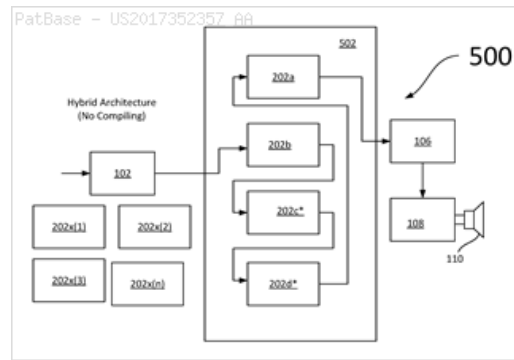
**Probable Assignee:** CRESTRON ELECTRONICS INC**Assignee(s):** (std): CRESTRON ELECTRONICS INC ; KIRKPATRICK PHILIP L**Inventor(s):** (std): KIRKPATRICK PHILIP L**Agent(s):** CRESTRON ELECTRONICS INC; CRESTRON ELECTRONICS INC ATTN PHILIP KIRKPATRICK**10) Family number: 67745817** (US2017352357 AA)

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**Title:** AUDIO DIGITAL SIGNAL PROCESSOR UTILIZING A HYBRID NETWORK ARCHITECTURE

**Abstract:** A system and method executed by audio processing software on one or more electronic devices in a computer system to process digital audio signals. The system comprises a digitizer for digitizing a received audio signal; and processor for performing a plurality of audio processing functions on the digitized audio signals, each of the audio processing functions having at least one programmable parameter, and wherein each of the audio processing functions are categorized and grouped as audio objects, and organized into a channel strip, the channel strip processing digitized audio signals for a particular received audio signal, and wherein, the audio objects are fixed in order, so that the digitized received audio signals are processed by a predefined number of N audio objects, and wherein the N audio objects occur in a fixed sequence, and further wherein, the N audio objects comprise a first subset of non-exchangeable audio objects and a second subset of exchangeable audio objects, such that any one or more of the second subset of audio objects can be exchanged by a replacement audio object, and further wherein when the audio processing functions are programmed, they can be saved without compiling the audio processing software.

**Classifications:****International (IPC 8-9):** G06F3/16 G06J1/00 G10L19/02 H04L12/64**CPC:** G06F3/162 G06F3/165 H04R2420/01 H04S2400/03**US:** 1/1 700/94



**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| US10474419 BB          | 20191112         | US20170614006      | 20170605         |
| <b>US2017352357 AA</b> | 20171207         | US20170614006      | 20170605         |
| US2020065054 AA        | 20200227         | US20190671688      | 20191101         |

**Priority:**

US20160345326P 20160603      US20170614006 20170605      US20190671688 20191101

**Probable Assignee:**

CRESTRON ELECTRONICS INC

**Assignee(s):** (std):

CRESTRON ELECTRONICS INC

**Inventor(s):** (std):

FINK DENNIS

**Agent(s):**

CRESTRON ELECTRONICS INC

**11) Family number: 65317939** (US2017091516 AA)

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**Title:** ASYNCHRONOUS ON-DIE EYE SCOPE

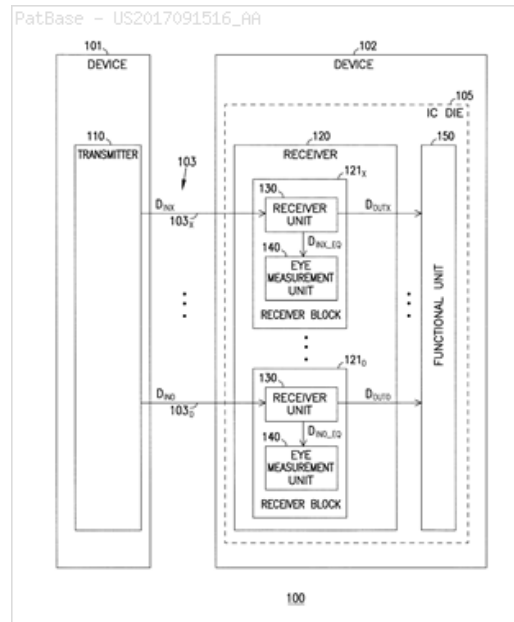
**Abstract:** Some embodiments include apparatuses and methods having a receiver unit included in a die and a measurement unit included in the die. The receiver unit includes a sampler to sample a first signal based on timing of a first clock signal to generate a second signal. The measurement unit is arranged to sample the first signal based on timing of a second clock signal to provide information for generation of a graph presenting an eye scan of the first signal. The second clock signal has a frequency asynchronous with a frequency of the first clock signal.

**Classifications:**

**International (IPC 8-9):** G01R13/02 G01R31/317 G06K9/00 H04L27/14

**CPC:** G01R13/02 G01R31/3171 G06K9/00503 G06K9/0053 G06K9/00557 G06K9/00604

**US:** 1/1 348/78



**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| CN107923941 A          | 20180417         | CN201680049230     | 20160824         |
| EP3353562 A1           | 20180801         | EP20160849260      | 20160824         |
| EP3353562 A4           | 20190522         | EP20160849260      | 20160824         |
| <b>US2017091516 AA</b> | 20170330         | US20150865401      | 20150925         |
| US9922248 BB           | 20180320         | US20150865401      | 20150925         |
| <b>WO17052930 A1</b>   | 20170330         | WO2016US48464      | 20160824         |

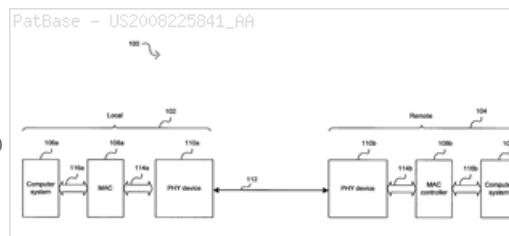
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US20150865401 20150925      WO2016US48464 20160824

**Designated states:** AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QZ RO RS RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

**Abstract:** Aspects of a method and system for low power IDLE signal transmission in Ethernet networks are provided. In this regard, during time periods between transmissions of actual data by a local Ethernet link partner, the local Ethernet Link partner may generate one or more signals, in place of a standard Ethernet IDLE signal, that enable synchronization between Ethernet link partners. In this manner, the generated signals may enable reducing power consumption as compared to standard Ethernet IDLE signals. Accordingly, link activity may be monitored to enable detecting periods when there may be no actual data for transmission and the generated signals may be transmitted. The generated signals may be transmitted at a reduced symbol rate as compared to standard Ethernet IDLE signals. The generated signals may be transmitted via fewer network links as compared to standard Ethernet IDLE signals.

**International (pc 8-9):** A61K31/513 A61K31/58 A61K31/7008  
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A61K36/24 A61K45/06 A61P15/00 A61P17/06 A61P19/02 A61P19/10  
A61P25/00 A61P27/02 A61P29/00 A61P35/00 A61P37/08 A61P9/10  
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LLP; PAUL M H; RICK; VON KREISLER SELTING WERNER; VON KREISLER SELTING WERNER  
PARTNERSCHAFT VON PATENTANWALTEN U RECHTSANWALTEN MBB; WATERMARK INTELLECTUAL  
PROPERTY PTY LTD; WATERMARK PATENT AND TRADE MARKS ATTORNEYS

**Designated states:** AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ  
DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP  
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NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TJ TM  
TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW

**13) Family number: 42270804** (US2008247452 AA)

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**Title:** ADAPTIVE EQUALIZER FOR USE WITH CLOCK AND DATA RECOVERY CIRCUIT OF SERIAL COMMUNICATION LINK

**Abstract:** An adaptive equalizer system for use in a serial communication link uses timing information generated by a phase detector of a clock and data recovery circuit of the serial communication link and a frequency pattern of the recovered data to determine whether the data received over the serial communication link is over-equalized or under-equalized. The equalizer strength of the adaptive equalizer system is adjusted based on such determination.

**Classifications:**

**International (IPC 8-9):** H03H7/38 H03H7/40 H03K5/159 H04B3/04

H04B7/005 H04L25/03 H04L27/01 H04L7/02 H04L7/033

**CPC:** H04L2025/03356 H04L2025/03598 H04L25/03019 H04L25/03885

H04L7/0004 H04L7/033

**US:** 375/232 375/232P 375/233 375/294 375/362 375/362S 375/371

375/373 375/377

**JP F-Term:** 5K029 5K046 5K047 5K029/AA03 5K029/BB03 5K029/FF10

5K029/HH05 5K029/HH06 5K029/HH26 5K029/LL12 5K046/BA01

5K046/EE05 5K046/EE32 5K046/EE48 5K046/EF52 5K046/EF55

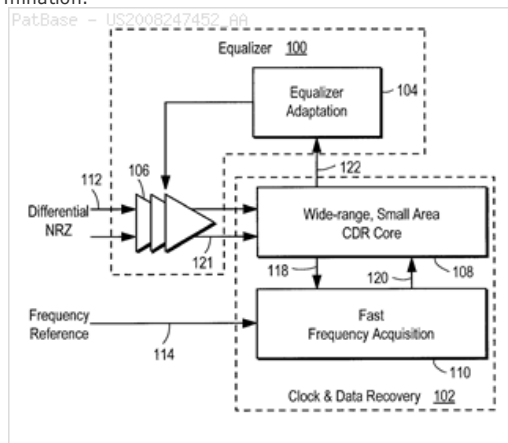
5K047/AA06 5K047/GG09 5K047/GG11 5K047/GG14 5K047/GG24

5K047/GG45 5K047/MM60 5K029/KK22 5K029/KK26 5K046/EE47

5K046/EF53

**JP F-Index:** H04B3/04@A H04B7/005 H04L25/03@C H04L7/00,040

H04L7/02@Z H04L7/033



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| CN101286959 A      | 20081015         | CN200810091708     | 20080409         |
| CN101286959 B      | 20110831         | CN200810091708     | 20080409         |
| JP2008263606 A2    | 20081030         | JP20080101005      | 20080409         |
| JP5372400 B2       | 20131218         | JP20080101005      | 20080409         |
| JP2014039292 A2    | 20140227         | JP20130193256      | 20130918         |
| JP5705286 B2       | 20150422         | JP20130193256      | 20130918         |
| KR100965964 B1     | 20100624         | KR20080032094      | 20080407         |
| KR20080091712 A    | 20081014         | KR20080032094      | 20080407         |
| TW200843383 A      | 20081101         | TW20080112651      | 20080408         |
| TWI514798 B        | 20151221         | TW20080112651      | 20080408         |
| US2008247452 AA    | 20081009         | US20070865621      | 20071001         |
| US7916780 BB       | 20110329         | US20070865621      | 20071001         |

**Priority:**

US20070910773P 20070409 US20070865621 20071001 JP20080101005 20080409

**Probable Assignee:** SYNERCHIP CO LTD

**Assignee(s):** (std): SILICON IMAGE INC ; SYNERCHIP CO LTD

**Assignee(s):** DVDO INC ; JEFFERIES FINANCE LLC ; LATTICE SEMICONDUCTOR CORP ; SIBeam INC ; SYNERCHIP CO ;  
WELLS FARGO BANK NATIONAL ASSOCIATION ADMINISTRATIVE AGENT AS

**Inventor(s):** (std): BONG JOON LEE ; LEE BONG JOON

**Agent(s):** ELIZABETH; FENWICK AND WEST LLP

**14) Family number: 42088071** (US2008192814 AA)

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**Title:** SYSTEM AND METHOD FOR PHYSICAL-LAYER TESTING OF HIGH-SPEED SERIAL LINKS IN THEIR MISSION ENVIRONMENTS

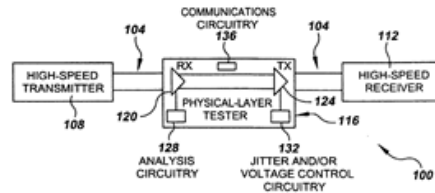
**Abstract:** A physical-layer tester for testing a high-speed serial link between a mission-environment transmitter and a mission-environment receiver. The tester includes a data path and a measurement path. The data path allows a data signal transmitted from the mission-environment transmitter to be passed through the tester to the mission-environment receiver. The measurement path includes circuitry for use in analyzing characteristics of the high-speed serial data traffic on the high-speed serial link. The tester is placed in the high-speed serial link and allows the link to be tested while live, mission-environment data is present on the link. Methods for implementing in-link testing are also disclosed.

**Classifications:****International (IPC 8-9):** G06F13/38 H04B3/46 H04L12/26 H04L25/02**CPC:** G01R31/31711 G01R31/31901 H04L43/50**US:** 375/224 375/224P**JP F-Term:** 5B077 5K029 5B077/NN02 5K029/AA03 5K029/CC01

5K029/KK23 5K029/KK25

**JP F-Index:** G06F13/38,350 H04L25/02,302@A

PatBase - US2008192814\_AA

**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| EP2115940 A2       | 20091111         | EP20080729440      | 20080208         |
| JP2010518760 T2    | 20100527         | JP20090549272T     | 20080208         |
| TW200935781 A      | 20090816         | TW20080117514      | 20080513         |
| US2008192814 AA    | 20080814         | US20080028577      | 20080208         |
| WO08098202 A2      | 20080814         | WO2008US53476      | 20080208         |
| WO08098202 A3      | 20081009         | WO2008US53476      | 20080208         |

**Priority:**

US20070889085P 20070209

WO2008US53476 20080208

US20080028577 20080208

**Probable Assignee:** DFT MICROSYSTEMS INC**Assignee(s):** (std): DANSEREAU DONALD ; DFT MICROSYSTEMS INC ; DUERDEN GEOFFREY ; HAFED MOHAMED M ; LABERGE SEBASTIEN ; NAZON YVON ; TAM CLARENCE KAR LUN**Assignee(s):** ADVANTEST CORP ; DFT MICROSYSTEMS CANADA INC ; DFT MICROSYSTEMS INC US**Inventor(s):** (std): DANSEREAU DONALD ; DUERDEN GEOFFREY ; HAFED MOHAMED M ; LABERGE SEBASTIEN ; NAZON YVON ; TAM CLARENCE KAR LUN**Agent(s):** CHIBA AKIO; DOWNS RACHLIN MARTIN PLLC; HELLER MORGAN S; KOBAYASHI YASUSHI; NAKANISHI MOTOHARU; ONO SHINJIRO; SHAMOTO ICHIO; TOMITA HIROYUKI; WIELSSON JOAKIM PER MAGNUS**Designated states:** AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LA LC LI LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SI SK SL SM SN SV SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW**15) Family number: 37221991** (US2009016421 AA)

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**Title:** PARAMETER CONTROL CIRCUIT

**Abstract:** An interface circuit inputting and outputting data and a clock that have multiple speeds is provided with an equalizer capable of changing a circuit parameter, a frequency detection part detecting a clock frequency, and a parameter calculation control part calculating an appropriate circuit parameter according to the clock frequency and controlling the equalizer. The frequency detection part detects at what frequency the interface circuit is operating presently and sends the frequency to the parameter calculation control part. The parameter calculation control part calculates the circuit parameter of the equalizer so that the interface circuit operates optimally at the detected frequency, and sets the circuit parameter to the equalizer. In this manner, since the circuit parameter of the equalizer in the interface circuit can be controlled appropriately according to the frequency of the input and output clock, optimum operation is always available.

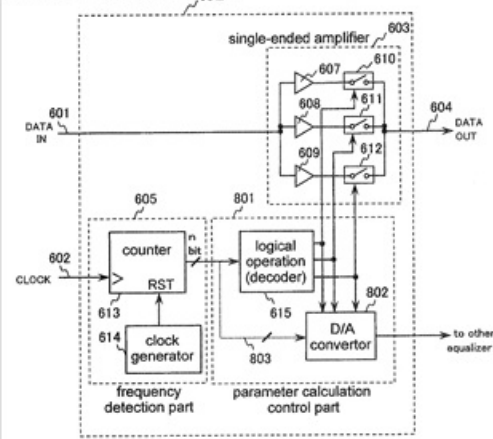
**Classifications:****International (IPC 8-9):** H03H7/30 H03L7/00 H04B3/04 H04L27/01**CPC:** H04B3/04 H04L25/0262 H04L25/028 H04L25/03885**US:** 331/17 331/17S 375/136 375/147 375/229 375/230 375/232

375/232P 375/234

**JP F-Term:** 5K046 5K046/AA01 5K046/EE05 5K046/EE33 5K046/EE46

5K046/EE59

PatBase - US2009016421\_AA

**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| JP4750842 B2       | 20110817         | JP20080506129      | 20060323         |
| JP2007108125 A1    | 20090730         | JP20080506129T     | 20060323         |
| JP4750842 B1       | 20110817         | JP20080506129T     | 20060323         |
| US2009016421 AA    | 20090115         | US20080236375      | 20080923         |
| US8428112 BB       | 20130423         | US20080236375      | 20080923         |
| WO07108125 A1      | 20070927         | WO2006JP305856     | 20060323         |

**Priority:**

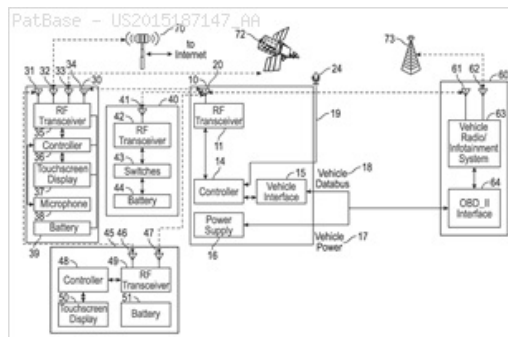
WO2006JP305856 20060323

WO2006JP05856 20060323

US20080236375 20080923

**Probable Assignee:** FUJITSU LTD**Assignee(s):** (std): FUJITSU LTD ; MASAKI SHUNICHIRO**Assignee(s):** FUJITSU LIMITED**Inventor(s):** (std): MASAKI SHUNICHIRO**Agent(s):** ARENT FOX LLP; FURUYA FUMIO**Designated states:** AE AG AL AM AT AU AZ BA BB BE BF BG BJ BR BW BY BZ CA CF CG CH CI CM CN CO CR CU CY CZ DE DK DM DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GW HR HU ID IE IL IN IS IT JP KE KG KM KN KP KR KZ LC LK LR LS LT LU LV LY MA MC MD MG MK ML MN MR MW MX MZ NA NE NG NI NL NO NZ OM PG PH PL PT RO RU SC SD SE SG SI SK SL SM SN SY SZ TD TG TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW**16) Family number: 59629255** (US2015187147 AA)

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**Title:** CONNECTED VEHICLE SYSTEM WITH INFOTAINMENT INTERFACE FOR MOBILE DEVICES**Abstract:** An OBD module comprising a controller; a data bus interface configured to draw power from and electronically communicate with a vehicle OBD-II data port; and a digital interface connector is disclosed. A radio/infotainment interface configured to communicate with the OBD module is disclosed.**Classifications:****International (IPC 8-9):** B60Q1/00 B60R16/02 G01M17/00 G01R31/00 G06F21/36 G06F7/00 G06Q30/02 G06Q40/00 G07C5/00 G07C5/02 G07C5/08 H04L12/40 H04M1/60 H04M1/725 H04W8/24**CPC:** H04L12/40032 B60Q1/00 G01M17/00 G01R31/00 G06F7/00 G06Q30/02 G07C5/00 G07C5/008 G07C5/02 G07C5/08 G07C5/0825 G07C5/0833 H04W8/24 G06F21/36 G06Q40/00 H04M1/60 H04M1/6075 H04M1/72577**US:** 1/1 701/33.2**Family:**

| Publication number     | Publication date | Application number   | Application date |
|------------------------|------------------|----------------------|------------------|
| CA2935617 AA           | 20160629         | CA20142935617        | 20141229         |
| US2015187147 AA        | 20150702         | US20140585557        | 20141230         |
| US9953471 BB           | 20180424         | US20140585557        | 20141230         |
| US10282923 BB          | 20190507         | US20160195113        | 20160628         |
| <b>US2016350984 AA</b> | <b>20161201</b>  | <b>US20160195113</b> | <b>20160628</b>  |
| WO15103159 A1          | 20150709         | WO2014US72600        | 20141229         |

**Priority:**

US20130921576P 20131230

US20140942399P 20140220

WO2014US72600 20141229

US20140585557 20141230

US20150186322P 20150629

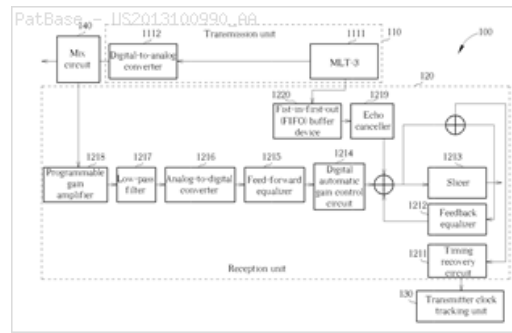
US20150186332P 20150629

US20160195113 20160628

**Probable Assignee:** TIEMAN CRAIG A**Assignee(s):** (std): TIEMAN CRAIG A ; TIEMAN CRAIG ARNOLD**Inventor(s):** (std): TIEMAN CRAIG A ; TIEMAN CRAIG ARNOLD**Agent(s):** ANDRUS INTELLECTUAL PROPERTY LAW LLP; BORDEN LADNER GERVAIS LLP; LOWDER PATRICK D**Designated states:** AE AG AL AM AO AT AU AZ BA BB BE BF BG BH BJ BN BR BW BY BZ CA CF CG CH CI CL CM CN CO CR CU CY CZ DE DK DM DO DZ EC EE EG ES FI FR GA GB GD GE GH GM GN GQ GR GT GW HN HR HU ID IE IL IN IR IS IT JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MC MD ME MG MK ML MN MR MT MW MX MY MZ NA NE NG NI NL NO NZ OM PA PE PG PH PL PT QA RO RS RU RW SA SC SD SE SG SI SK SL SM SN ST SV SY SZ TD TG TH TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW**17) Family number: 53537937** (US2013100990 AA)

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**Title:** TRANSCIVER CAPABLE OF DYNAMICALLY ADJUSTING TRANSMITTER CLOCK AND RELATED METHOD THEREOF**Abstract:** A transceiver for dynamically adjusting a transmission clock includes: a transmitting unit, a receiving unit, and a transmission clock tracking unit. The transmitting unit is arranged for transmitting a transmission signal according to the transmission clock. The receiving unit is arranged for receiving a reception signal. The transmission clock tracking unit is coupled to the transmitting unit and the receiving unit, and arranged for dynamically controlling the transmission clock of the transmitting unit according to a reception clock corresponding to the reception signal.**Classifications:****International (IPC 8-9):** H04B1/38 H04L5/16 H04L7/00 H04L7/027**CPC:** H04L7/0004 H04L7/0062 H04L7/0091**US:** 375/219 375/259



#### Family:

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| TW201318392 A          | 20130501         | TW20110138392      | 20111021         |
| TWI466522 B            | 20141221         | TW20110138392      | 20111021         |
| <b>US2013100990 AA</b> | 20130425         | US20120615504      | 20120913         |
| <b>US8861573 BB</b>    | 20141014         | US20120615504      | 20120913         |

#### Priority:

TW20110138392 20111021

**Probable Assignee:** REALTEK SEMICONDUCTOR CORP

**Assignee(s):** (std): CHU YUAN JIH ; HSU MING FENG ; HUANG LIANG WEI ; REALTEK SEMICONDUCTOR CORP ; SU CHING YAO

**Inventor(s):** (std): CHU YUAN JIH ; HSU MING FENG ; HUANG LIANG WEI ; SU CHING YAO

**Agent(s):** SCOTT; WINSTON

#### 18) Family number: 42231875 (US2008240230 AA)

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**Title:** MEDIA PROCESSOR WITH AN INTEGRATED TV RECEIVER

**Abstract:** An integrated circuit for processing a media stream, including an RF input interface, an RF receiver unit configured for receiving an RF media stream from the RF input interface and extracting the media stream from the RF media stream, an input interface unit configured for receiving the media stream from a content source, a plurality of processing units, a switch, operatively connected to the RF receiver unit, to the input interface unit, and to each of the processing units, the switch configured to allow more than one of the operatively connected units to simultaneously receive the media stream, thereby allowing simultaneous processing of the media stream by the processing units, and an output interface, operatively connected to the switch, configured for outputting the simultaneously processed media stream. Related apparatus and methods are also described.

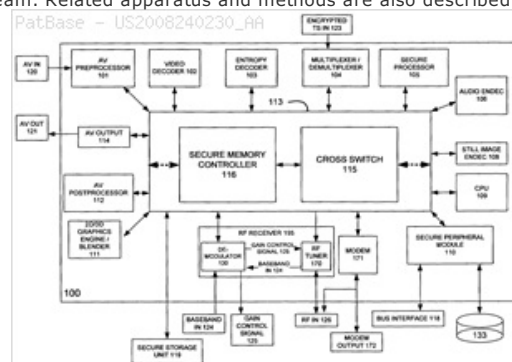
#### Classifications:

**International (IPC 8-9):** H04N11/04

**CPC:** H04N21/23608 H04N21/426 H04N21/4344 H04N21/4382

H04N21/4383 H04N21/4622 H04N5/46

**US:** 348/E5.108 348/E5.114 348/E51.08S 348/E51.14S 375/240.01 375/240.010P 375/E7.001 375/E70.01S



#### Family:

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| <b>US2008240230 AA</b> | 20081002         | US20070730070      | 20070329         |

#### Priority:

US20070730070 20070329

**Probable Assignee:** TESSERA INC

**Assignee(s):** (std): HORIZON SEMICONDUCTORS LTD

**Assignee(s):** DIGITALOPTICS INT CORP ; TESSERA INC

**Inventor(s):** (std): KHRAPKOVSKY MICHAEL ; LANDIS SHAY ; MORAD AMIR ; OXMAN GEDALIA ; TWITO MOSHE ; YAVITS LEONID

**Agent(s):** MARTIN D MOYNIHAN PRTSI INC

#### 19) Family number: 52082338 (US2012257103 AA)

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**Title:** SMALL FORM FACTOR PLUGGABLE UNIT WITH SIGNAL CONVERSION CAPABILITIES

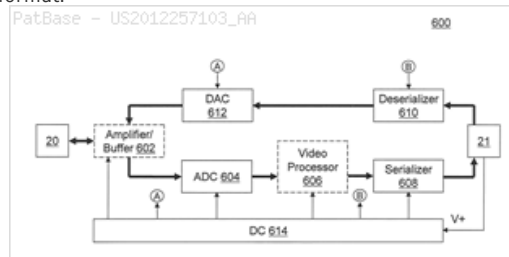
**Abstract:** The present disclosure relates to devices comprising small form factor pluggable units (SFP) having connectors for receiving and sending signals and a processor for converting the received signals prior to sending the converted signals. Received or sent signals may comprise video signals in various analog or digital formats. Conversion of the received signals may comprise analog to digital or digital to analog conversion, serializing or deserializing a digital signal, frame synchronization of a video signal, and/or cross conversion of a video signal from a first format to a second format.

**Classifications:**

**International (IPC 8-9):** H03M1/00 H04B10/00 H04B10/40 H04N11/20 H04N11/24 H04N5/44 H04N7/01 H04N7/24 H05K7/02 H05K7/14

**CPC:** G09G2370/04 G09G5/005 H04B10/40 H04L25/12 H04N11/20 H04N11/24 H04N7/01 H04N7/0125

**US:** 348/441 348/725 348/E.096 348/E.003 398/135 398/138



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| CA2774849 AA       | 20121008         | CA20122774849      | 20120410         |
| CA2774849 C        | 20151020         | CA20122774849      | 20120410         |
| US2012257103 AA    | 20121011         | US20110082628      | 20110408         |
| US8761604 BB       | 20140624         | US20110082628      | 20110408         |
| US2014240592 AA    | 20140828         | US20140275343      | 20140512         |

**Priority:**

US20110082628 20110408 CA20122774849 20120410 US20140275343 20140512

**Probable Assignee:** EMBRIONIX DESIGN INC

**Assignee(s):** (std): DUDEMAINE ERIC ; EMBRIONIX DESIGN INC ; EMBRYONIX DESIGN INC ; LAVOIE RENAUD

**Assignee(s):** RIEDEL COMMUNICATIONS CANADA INC

**Inventor(s):** (std): DUDEMAINE ERIC ; LAVOIE RENAUD

**Agent(s):** BCF LLP; IP DELTA PLUS INC

**20) Family number: 51430543 (US2012170735 AA)**

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**Title:** COMMUNICATION APPARATUS FOR RAPIDLY ADJUSTING ANALOG ECHO CANCELLATION CIRCUIT AND RELATED ECHO CANCELLATION METHOD

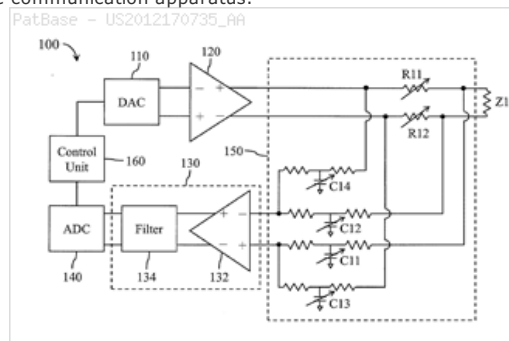
**Abstract:** A communication apparatus is disclosed including: an analog-front-end circuit for receiving and processing an analog input signal; an analog-to-digital converter (ADC) coupled with the analog-front-end circuit for converting processed signal from the analog-front-end circuit into a digital input signal; and a control unit coupled with the ADC for adjusting at least one resistance and/or at least one capacitance in an analog echo cancellation circuit according to the digital input signal before the analog-front-end circuit receives a training sequence that is the first training sequence transmitted from a second communication apparatus after the second communication apparatus begins communicating with the communication apparatus.

**Classifications:**

**International (IPC 8-9):** H04B3/20 H04M9/08

**CPC:** H04B3/238

**US:** 379/406.1 379/406.100P



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| CN102545960 A      | 20120704         | CN201110046964     | 20110225         |
| CN102545960 B      | 20151216         | CN201110046964     | 20110225         |
| TW201228266 A      | 20120701         | TW20100146589      | 20101229         |
| TWI452854 B        | 20140911         | TW20100146589      | 20101229         |
| US2012170735 AA    | 20120705         | US20110339255      | 20111228         |
| US8670555 BB       | 20140311         | US20110339255      | 20111228         |

**Priority:**

TW20100146589 20101229

**Probable Assignee:** REALTEK SEMICONDUCTOR CORP

**Assignee(s):** (std): HSU TZU HAN ; HUANG LIANG WEI ; KUO SHIEH HSING ; LIU JUI YI ; REALTEK SEMICONDUCTOR CORP

**Inventor(s):** (std): HSU TZU HAN ; HUANG LIANG WEI ; JUI YI LIU ; KUO SHIEH HSING ; LIANG WEI HUANG ; LIU JUI YI ; SHIEH HSING KUO ; TZU HAN HSU

**Agent(s):** BIRCH STEWART KOLASCH AND BIRCH LLP

**Title:** ADAPTIVE PADE FILTER AND TRANSCEIVER

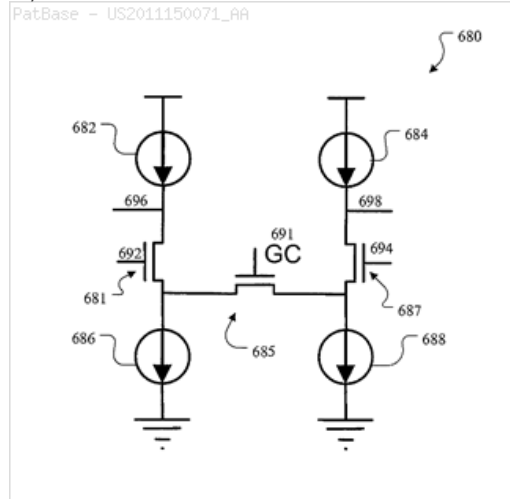
**Abstract:** According to an embodiment of the disclosure, a communication transmitter and receiver include an adaptive filter and a decision feedback equalizer as well as cross-talk cancellers. The adaptive filter is configured to receive an input signal and includes a continuous analog delay circuit with a plurality of Pade-based delay elements.

**Classifications:**

**International (IPC 8-9):** H03H11/26 H03H11/46 H03H15/02 H03H21/00 H03H7/30 H03H7/40 H03K5/159 H04B3/32 H04L1/00 H04L25/03 H04L27/01 H04L27/06

**CPC:** H03H11/26 H03H11/46 H03H15/02 H03H21/0001 H04B3/32 H04L1/0047 H04L2025/03477 H04L2025/0349 H04L2025/03503 H04L2025/03598 H04L25/03038 H04L25/03057 H04L25/03133 H04L25/03343

**US:** 375/230 375/230S 375/232 375/232S 375/233 375/233P 375/316 375/316S 375/348



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| US2011150071 AA    | 20110623         | US20100905912      | 20101015         |
| US8929429 BB       | 20150106         | US20100905912      | 20101015         |
| US2015256360 AA    | 20150910         | US20150589872      | 20150105         |

**Priority:**

US20090252050P 20091015      US20100905912 20101015      US20150589872 20150105

**Probable Assignee:** TAKATORI HIROSHI

**Assignee(s):** (std): TAKATORI HIROSHI ; VARELIAN ALBERT ; ZABRODA ALEX OLEKSIY ; ZABRODA OLEKSIY

**Inventor(s):** (std): TAKATORI HIROSHI ; VARELIAN ALBERT ; ZABRODA ALEX OLEKSIY ; ZABRODA OLEKSIY

**Inventor(s):** ZABRODA ALEX (OLEKSIY)

**Agent(s):** ROBERT D

**Title:** PASS THROUGH DIGITAL TELEVISION SIGNAL THROUGH NON-TV CONSUMER ELECTRONICS (CE) DEVICE

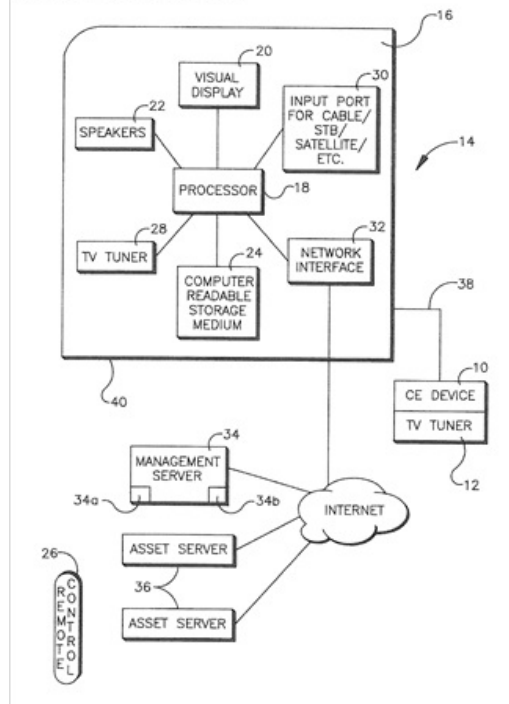
**Abstract:** A digital TV tuner is included in an audio or video device that typically does not have a TV tuner or is expected to have a TV tuner. Such provisioning affords a user free access to broadcast (e.g., NBC, CBS, ABC, Fox, PBS, etc.) channels that may otherwise be provided by another third party via paid subscription or other service level as part of a package, thus allowing consumers the choice of bypassing their cable or satellite or other video content service provider by providing access to readily available broadcast video content services. Devices in which the digital TV tuner include but are not limited to Blu-ray players; streaming media players; audio receivers; soundbars; multi-room audio speakers or source devices; cameras; camcorders; personal audio players; and portable DVD or Blu-ray players.

**Classifications:**

**International (IPC 8-9):** H04N21/254 H04N5/50

**CPC:** H04N21/41407 H04N21/418 H04N21/43635

**US:** 348/731 348/E5.097

**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| CN102821315 A          | 20121212         | CN201210166993     | 20120523         |
| <b>US2012314139 AA</b> | 20121213         | US20110154900      | 20110607         |

**Priority:**

US20110154900 20110607

**Probable Assignee:**

SONY CORP

**Assignee(s):** (std):

SIEGEL BRIAN M ; SONY CORP

**Inventor(s):** (std):

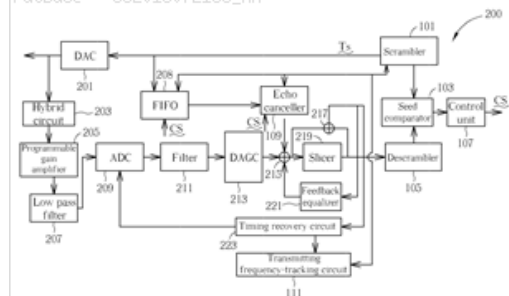
SIEGEL BRIAN M

**23) Family number: 53273806** (US2013072133 AA)

© PatBase

**Title:** SIGNAL TRANSCIVING METHOD, SIGNAL TRANSCIVER UTILIZING THE SIGNAL TRANSCIVING METHOD, NETWORK CONNECTION METHOD AND NETWORK DEVICE UTILIZING THE NETWORK CONNECTION METHOD

**Abstract:** A signal transceiving method, applied to a signal transceiver, includes: adjusting to approximate a value of a clock frequency of a signal to be transmitted from the signal transceiver to a value of a clock frequency of a received signal; performing an echo cancellation operation; computing a distance between a first certification code transmitted by the signal transceiver and a second certification code received by the signal transceiver; and stopping the echo cancellation operation when the distance is smaller than a threshold value.

**Classifications:****International (IPC 8-9):** H04B1/38 H04B15/00 H04L12/46 H04M9/08**CPC:** H04B1/38 H04B15/00 H04B3/20**US:** 379/406.01 455/501 455/570 455/63.1 455/73**Family:**

| Publication number     | Publication date | Application number | Application date |
|------------------------|------------------|--------------------|------------------|
| CN103002169 A          | 20130327         | CN201110276303     | 20110916         |
| CN103002169 B          | 20141126         | CN201110276303     | 20110916         |
| <b>US2013072133 AA</b> | 20130321         | US20120609246      | 20120910         |
| <b>US8787844 BB</b>    | 20140722         | US20120609246      | 20120910         |

**Priority:**

CN201110276303 20110916

**Probable Assignee:** REALTEK SEMICONDUCTOR CORP

**Assignee(s):** (std): CHU YUAN JIH ; HSU MING FENG ; HUANG LIANG WEI ; REALTEK SEMICONDUCTOR CORP ; SU CHING YAO  
**Inventor(s):** (std): CHU YUAN JIH ; HSU MING FENG ; HUANG LIANG WEI ; SU CHING YAO ; SU JINGYAO ; XU MINGFENG ; ZHU YUANZHI  
**Agent(s):** SCOTT; WINSTON

#### 24) Family number: 50889049 (US8151121 BA)

PatBase

**Title:** SECURE DATA STORAGE

**Abstract:** Securely storing data to an optical disc has been described, including generating write data that includes the data and overhead data that facilitates reading the data from the disc; and configuring the overhead data according to a key.

**Classifications:**

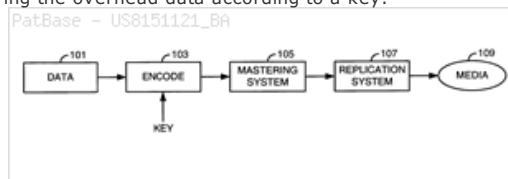
**International (IPC 8-9):** G06F21/00

**CPC:** G11B20/00086 G11B20/0021 G11B20/00289 G11B20/00536

G11B20/00557 G11B20/10027 G11B20/10046 G11B20/1403

G11B20/1426 G11B20/1496 G11B2220/2537 G11B2220/2562

**US:** 713/193



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| US8151121 BA       | 20120403         | US20030387232      | 20030311         |

**Priority:**

US20030387232 20030311

**Probable Assignee:** AVAGO TECHNOLOGIES LTD

**Assignee(s):** (std): HARVEY IAN E ; LEE DAVID C ; LEWIS GREG S ; LSI CORP ; SPIELMAN STEVEN R ; TAN CHRISTOPHER C ; WARLAND DAVID K ; WONG TERRENCE L

**Assignee(s):** AGERE SYSTEMS LLC ; AVAGO TECHNOLOGIES GENERAL IP SINGAPORE PTE LTD ; AVAGO TECHNOLOGIES INT SALES PTE LTD ; AVAGO TECHNOLOGIES LTD ; BANK OF AMERICA NA COLLATERAL AGENT AS ; CALIMETRICS INC ; DEUTSCHE BANK NEW YORK BRANCH COLLATERAL AGENT AG AS ; LSI LOGIC CORP ; MICROSOFT CAPITAL CORP

**Inventor(s):** (std): HARVEY IAN E ; LEE DAVID C ; LEWIS GREG S ; SPIELMAN STEVEN R ; TAN CHRISTOPHER C ; WARLAND DAVID K ; WONG TERRENCE L

**Agent(s):** CHRISTOPHER P

#### 25) Family number: 62876300 (US9392381 BA)

PatBase

**Title:** HEARING AID ATTACHED TO MOBILE ELECTRONIC DEVICE

**Abstract:** Disclosed is a hearing aid attached to a mobile electronic device. Elements forming the hearing aid are separated into a main hearing aid device and a sub-hearing aid device. The main hearing aid device is attached to the casing of a mobile electronic device and connected to the mobile electronic device through a wired cable, and the sub-hearing aid device is placed in an ear of a user. Other people rarely notice that a user uses the hearing aid because the main hearing aid device is mounted on the casing of a mobile electronic device. The hearing aid is supplied with power from the battery of the mobile electronic device, and has the same size as the casing of the mobile electronic device. Accordingly, a beamforming operation through a microphone array is possible, and use convenience and a level of satisfaction of the hearing aid can be improved.

**Classifications:**

**International (IPC 8-9):** H04M1/60 H04R1/10 H04R1/40 H04R25/00

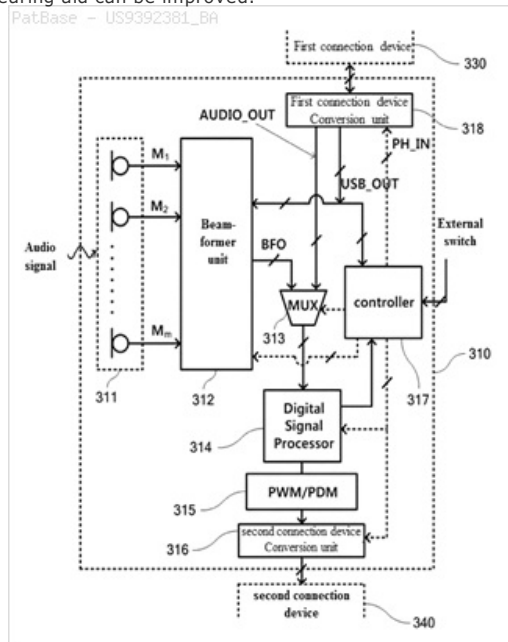
H04R3/00

**CPC:** H04M1/60 H04R1/1083 H04R1/40 H04R1/406 H04R2201/401

H04R2203/12 H04R2225/41 H04R2420/09 H04R2430/20 H04R2499/11

H04R25/402 H04R25/407 H04R25/554 H04R25/556 H04R3/00

**US:** 1/1



**Family:**

| Publication number | Publication date | Application number | Application date |
|--------------------|------------------|--------------------|------------------|
| KR101648840 B1     | 20160830         | KR20150023394      | 20150216         |
| US9392381 BA       | 20160712         | US20150795266      | 20150709         |

**Priority:**

KR20150023394 20150216

**Probable Assignee:** POSTECH ACADEMY IND FOUNDATION

**Assignee(s):** (std): POSTECH ACAD IND FOUND

**Assignee(s):** POSTECH ACADEMY IND FOUNDATION ; POSTECH ACADEMY INDUSTRY FOUNDATION

**Inventor(s):** (std): CHO SEONG EUN ; JANG YOUNG JAE ; NOH HYEON KYU ; PARK HONG JUNE ; PARK SANG HU ; YEO DONG HEE

**Agent(s):** KILE PARK REED AND HOUTTEMAN PLLC