

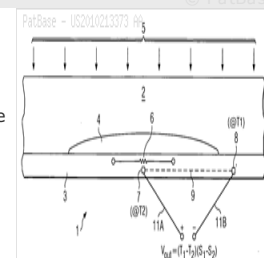
1) Family number: 46625122 (US2010213373 AA)

INFRARED SENSOR STRUCTURE AND METHOD

Abstract: Source: US2010213373 AA A radiation sensor (27) includes a radiation sensor chip (1) including first (7) and second (8) thermopile junctions connected to form a thermopile (7,8). The first thermopile junction is disposed in a floating portion of a dielectric membrane (3) thermally insulated from a silicon substrate (2) of the chip, and the second thermopile junction is disposed in the dielectric membrane directly adjacent to the substrate. Bump conductors (28) are bonded to corresponding bonding pads (28A) coupled to the thermopile (7,8) to physically and electrically connect the chip to conductors on a printed circuit board (23). The silicon substrate transmits infrared radiation to the thermopile while blocking visible light.

Probable Assignee: TEXAS INSTRUMENTS INC

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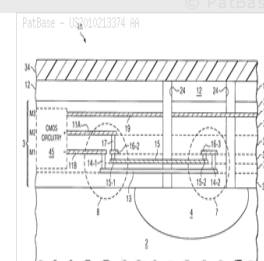
2) Family number: 46625128 (US2010213374 AA)

ON-CHIP CALIBRATION SYSTEM AND METHOD FOR INFRARED SENSOR

Abstract: Source: US2010213374 AA A radiation sensor includes an integrated circuit radiation sensor chip (1A) including first (7) and second (8) thermopile junctions connected in series to form a thermopile (7,8) within a dielectric stack (3). The first thermopile junction (7) is insulated from a substrate (2) of the chip. A resistive heater (6) in the dielectric stack for heating the first thermopile junction is coupled to a calibration circuit (67) for calibrating responsivity of the thermopile (7,8). The calibration circuit causes a current flow in the heater and multiplies the current by a resulting voltage across the heater to determine power dissipation. A resulting thermoelectric voltage (V_{out}) of the thermopile (7,8) is divided by the power to provide the responsivity of the sensor.

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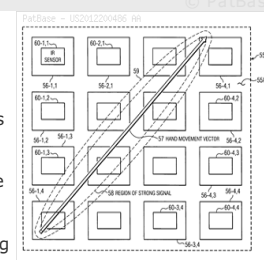
3) Family number: 51717372 (US2012200486 AA)

INFRARED GESTURE RECOGNITION DEVICE AND METHOD

Abstract: Source: US2012200486 AA A system for generating tracking coordinate information in response to movement of an information-indicating element includes an array (55) of IR sensors (60-x,y) disposed along a surface (55A) of the array. Each IR sensor includes first (7) and second (8) thermopile junctions connected in series to form a thermopile (7,8) within a dielectric stack (3) of a radiation sensor chip (1). The first thermopile junction is more thermally insulated from a substrate (2) of the radiation sensor chip than the second thermopile junction. A sensor output signal between the first and second thermopile junctions is coupled to a bus (63). A processing device (64) is coupled to the bus for operating on information representing temperature differences between the first and second thermopile junctions of the various IR sensors, respectively, caused by the presence of the information-indicating element to produce the tracking coordinate information as the information-indicating element moves along the surface.

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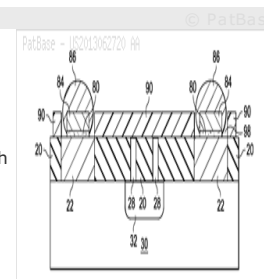
4) Family number: 53195510 (US2013062720 AA)

EXTENDED AREA COVER PLATE FOR INTEGRATED INFRARED SENSOR

Abstract: Source: US2013062720 AA An integrated circuit chip includes a window cover over etchant holes in a dielectric layer and over a cavity in the substrate of said integrated circuit chip. The window cover extends at least 400 microns beyond the edge of the cavity. An integrated sensor chip with a sensor cover which extends at least 400 microns beyond the edges of a cavity. A method of forming an integrated sensor chip with a sensor cover which extends at least 400 microns beyond the edge of a cavity.

Probable Assignee: TEXAS INSTRUMENTS INC

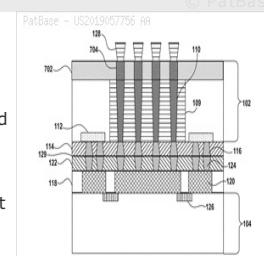
Earliest Publication Date: 20130314



5) Family number: 66253773 (US2019057756 AA)

STRUCTURE AND METHOD FOR TESTING THREE-DIMENSIONAL MEMORY DEVICE

Abstract: Source: US2019057756 AA Embodiments of structures and methods for testing three-dimensional (3D) memory devices are disclosed. In one example, a 3D memory device includes a memory array structure, a peripheral device structure, and an interconnect layer in contact with a front side of the memory array structure and a front side of the peripheral device structure, and a conductive pad at a back side of the memory array structure and that overlaps the memory array structure. The memory array structure includes a memory array stack, a through array contact (TAC) extending vertically through at least part of the memory array stack, and a memory array contact. The peripheral device structure includes a test circuit. The interconnect layer includes an interconnect structure. The conductive pad, the TAC, the interconnect structure, and at least one of the test circuit and the memory array contact are electrically connected.



Probable Assignee: YANGTZE MEMORY TECHNOLOGIES CO LTD

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