



(51) International Patent Classification:

G06K 19/077 (2006.01)

(21) International Application Number:

PCT/CN2022/104250

(22) International Filing Date:

07 July 2022 (07.07.2022)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/222,560

16 July 2021 (16.07.2021)

US

(71) Applicant: ACT IDENTITY TECHNOLOGY LIMITED [CN/CN]; Room 24A, 9/F., Well Fung Industrial Centre, 68 Ta Chuen Ping Street, Kwai Chung, New Territories, Hong Kong (CN).

(72) Inventor: CHEN, Gang; Room 24A, 9/F., Well Fung Industrial Centre, 68 Ta Chuen Ping Street, Kwai Chung, New Territories, Hong Kong (CN).

(74) Agent: RUNPING & PARTNERS; Suite 515, Yingu Mansion, No.9 Beisihuanxilu, Haidian District, Beijing 100190 (CN).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) Title: CHIP MODULE AND METHOD OF FORMING SAME

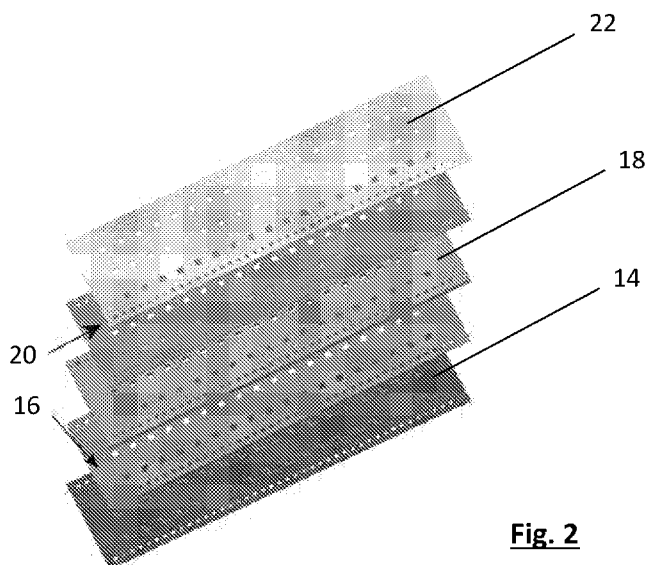


Fig. 2

(57) Abstract: A chip module (40a, 40b, 62) is disclosed as including an integrated-circuit (IC) chip (34, 64), a first flexible substrate layer (18) with a number of holes (28), a second adhesive substrate layer (16) with a number of holes (26), and a third substrate layer (14) made of an electrically conductive material, the second substrate layer being sandwiched between and fixedly engaged with the first and third substrate layers, the holes of the first substrate layer and the holes of the second substrate layer being aligned with each other to form a number of cavities (12, 66) each receiving at least a part of the IC chip.



TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*